

Effective Doping Concentration Theory: A New Physical Insight for the Double-RESURF Lateral Power Devices on SOI Substrate

Jun Zhan[g](https://orcid.org/0000-0002-5688-295X)[®], Student Member, IEEE, [Yu](https://orcid.org/0000-0003-2970-993X)-Feng Guo, Member, IEEE, David Z. Pan, Fellow, IEEE, Ke-Meng Yangⁿ, Xiao-Juan Lian, and Jia-Fei Yao

Abstract—Double-reduced surface field (D-RESURF) technique aims to increase the doping concentration of drift regions and maintain a high breakdown voltage. However, conventional 2-D models are too complicated and unable to elaborate its physical meaning. Hence, the D-RESURF effective doping concentration (EDC) theory is proposed in this paper to explore the physical insight of the D-RESURF effect by equating the sophisticated 2-D structure to a simple 1-D RESURF model with segmented-dopedp-n junction.The EDC indicates that an NPNP structure may exist because of the influence of the P-top region. Thus, two electric field valleys and one electric field peak can be formed on the surface. Based on the theory, a 1-D analytical model is presented to qualitatively and quantitatively explore the impact of D-RESURF effect on breakdown mechanism of silicon on insulator lateral double diffusion MOS. The results obtained by the proposed model are found to be sufficiently accurate comparing with TCAD simulation results.

Index Terms—1-D model, breakdown voltage (BV), double RESURF (D-RESURF), effective doping.

I. INTRODUCTION

THE development of lateral power devices has made
revolutionary progress as the introduction of reduced surface field (RESURF) technique [1]–[4]. One of the key challenges for designing lateral power devices is to obtain high breakdown voltage (BV), low specific ON-resistance (R_{ON}) , and reasonable costs simultaneously [5]–[9]. Compared to single-RESUR technique (S-RESURF), double-RESURF

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J. Zhang, Y.-F. Guo, K.-M. Yang, X.-J. Lian, and J.-F. Yao are with the College of Electronic Science and Engineering and also with the National and Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, Nanjing University of Posts and Telecommunications, Nanjing 210023, China (e-mail: bravaisxx@163.com; yfguo@njupt.edu.cn; b09020726@outlook.com).

D. Z. Pan is with the College of Electronic Science and Engineering and also with the National and Local Joint Engineering Laboratory for RF Integration and Micro-Packaging Technologies, Nanjing University of Posts and Telecommunications, Nanjing 210023, China, and also with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78712 USA.

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(D-RESURF) enables designers to obtain a better tradeoff between BV and R_{ON} via inserting a p-type top layer into the n-type drift region [4], [5]. Owing to the P-top region, D-RESURF lateral double diffusion MOS (LDMOS) provides a higher doping concentration (N_d) in drift regions to reduce R_{ON} and keep a high BV compared to an S-RESURF LDMOS [3]–[5]. Such improvements are qualitatively attributed to the two-sided vertical depletion in D-RESURF. As such, researchers [4], [5] have proposed that the doping concentration of drift region can be increased by two times as much as that in S-RESURF while BV is maintained. In order to quantitatively analyze the influence of the D-RESURF effect on BV, researchers have made the greatest efforts on the development of theoretical model, Conventional analytical models depict BV, and surface electric field of drift region based on 2-D Poisson's equation due to the geometric complexity of the drift region. These 2-D models can effectively analyze 2-D potential and electric field distribution. Nevertheless, the mathematical expressions of these 2-D models are very complicated and lack of clear physical meaning. More importantly, 2-D models are usually incapable of providing a theoretical guidance on optimizing the structure parameters due to its complicated expressions [4], [5], [11]–[14].

In this paper, in order to take the benefits of both the simplicity of 1-D models and the veracity of 2-D models, we propose the D-RESURF effective doping concentration (EDC) theory to simplify the complicated 2-D D-RESURF effect into a 1-D problem. The EDC theory indicates that the P-top region in drift region results in an equivalent NP, NPN, or NPNP structure. Therefore, an electric field peak occurs at the interface between Regions II and III. Furthermore, the D-RESURF technique can be treated as an S-RESURF with segmented-doped drift region. Based on this theory, we further developed a 1-D analytical model for D-RESURF lateral power device. To our knowledge, the proposed D-RESURF EDC theory and corresponding 1-D model for silicon on insulator (SOI) D-RESURF LDMOS is the first methodology that can provide a clear, reasonable, and simple explanation of the D-RESURF effects. The analytical model is validated by the good agreement between the modeling results and simulation results by MEDICI, a commercial TCAD tool. The simulation models used in MEDICI are CONSRH, AUGER, BGN, FLDMOB, IMPACT.I, and CCSMOB [1], [6], [7].

Fig. 1. 2-D cross section of (a) SOI Double LDMOS and (b) EDC equivalent structure for modeling (xy plane).

II. EFFECTIVE DOPING CONCENTRATION

The EDC theory assumes that the influence of 2-D RESURF effects on the breakdown characteristic of drift region can be represented by a 1-D model with gradually doped p-n junction. In this paper, we assume that compared to the S-RESURF, D-RESURF affects the EDC of the drift region to obtain a lower EDC and form a new electric peak, and ultimately achieve a better tradeoff between R_{ON} and BV. To determine EDC, the 2-D cross section shown in Fig. $1(a)$ is used for modeling. In Fig. $1(a)$, a P-top region is on the top of the drift region and the doping concentrations of P-top and drift region are *P*top and *Nd* , respectively. Due to the existence of the P-top region, the n-type drift region is divided into four subregions along the P-top region edges, and the region boundary is given by $x = 0$, L_1 , $L_1 + L_p$, L_d and $y = 0$, t_{top} , t_s . When the device is reversely biased, a depletion region is formed to sustain the applied voltage. Meanwhile, the potential function in the silicon must be satisfied by 2-D Poisson's equation, which yields

$$
\frac{\partial^2 \varphi_i(x, y)}{\partial x^2} + \frac{\partial^2 \varphi_i(x, y)}{\partial y^2} = -\frac{q N_i}{\varepsilon_s}, \quad i = \text{I, II, III, IV} \quad (1)
$$

where q is the electronic charge, ε_s is the dielectric constant of Silicon, N_d is the doping concentration of drift region, P_{top} is the P-top region doping concentration, and $N_1 = N_3$ $N_4 = N_d$ and $N_2 = P_{top}$. The second-order Taylor series expansion along the *y*-dimension is employed to approximate the electric potential

$$
\varphi_i(x, y) = \varphi_i(x, 0) + \frac{\partial \varphi_i(x, y)}{\partial y}\bigg|_{y=0} y + \frac{\partial^2 \varphi_i(x, y)}{\partial y^2}\bigg|_{y=0} \frac{y^2}{2}.
$$
\n(2)

$$
\frac{\partial^2 \varphi_i(x,0)}{\partial x^2} - \frac{\varphi_i(x,0)}{t^2} = -\frac{qN_d}{\varepsilon_s}, \quad i = \text{I, III} \tag{3}
$$

$$
\frac{\partial^2 \varphi_i(x,0)}{\partial x^2} - \frac{\varphi_i(x,0)}{t^2} = -\frac{q(N_d - N_{\text{et}})}{\varepsilon_s}, \quad i = \text{II} \tag{4}
$$

where $t = (0.5t_s^2 + Kt_s t_{ox})^{0.5}$ is the characteristic thickness [5], [16], $K = \varepsilon_s/\varepsilon_{\text{ox}} \approx 3$ is the dielectric constant ratio of silicon and silicon dioxide material, *ts* being the epitaxial layer thickness, *t*ox represents the thickness of the buried oxide layer, and $N_{\text{et}} = (N_d + P_{\text{top}})(Kt_{\text{top}}t_{\text{ox}} + t_{\text{top}}t_s - t_{\text{top}}^2/2)t^2$ indicates the influence of P-top region on the drift region EDC. It worth noting that (4) is exactly the same as the corresponding expression in the 2-D model [5].

So far, a set of accurate but complicated surface electric field and potential expressions could be obtained via directly solving the 2-D equation in Regions I–IV, respectively. Nevertheless, in order to elaborate the D-RESURF effect and provide the designing guidance of device parameters, we need to reduce the dimension of inherited 2-D equations. Furthermore, the dimension-reduction method proposed in [7] is employed to reduce the dimension of 2-D Poisson's equations such as (3) and (4) . As shown in Fig. $1(b)$, such dimensionreduction method assumes that the charges in sharing charge region (SCR) only partially contribute to the lateral junction due to the overlapping between lateral and vertical depletion regions. The charge appointment line shown in Fig. $1(b)$ divided the SCR into the upper and lower parts, and only the charge in upper part contributes to the lateral junction. The SCR is limited by the lateral and vertical depletion length x_{lat} and x_{ver} , respectively. Thus, $\eta = x_{\text{ver}}(V_{\text{app}})/t_s$ is the ratio of the spreading of the vertical depletion region into the epitaxial layer and SOI layer thickness which indicates the coupling degree between lateral and vertical structure. Accordingly, the effect of 2-D coupling between vertical and lateral structures can be transformed into the variation of the drift region EDC. By using the dimension-reduction method reported in [7], (3) and (4) can be further simplified as

$$
\frac{d^2\varphi_i(x,0)}{dx^2} = \frac{dE_i(x,0)}{dx} = -\frac{qN_{\text{eff}}^{\text{I,III}}}{\varepsilon_s}, \quad i = \text{I, III} \tag{5}
$$

$$
\frac{d^2\varphi_i(x,0)}{dx^2} = \frac{dE_i(x,0)}{dx} = -\frac{qN_{\text{eff}}^{\text{II}}}{\varepsilon_s}, \quad i = \text{II}
$$
 (6)

where for the full-depletion case, $N_{\text{eff}}^{\text{II}} = N_d (1 - \eta \cdot x / L_d) - N_{\text{et}}$, $N_{\text{eff}}^{\text{I,III}} = N_d (1 - \eta \cdot x / L_d)$ being the EDC of regions II and I, III, respectively. Therefore, due to the existence of the P-top region, the EDC of the Region II is reduced largely. In the one hand, a lower EDC can sustain a higher reverse-biased applied voltage. On the other hand, as the result of the incoherence of the EDC in the drift region, a third electric field peak may be expected at the interface between Regions II and III.

Fig. 2. Drift region EDC of the drift region for for various (a) applied voltage ($P_{\text{top}} = 1.5 \times 10^{15}$ cm⁻³, $N_d = 1.5 \times 10^{15}$ cm⁻³, and $t_{\text{top}} =$ 1.5 μ m), (b) P-top region doping ($V_{\text{app}} = 200$ V, $t_{\text{top}} = 1.5$ μ m, and $N_d = 1.5 \times 10^{15}$ cm⁻³), (c) P-top region thickness (V_{app} = 200 V, $P_\mathsf{top}=1.5\times10^{15}$ cm $^{-3}$, and $\mathcal{N}_d=1.5\times10^{15}$ cm $^{-3}$), and (\mathbf{d}) drift region doping (V_{app} = 200 V, t_{top} = 1.5 μ m, and P_{top} = 1.5 \times 10¹⁵ cm⁻³) with $t_{\text{ox}} = 2 \ \mu \text{m}, t_{\text{s}} = 7 \ \mu \text{m}, L_1 = 3 \ \mu \text{m}, L_p = 17 \ \mu \text{m}, \text{and } L_d = 30 \ \mu \text{m}.$

Furthermore, the EDC can be obtained accordingly, which yields

$$
N(x) = \begin{cases} N_d \left(1 - \eta \frac{x}{L_d}\right) & 0 \le x \le L_1 \\ N_d \left(1 - \eta \frac{x}{L_d}\right) - N_{\text{et}} & L_1 \le x \le L_1 + L_p \\ N_d \left(1 - \eta \frac{x}{L_d}\right) & L_1 + L_p \le x \le L_d. \end{cases}
$$

It is worth noting that the proposed methodology also can be applied to the bulk silicon D-RESURF LDMOS. For the bulk silicon D-RESURF LDMOS case, (7) need to be amended by using the dimension-reduction method proposed in [6], accordingly. Obviously, when t_{top} equals to zero or P_{top} equals to $-N_d$, the influence of D-RESURF effect apparently would no longer exist, and (7) is consistent with the S-RESURF case [15]. So far, as (7) indicates, the original 2-D D-RESURF lateral power device is equivalent to a single-side abrupt junction with varied doping concentration.

Fig. 2 intuitively shows the variation of drift region EDC under varied bias and structure conditions under the condition of full depletion. The EDC has a big drop at the interface between Regions I and II as a result of the P-top region, shown in Fig. $2(a)$. The same like that in S-RESURF, an equivalent p-type region would appear in Region II and then form an equivalent $P(x)N(x)$ junction. Apparently, as shown in Fig. 2(b) and (c), the variation of EDC in Region II is a strong function of the P-top region doping dose ($Q_{top} = P_{top} \times t_{top}$). As Fig. $2(a)$ and (d) clearly shows, there are three possible cases for Region III which are n-type, np-type, and p-type. Fig. 3(a) shows that for an n-type equivalent Region III, there is only one forward-biased p-n junction in Region III. The n-type Region III case occurs when drift region is partially

Fig. 3. Effective lateral structure and the electric field distribution of the D-RESURF device at the: (a) n-type, (b) np-type, and (c) p-type Region III.

depleted or just fully depleted, namely, $\eta \leq 1$. Except for the electric field peak at $x = 0$, another electric field peak is formed at $x = L_1 + L_p$, as a result of the reverse-biased p-n junction at the interface between Regions II and III. For a higher 2-D coupling ratio, an equivalent p-type region appears and results in a p-n junction within Region III. To form such an np-type Region III, the 2-D coupling ratio ought to reach the condition that $1 < \eta < L_p/(L_1 + L_p) \cdot (N_d - N_{\text{et}})/N_{\text{et}}$. In this case, there are two reverse-biased and one forwardbiased PN junctions in Region III. Namely, two electric field peaks and one valley are formed in Region III. If $\eta > L_p$ / $(L_1 + L_p) \cdot (N_d - N_{et})/N_{et}$, the Region III would be fully taken over by equivalent p-type region due to the high 2-D coupling effect. Therefore, only one electric field peak could appear at the N^+N^- junction.

In the conclusion, the existence of P-top region alters the U-shaped surface electric field that S-RESURF lateral power device has. Furthermore, the effect of P-top region and vertical structure induced coupling results a sophisticated EDC profile, which further leads to an unusual three-peak surface electric field. Using the proposed methodology, it can be clearly demonstrated that the p-type region equivalently decreases the EDC and thus results in a further depletion of the drift region. Namely, the equivalent p-type region may occur in Region II before the full depletion of the drift region. This would further result in an electric valley at the interface of the Regions I and II. Meanwhile, as shown in (7) and Fig. 2, the depletion in Region III is still determined by S-RESURF structure since the P-top region and Region II does not affect the EDC in Region III. Therefore, as shown in Fig. $3(a)$ and (b) , a new electric peak formed at the interface between Regions II and III when a fully depleted Region II attached to the partially depleted Region III. In other words, considering the P-top region, the doping concentration of drift region can be increased accordingly while maintaining the same BV. So far, by using the EDC in D-RESURF lateral power device, the surface electric field profile is qualitatively discussed. However, accurate and simple expressions for the surface electric field are vital to explore the physical insight of the D-RESURF effect and further guide the device structure optimization.

III. SURFACE ELECTRIC FIELD

The breakdown characteristic is determined by the weakest point in the structure that reaches critical electric field at the lowest reversed applied voltage. Specifically speaking, for an SOI lateral power device, the weak points occur both at the surface of the drift region and SOI-BOX layer interface. Nevertheless, the vertical breakdown is usually changes very insignificantly for a specified processing. Therefore, the analysis of surface electric field is essential for the exploring on the breakdown characteristic of the lateral power device. In this paper, we obtain accurate and simple surface electric field expressions by using the EDC into 1-D Poisson's equation.

In a commercial lateral power device, in order to meet the objective of maintaining high breakdown voltages, the drift region is ought to fulfill the full depletion condition. Furthermore, for a fully depleted drift region, the surface electric field profile can be obtained by using (5) and (6) and continuity conditions of surface electric field profile, which yields [4], [5], [13]

$$
E(x) = \begin{cases} E_0 - \frac{qN_d}{\varepsilon_s} \left(x - \eta \frac{x^2}{2L_d} \right) & 0 \le x \le L_1 \\ E_0 + \frac{qN_{\text{et}}}{\varepsilon_s} \left(x - L_1 \right) - \frac{qN_d}{\varepsilon_s} \left(x - \eta \frac{x^2}{2L_d} \right) \\ L_1 \le x \le L_1 + L_p \\ E_0 + \frac{qN_{\text{et}}L_P}{\varepsilon_s} - \frac{qN_d}{\varepsilon_s} \left(x - \eta \frac{x^2}{2L_d} \right) \\ L_1 + L_p \le x \le L_d \end{cases} \tag{8}
$$

where $E_0 = E(0)$ is the surface electric field at the p-n junction. The consistency between the analytical solution and the simulation shows that the 1-D model is valid. As shown in Fig. 4, unlike S-REUSRF device, the D-RESURF has three possible electric peaks on the surface of the drift region. The lateral BV is limited by the weakest point on the surface; therefore, the surface electric field peaks are essential to the lateral BV. From the PN_d junction to the N^+N_d junction, as shown in Fig. 4(a), the first surface electric field peak appears at $x = 0$, the second occurs at $x = L_1 + L_p$ and the last one is at $x = L_d$. As discussed in Section II, such an abnormal electric field is induced by the reversed equivalent p-n junction in Region III. As shown in Fig. $4(b)$ and (c), the increase of Q_{top} leads to a further depletion of the drift region which is consistent with the discussion in Section II. However, a higher *Q*top is not necessary because of meaning a higher BV. As shown in Fig. $4(d)$,

Fig. 4. Analytical and numerical surface electric field profiles of the drift region for various (a) applied voltage ($P_{top} = 1.5 \times 10^{15}$ cm⁻³, $N_d = 1.5 \times 10^{15}$ cm⁻³, and $t_{top} = 1.5 \mu m$), (b) P-top region doping (V_{app} = 200 V, t_{top} = 1.5 μ m, and N_d = 1.5 × 10¹⁵ cm⁻³), (c) P-top region thickness ($V_{\text{app}} = 200 \text{ V}, P_{\text{top}} = 1.5 \times 10^{15} \text{ cm}^{-3}$, and $N_d = 1.5 \times 10^{15} \text{ cm}^{-3}$ 10¹⁵ cm^{−3}), and (d) drift region doping (V_{app} = 200 V, t_{top} = 1.5 μm, $P_{\text{top}} = 1.5 \times 10^{15} \text{ cm}^{-3}$) with $t_{\text{ox}} = 2 \mu \text{m}$, $t_s = 7 \mu \text{m}$, $L_1 = 3 \mu \text{m}$, $L_p = 17 \mu m$, and $L_d = 30 \mu m$.

the overdose of Q_{top} marked in black line results in overdepletion of the drift region and further leads to a high electric field at the N^+N^- junction. In order to obtain a lateral BV as high as possible, it is ideal to make the surface electric field as even as possible. For a D-RESURF lateral power device, the best scenario is to make the three electric field peaks reach the critical electric field (E_C) , simultaneously. By submitting $E(0) = E(L_1 + L_p) = E(L_d) = E_c$ into (8), the structure parameter requirement yields as follows:

$$
\frac{N_{\text{et}}}{N_d} = \frac{L_1 + L_p}{L_1 + L_p + L_d} \cdot \frac{L_d}{L_p}.
$$
 (9)

In such case, the $\eta = 2L_d/(L_d + L_1 + L_p)$ when the surface breakdown occurs. Although the simultaneous breakdowns of three p-n junction at the surface are very tempting, the realization of (9) is not easy while considering the commercial application and process tolerance.

It is worth noting that the proposed method can also be applied to elaborate the partially depleted surface electric field profile. For a partial-depleted drift region, the coupling ratio n can be determined by vertical voltage expression [6], [7]. Then the drift region depletion length *x*lat can be obtained by using $\int E(x)dx = V_{\text{app}}$ and $E(x_{\text{lat}}) = 0$. At last, replace the L_d in (8) with *x*lat. However, considering that the discussion of the partial-depletion case is a lack of meaning in the application of lateral power devices, we will not explore it in this paper.

IV. BREAKDOWN VOLTAGE

BV is one of the most important indexes to the breakdown characteristic of a power device. As the BV is limited by the minimum of lateral and vertical BV, we will discuss these breakdown cases separately.

As discussed earlier, the D-RESURF effect results in various changes to the surface EDC and electric field profile. According to the breakdown conditions, there are three possible cases for the lateral breakdown [1]–[4]. By submitting (8) into 1-D Poisson's equation, the lateral BV can be obtained as

$$
BV_{\text{lat}} = E_0 L_d - \frac{q N_d L_d^2}{2\varepsilon_s} \left(1 - \frac{\eta}{3} \right) + \frac{q N_{\text{et}} L_d \cdot L_P}{\varepsilon_s}.
$$
 (10)

For the PN_d junction breakdown case, $E(0) = E_0 = E_C$. For $P(x)N(x)$ junction breakdown case, $E(L_1 + L_p) = E_c$ and thus E_0 can be given as

$$
E_0 = E_C - \frac{qN_{\text{et}}L_P}{\varepsilon_s} + \frac{qN_d(L_1 + L_P)}{\varepsilon_s} \left[1 - \eta \frac{(L_1 + L_P)}{2L_d}\right].
$$
\n(11)

For the N⁺N breakdown case, $E(L_d) = E_C$ and E_0 can be given as

$$
E_0 = E_C - \frac{qN_{\text{et}}L_P}{\varepsilon_s} + \frac{qN_dL_d}{\varepsilon_s} \left(1 - \frac{\eta}{2}\right). \tag{12}
$$

In this paper, the critical electric field (E_C) is determined by $E_C = 3 \times 10^5 / [1 - 0.33 \log_{10} (N_d / 10^{16})]$ (V/cm) [10]. As for the vertical breakdown case, due to the severe lateral BV deterioration, the vertical breakdown only occurs under the full-depletion condition, thus the vertical BV yields as

$$
BV_{ver} = \frac{qN_d t_s}{\varepsilon_s} \left(K \eta t_{ox} + \frac{2\eta - 1}{2} t_s \right). \tag{13}
$$

As discussed earlier, the BV of the D-RESURF lateral power device is determined by the lowest BV, which yields

$$
BV = Min [BVlat, BVver]. \t(14)
$$

Fig. 5 shows the BV – N_d , BV – t_s , BV – L_d , and $BV - t_{ox}$ characteristics of the D-RESURF lateral power device. As shown in Fig. $5(a)$ and (b), the D-RESURF device successively undergoes N_dN^+ junction full-depletion, vertical breakdown, PN_d junction full depletion, and PN_d junction partial depletion with the increase of N_d and t_s , respectively. As Fig. 5(a) and (b) intuitively show the increase of the P-top region doping concentration makes the drift region full-depletion easier to occur, thus the doping concentration can be increased while maintaining the vertical breakdown. Fig. 5(c) shows the calculated breakdown voltages as a function of the drift region length, along with the MEDICI simulations. Similar to the S-RESURF case, breakdown occurs at the N_dN^+ junction with a very short drift region. Then, when the drift region is long enough, the lateral breakdown occurs hardly. It is can be seen that the constant BV is independent of *Ld* because of the vertical breakdown. Fig. 5(d) shows the influences of t_{ox} on BV. At a very thin buried oxide layer, BV is determined by vertical breakdown. When *t*ox increases to a point in which case the vertical breakdown is higher than the lateral BV, and BV is determined by N_dN^+ junction. Once the breakdown voltage hits its maximum, the BV began to decrease with the increase of *t*ox because the breakdown location moves to PN_d junction. If the buried oxide layer is very thick, the drift region will partially deplete when the breakdown occurs.

Fig. 5. Dependence of BV on (a) drift region doping ($t_{top} = 1.5 \mu m$, $t_s = 7 \mu m$, $t_{ox} = 2 \mu m$, and $L_d = 30 \mu m$), (b) epitaxial layer thickness $(P_{\text{top}} = 1.5 \times 10^{15} \text{ cm}^{-3}, N_d = 1.5 \times 10^{15} \text{ cm}^{-3}, t_{\text{ox}} = 2 \mu \text{m}, \text{and}$ L_d = 30 μ m), (c) drift region length (P_{top} = 1.5 \times 10¹⁵ cm^{−3}, t_s = 7 μ m, t_{top} = 1.5 μ m, and t_{ox} = 2 μ m), and (d) BOX layer thickness (P_{top} = 1.5×10^{15} cm⁻³, $N_d = 1.5 \times 10^{15}$ cm⁻³, $t_{top} = 1.5 \mu$ m, and $t_{ox} = 2 \mu$ m) with $L_1 = 3 \mu m$ and $L_p = 17 \mu m$.

To summarize, the existence of the P-top region results in an enhanced 2-D coupling effect that reduces the EDC in the drift region and thus results in an electric field peak at the interface between Regions II and III. Therefore, the vertical breakdown is more likely to occur which enable the drift region to be doped highly. However, such a complicated surface electric profile results in a sophisticated breakdown characteristic, which increases the design difficulty in optimizing the structure parameters of the D-RESURF lateral power devices.

V. STRUCTURE OPTIMIZATION

In order to obtain a higher doping concentration of drift region while maintaining a high BV, it is vital to optimize the structure parameters of lateral power devices during the design phase. Especially for D-RESURF lateral power devices, the abnormal electric field peak at the interface between Regions II and III leads to a higher degree of optimization complexity. Meanwhile, the conventional S-RESURF is clearly no longer applicable for D-RESURF.

First of all, we propose a D-RESURF optimization criterion to provide a theoretical window for optimizing the drift region doping dose ($Q = N_d \times t_s$). Similar to conventional S-RESURF case, the limits of the optimized doping dose (ODD) are determined by vertical and lateral BVs [6], [7], [15]. As shown in Fig. $5(a)$ and (b), the upper limit of ODD (Q_{up}) is determined by the vertical and PN_d junction breakdown voltages. Meanwhile, the lower limit (Q_{down}) is governed by the vertical breakdown and N^+N_d junction breakdown. Thus, the optimized doping window of drift region

Fig. 6. Drift region doping dose as a function of (a) P-top region doping concentration (L_d = 30 μ m) and (b). drift region length (P_{top} = 1.5 \times 10¹⁵ cm^{−3}) with $t_s = 7 \mu m$, $t_{top} = 1.0 \mu m$, $t_{ox} = 2 \mu m$, $L_1 = 3 \mu m$, and $L_2 = 3 \ \mu m$.

can be obtained by substituting (13) into (10)

$$
Q_{\rm up} = \frac{\varepsilon_s E_C}{q} \left[\frac{6\alpha^2 - 18\alpha\beta + 6\alpha - 1}{3(\alpha^2 - 1)} \right] + 2N_{\rm et}L_P \frac{\alpha}{(1 - \alpha^2)}\tag{15}
$$

$$
Q_{\text{down}} = \frac{\varepsilon_s E_C}{q} \left[\frac{6\alpha^2 - 18\alpha\beta + 6\alpha + 2}{3(\alpha^2 + 1)} \right] \tag{16}
$$

where $\alpha = t_s/L_d$ and $\beta = t_{ox}/L_d$. For the simplicity, the E_C used in (15) and (16) is $E_C = 3 \times 10^5$ (V/cm). Similar to the S-RESURF case, α and β are the shape factors of SOI layer and buried oxide layer, respectively. Hereby, the structure optimization criterion can be given as

$$
Q_{\text{down}} \le Q \le Q_{\text{up}}.\tag{17}
$$

Meanwhile, the upper and lower limits of the S-RESURF criterion are given in [7] as

$$
Q_{\text{S-up}} = \frac{\varepsilon_s E_C}{q} \left[\frac{6\alpha^2 - 18\alpha\beta + 6\alpha - 1}{3(\alpha^2 - 1)} \right] \tag{18}
$$

$$
Q_{\text{S-down}} = \frac{\varepsilon_s E_C}{q} \left[\frac{6\alpha^2 - 18\alpha\beta + 6\alpha + 2}{3(\alpha^2 + 1)} \right].
$$
 (19)

It is worth noting that for the upper limit of ODD, the only difference between D-RESURF and S-RESURF cases is the $2N_{\text{et}}L_p\alpha/(\alpha^2-1)$. Meanwhile, the lower limit of ODD is the exact same as that in S-RESURF case. This explains the reason why the D-RESURF only affect the lateral PN*d* junction breakdown while having no influence on N_dN^+ junction [7].

For a D-RESURF lateral power device, the existence of P-top region improves the drift region process tolerance $(Q = Q_{\text{up}} - Q_{\text{down}})$. More importantly, due to the depletionenhancing effect of the P-top region, the drift region doping dose required for lateral PN*d* breakdown is increased significantly. Namely, it is possible for the D-RESURF device to have a higher doping concentration in drift region to reduce R_{ON} while maintaining a high BV compared with an S-RESURF LDMOS. In practice, for a specific process, the t_s and t_{ox} are normally fixed. Therefore, as (15) indicates, the designing optimization should be a focus on drift region doping concentration, drift region length, P-top region doping dose, and P-top region length. As shown in Fig. $6(a)$, when P-top region is n-type doped and $|P_{top}| = |N_d|$, the D-RESURF lateral power device at point A degenerates to a S-RESURF device, thus $Q_{\text{up}} = Q_{S-\text{up}}$. With the increase

of P-top region doping concentration, the depletion-enhancing effect induced by P-top region becomes more and more obvious and results in the linear growth of *Q*up. Furthermore, when P-top region is p-type doped and $|P_{top}|=|N_d|$, the ΔQ of the D-RESURF device at point B is about two times the ΔQ in S-RESURF case. Fig. 6(b) demonstrates the influence of *Ld* on ODD. It can be seen that the D-RESURF effect significantly improves the window of optimized drift region doping dose.

VI. CONCLUSION

In order to elaborate the physical meaning of the D-RESURF technique, we proposed the D-RESURF EDC theory. Using the EDC theory, a complicated 2-D drift region can be equivalent to the 1-D planar junction with EDC at the same time considering its breakdown characteristic. In this case, due to the influence of the P-top region, the equivalent 1-D junction can act as an NP, NPN, or NPNP structure, which explains the distinctive three electric field peaks in the drift region. The proposed EDC theory provides an effective way to reveal the influence of D-RESURF effect on the performance of SOI LDMOS. Based on the proposed theory, a novel 1-D analytical model is presented to qualitatively and quantitatively explore the sensitivity of the surface electric field and breakdown mechanism of the D-RESURF LDMOS for the first time. The proposed optimization criterion provides a simple and effective tool for optimizing the structure parameters of D-RESURF SOI lateral power devices. The analytical solutions are found out to be consistent with the simulation results obtained from MEDICI, a commercial TCAD tool.

REFERENCES

- [1] Y. F. Guo, J. F. Yao, B. Zhang, H. Lin, and C. C. Zhang, "Variation of lateral width technique in SoI high-voltage lateral double-diffused metal– oxide–semiconductor transistors using high-*k* dielectric," *IEEE Electron Devices Letter*, vol. 36, no. 3, pp. 262–264, Mar. 2015, doi: [10.1109/](http://dx.doi.org/10.1109/LED.2015.2393913) [LED.2015.2393913.](http://dx.doi.org/10.1109/LED.2015.2393913)
- [2] X. Luo *et al.*, "Ultralow ON-resistance high-voltage p-channel LDMOS with an accumulation-effect extended gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2614–2619, Jun. 2016, doi: [10.1109/TED.](http://dx.doi.org/10.1109/TED.2016.2555327) [2016.2555327.](http://dx.doi.org/10.1109/TED.2016.2555327)
- [3] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction power devices, history, development, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 720–734, Mar. 2017, doi: [10.1109/TED.](http://dx.doi.org/10.1109/TED.2017.2658344) [2017.2658344.](http://dx.doi.org/10.1109/TED.2017.2658344)
- [4] S. Gao, J. Chen, D. Ke, and L. Liu, "Analytical model for surface electrical field of double RESURF LDMOS with field plate," in *Proc. 8th Int. Conf. Solid-State Integr. Circuit Technol.*, Shanghai, China, Oct. 2006, pp. 1324–1326, doi: [10.1109/ICSICT.2006.306149](http://dx.doi.org/10.1109/ICSICT.2006.306149).
- [5] Q. Li and Z. Li, "A new analytical model for the surface electrical field distribution of double RESURF LDMOS," in *Proc. CES/IEEE 5th Int. Power Electron. Motion Control Conf.*, Shanghai, China, Aug. 2006, pp. 1–4, doi: [10.1109/IPEMC.2006.4777951.](http://dx.doi.org/10.1109/IPEMC.2006.4777951)
- [6] J. Zhang *et al.*, "A new physical insight of RESURF effects based on gradual charge appointment concept for bulk silicon lateral power devices," *Superlattices Microstruct.*, vol. 96, pp. 111–123, 2016, doi: [10.1016/j.spmi.2016.02.011.](http://dx.doi.org/10.1016/j.spmi.2016.02.011)
- [7] Z. Jun *et al.*, "One-dimensional breakdown voltage model of SOI RESURF lateral power device based on lateral linearly graded approximation," *Chin. Phys. B*, vol. 24, no. 2, p. 028502, 2015, doi: [10.1088/1674-1056/24/2/028502.](http://dx.doi.org/10.1088/1674-1056/24/2/028502)
- [8] J. Wei *et al.*, "High-voltage thin-SOI LDMOS with ultralow ONresistance and even temperature characteristic," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1637–1643, Apr. 2016, doi: [10.1109/](http://dx.doi.org/10.1109/TED.2016.2533022) [TED.2016.2533022](http://dx.doi.org/10.1109/TED.2016.2533022).
- [9] I. Cortés, G. Toulon, F. Morancho, E. Hugonnard-Bruyere, B. Villard, and W. J. Toren, "Analysis and optimization of lateral thin-film Siliconon-insulator (SOI) MOSFET transistors," *Microelectron. Rel.*, vol. 52, no. 3, pp. 503–508, 2012, doi: [10.1016/j.microrel.2011.12.011.](http://dx.doi.org/10.1016/j.microrel.2011.12.011)
- [10] M. Imam, M. Quddus, J. Adams, and Z. Hossain, "Efficacy of charge sharing in reshaping the surface electric field in high-voltage lateral RESURF devices," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 141–148, Jan. 2004, doi: [10.1109/TED.2003.821383](http://dx.doi.org/10.1109/TED.2003.821383).
- [11] S.-K. Chung and S.-Y. Han, "Analytical model for the surface field distribution of SOI RESURF devices," *IEEE Trans. Electron Devices*, vol. 45, no. 6, pp. 1374–1376, Jun. 1998, doi: [10.1109/16.678582](http://dx.doi.org/10.1109/16.678582).
- [12] J. A. Appels and H. M. J. Vaes, "High voltage thin layer devices (RESURF devices)," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 1979, pp. 238–241, doi: [10.1109/IEDM.1979.189589](http://dx.doi.org/10.1109/IEDM.1979.189589).
- [13] Z. Li, Y. Guo, B. Zhang, J. Fang, and Z. Li, "A new 2D analytical model of double RESURF in SOI high voltage devices," in *Proc. 7th Int. Conf. Solid-State Integr. Circuits Technol.*, vol. 1, pp. 328–331 2004, doi: [10.1109/ICSICT.2004.1435019.](http://dx.doi.org/10.1109/ICSICT.2004.1435019)
- [14] W. Yang, X. Cheng, Y. Yu, Z. Song, and D. Shen, "A novel analytical model for the breakdown voltage of thin-film SOI power MOSFETs," *Solid-State Electron.*, vol. 49, no. 1, pp. 43–48, 2005, doi: [10.1016/j.sse.2004.07.004](http://dx.doi.org/10.1016/j.sse.2004.07.004).
- [15] J. Zhang, Y.-F. Guo, D. Z. Pan, and K.-M. Yang, "A novel 3-D analytical method for curvature effect-induced electric field crowding in SOI lateral power device," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4359–4365, Nov. 2016, doi: [10.1109/TED.2016.2609908.](http://dx.doi.org/10.1109/TED.2016.2609908)
- [16] Y. Guo, Z. Li, and B. Zhang, "A new analytical model for optimizing SOI LDMOS with step doped drift region," *Microelectron. J.*, vol. 37, no. 9, pp. 861–866, 2006, doi: [10.1016/j.mejo.2006.03.004.](http://dx.doi.org/10.1016/j.mejo.2006.03.004)

Jun Zhang (S'17) received the B.S. degree in microelectronics from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2013, where he is currently pursuing the Ph.D. degree in microelectronics and solid-state electronics under the supervision of Prof. Y. Guo.

David Z. Pan (S'97–M'00–SM'06–F'14) is currently the Engineering Foundation Professor with The University of Texas at Austin, Austin, TX, USA.

Dr. Pan has served as a Senior Associate Editor for the *ACM Transactions on Design Automation of Electronic Systems*, and an associate editor for a number of other journals.

Ke-Meng Yang received the B.S. degree from the Nanjing University of Posts and Telecommunications, Nanjing, China, in 2014, where she is currently pursuing the Ph.D. degree with the College of Electronic and Optical Engineering.

Xiao-Juan Lian received the B.S. and M.S. degrees from Xidian University, Xi'an, China, in 2008 and 2011, respectively, and the Ph.D. degree from the Universidad Autònoma de Barcelona, Bellaterra, Spain, in 2014. She has been a Post-Doctoral Researcher with Nanjing University for about three years.

Yu-Feng Guo (M'05) received the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China, Chengdu, in 2005.

He is currently the Dean of the College of Electronic and Optical Engineering and the Vice-Director of the National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, Nanjing University of Posts and Telecommunications, Nanjing, China.

Jia-Fei Yao received the B.S. degree in microelectronics from the Nanjing University of Posts and Telecommunications, China, in 2010, and the joint Ph.D. degree in micro-electronics from the Nanjing University of Posts and Telecommunications and the University of Vermont, Burlington, VT, USA, in 2016

He has been supported by the China Scholarship Council for his joint Ph.D. degree in 2015.