Investigations of Asymmetric Spacer Tunnel Layer Diodes for High-Frequency Applications

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***Abstract*— A complete description of physical models for fabricated asymmetric spacer tunnel layer (ASPAT) diodes is reported in this paper. A novel $In_{0.53}Ga_{0.47}As$/AlAs design is presented and compared to the conventional GaAs/AlAs material system. For both material schemes, physical models were developed based on experimental measurements. Simulated dc characteristics of the devices are given for both planar- and back-contacted structures to highlight the impact of spreading resistance on device behavior. Furthermore, full S-parameter derivations from numerical simulation for tunnel diodes are demonstrated for the first time on the basis of quantum-mechanical ac modeling of the capacitance–voltage and conductance–voltage performances of these ASPAT diodes. A negligibly small difference between measured and simulated zero-biased intrinsic capacitances is observed (i.e., $\leq$ 0.2 fF). These are beneficial for accurate predictive models for device characteristics. In addition, key parameters which can be extracted from simulation results are obtained to aid in the development of millimeter-wave/terahertz applications of these types of heterostructure tunnel devices.**

***Index Terms*— Asymmetric spacer tunnel layer (ASPAT) tunneling device, dc and RF characterization, physical modeling.**

I. Introduction

TUNNELING is a quantum mechanical phenomenon which allows carriers with low energy to have a probability of passing through a larger energy barrier [1]–[3]. The asymmetric spacer tunnel layer (ASPAT) employs this phenomenon as its major carrier transport mechanism. The first attempt at demonstrating the ASPAT diode was made by Syme *et al.* [2]. Their device consisted of a thin AlAs barrier layer [ten monolayers (MLs)] sandwiched between two asymmetrical GaAs spacer layer thicknesses with a ratio of 40:1. The asymmetric design of the epitaxial spacer layers leads to asymmetric IV characteristics.

To date the majority of semiconductor microwave devices use three-terminal transistor structures. Even though these devices exhibit excellent performances at millimeter-wave/terahertz frequencies, there are limitations because of complexity in fabrication and lithography processes [4]–[6]. Thus, two-terminal devices are exploited as alternative elements in very high-frequency applications due to their much simpler fabrication process and relaxed lithography requirements (micrometer scale features rather than nanometre scale features for three-terminal devices). Additionally, quantum tunneling-based diodes show superior temperature stability [7], [8] as their characteristics are not limited by kT compared to thermionic emission of low-barrier Schottky diode. Such a limitation in low-barrier Schottky diode is attributed to the dependence of its curvature coefficient on temperature, $k_v < q/kT$ [9], [10]. The latter fact is a key parameter for detector performance as it directly impacts the sensitivity where high coefficient translates into high detector sensitivity. In contrast to the backward diode [11], the leakage current of the ASPAT diodes is significantly lower. This may improve the detector quality as the negative cycle of the input power applied to the detector will be removed by the reverse bias of the IV characteristic. Hence this key feature aids significantly in improving ASPAT diodes without sacrificing their sensitivity or dynamic range. As an emerging device, the ASPAT can, therefore, be treated as a promising candidate for key component in the future millimeter-wave/terahertz detector circuits [2], [12], [13].

Efforts have been made to simulate the ASPAT diode using numerical models developed by Syme *et al.* [2], [14]. However, the reported dc models [2], [15] were not accurate enough since substantial mismatches occurred with measured I–V results. In addition, these models were based on a back-contact structure device (contacts are located on the top and bottom of the epilayers) compared to the planar design

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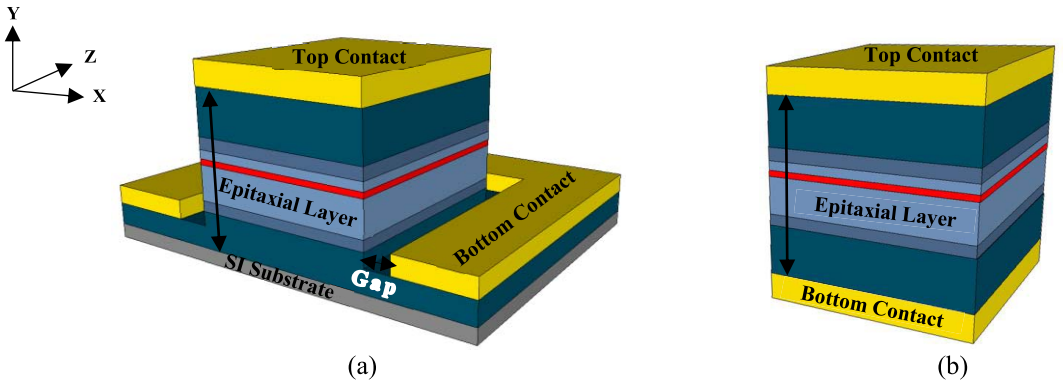

Fig. 1. 3-D structure of ASPAT diodes including contacts and semi-insulating substrates. (a) Planar structure. (b) Back-contacted structure.

presented here (see Fig. 1). Furthermore, as the promising application for the ASPAT diode is in millimeter-wave/sub-millimeter-wave detection [12], [16], ac models for this type of device are required for accurate predictive modeling. Physical modeling becomes essential as it is a highly efficient method of device development. Internal device variables which cannot be found directly from I–V or RF measurements such as the two-dimensional electron gas density, energy band diagrams, and electric fields can be readily achieved via physical device simulation.

In this paper, accurate models for the ASPAT diode for both dc and ac analyses are developed. The first planar structure model of the ASPAT diode simulation is provided which aids in device modeling since it includes the effects of spreading resistance, R_{Spr}. The model and material descriptions for both conventional GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes are detailed following their structure definitions. The simulation is verified by adjusting the mesa size and comparing it to measured data for dc analysis. The ac simulation is obtained by optimizing the component values to match measured S-parameters of the device. The capacitance, conductance, and S-parameters of the intrinsic ASPAT diode are successfully simulated and then compared with RF measurements of fabricated devices.

II. Device Structures and Fabrication

The ASPAT structures in this paper were grown in-house in a Riber V100HU solid-source molecular beam epitaxy system. The main active epitaxial layers of the ASPAT diode contain a thin AlAs barrier, sandwiched between two intrinsic spacer layers with asymmetric thicknesses. Besides these, heavily doped ohmic contact layers, lightly doped layers for emitting, and collecting carriers are also grown on both sides of the main active layers.

The two designs of the ASPAT diodes investigated in this paper comprise a conventional GaAs-AlAs ASPAT and a new $In_{0.53}Ga_{0.47}As$-AlAs ASPAT. The AlAs barrier is designed to be thin enough to ensure a gamma to gamma direct tunnelling in contrast to the normal bulk indirect bandgap AlAs carrier transport. The implementation of direct tunneling influences the device characteristic and makes it temperature insensitive [7], [8].

The thicknesses of the main active layers for both samples are designed to be identical, both incorporating a thin AlAs barrier of thickness 28.3 Å (equivalent to ten MLs). Two spacers are located outside the AlAs barrier with thicknesses of 5 and 200 nm, respectively. This 1:40 spacer ratio was maintained for both GaAs and $In_{0.53}Ga_{0.47}As$ designs. The emitter and collector layer sandwich the main active layers and have a doping concentration of 1×1^{17} cm^{-3}. The doping concentration of the ohmic layers is 4×10^{18} cm^{-3} for GaAs and 1.5×10^{19} cm^{-3} for $In_{0.53}Ga_{0.47}As$ to further decrease the contact resistances.

Both samples were fabricated using standard i-line photolithography. The GaAs/AlAs ASPAT used polyimide for passivation, while the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT used an air-bridge technique. These fabrication processes are different due to the difference in undercut etch-profiles for the two material systems, with the air-bridge technique causing excessive undercut in the GaAs/AlAs epitaxial structure and thus was not suitable (or had very low yields). The contact metal scheme deployed for GaAs/AlAs ASPAT diodes is AuGe/Ni/Au while $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes use nonalloyed Pd/Ti/Pd/Au instead. Both ASPAT diodes use Ti/Au metal scheme as their ground-signal-ground (GSG) coplanar waveguide (CPW) for both dc and ac characterisations.

For both ASPAT designs, diodes with different emitter sizes were fabricated and measured on the same wafer. This paper will focus mainly on fabricated devices with mesa area of 10×10 μm^2, 6×6 μm^2, and 4×4 μm^2. Fig. 1 illustrates the 3-D schematic of the fabricated diodes, including device terminals, and substrate while the epitaxial layer profiles of the ASPAT sample are shown in Table I.

III. Physical Modeling

Physical modeling for the ASPAT diode commences with defining the multilayer structure listed in Table I. The Silvaco simulator used is capable of modeling and simulating different semiconductor structures with various materials properties. By using the DeckBuild feature provided by Silvaco [17], a 2-D device simulation was performed to determine the dc and RF characteristics. All simulations in this paper were performed at room temperature (300 K).

TABLE I
EPITAXIAL LAYERS FOR ASPAT SAMPLES. EPITAXIAL LAYER STRUCTURES FOR ASPAT DIODES WITH DOPING AND LAYER THICKNESS PROFILES. (a) GaAs/AlAs ASPAT. (b) $In_{0.53}Ga_{0.47}As$/AlAs ASPAT

	GaAs 4.0 × 10^{18} cm^{-3}
	GaAs 1.0 × 10^{17} cm^{-3}
5 nm	GaAs
2.83 nm	AlAs
200 nm	GaAs
	GaAs 1.0 × 10^{17} cm^{-3}
	GaAs 4.0 × 10^{18} cm^{-3}
	GaAs (SI)

(a)

	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}
	$In_{0.53}Ga_{0.47}As$ 1.0×10^{17} cm^{-3}
5 nm	$In_{0.53}Ga_{0.47}As$
2.83 nm	AlAs
200 nm	$In_{0.53}Ga_{0.47}As$
	$In_{0.53}Ga_{0.47}As$ 1.0×10^{17} cm^{-3}
	$In_{0.53}Ga_{0.47}As$ 1.5×10^{19} cm^{-3}
	InP (SI)

(b)

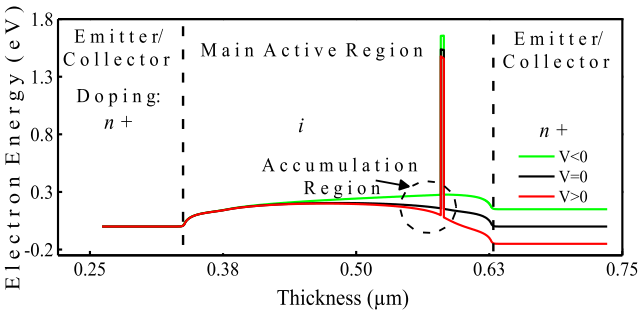

Fig. 2. Silvaco simulated schematic conduction band profile of ASPAT diodes under bias [1].

A. Model Definition

The conduction band profile shown in Fig. 2 depicts the band bending behavior under bias conditions for both devices. The band bending (green line in Fig. 2) occurs when a forward bias is applied to the device and the potential barrier decreases. On the other hand, the opposite trend is seen when applying a reverse bias. Compared with the unbiased device, the potential barrier increases. As shown in Fig. 2, the ASPAT device is segmented into three distinct regions, main active region, emitter region, and collector region. The emitter and collector regions depend on the biasing condition.

The collector and emitter regions are under quasi-equilibrium, and the main active region with the barrier structure is treated to be in nonequilibrium using the semiconductor–insulator–semiconductor (SIS) model solver. The solver calculates the 1-D tunneling current between the two spacers which are separated by the AlAs barrier. It is assumed that the charge (carriers) passes through both sides of the barrier interfaces.

In the main active region, the location of the barrier structure must be identified to help specify the quantum tunneling area to assists the simulator into injecting the tunneling current at the exact position of the barrier interface. By coupling special rectangular and regular meshes, the output generated current [17] is presented in terms of per unit width (where the width dimension is denoted as x-direction in Fig. 1).

The tunneling current calculated in the simulation is evaluated for all energies at which the tunneling is possible by employing the 1-D Schrodinger equation. This equation is formulated in the effective mass approximation and determines the transmission coefficient of a carrier through the tunneling barrier structure [2], [14]. The transmission coefficient is a function of energy, and it depends on the barrier characteristics such as electron effective mass, thickness, and height. The probability that an electron with energy E tunnels through the barrier was evaluated using a transfer matrix method (TMM) to solve the Schrodinger equation [17]. TMM [18]–[20] solves the equation by discretized the device band profile and computes a transfer matrix that consists of the potential energy and effective mass.

The Silvaco SIS model calculates the current density through the barrier by using the following expression:

$$J = \frac{qm^*\mathrm{kT}}{2\pi^2\hbar^3}\int_0^\infty T(E)\ln\left\{\frac{1+e^{\left[\frac{(E_{\mathrm{Fr}}-E)}{\mathrm{kT}}\right]}}{1+e^{\left[\frac{(E_{\mathrm{Fl}}-E)}{\mathrm{kT}}\right]}}\right\}dE \quad (1)$$

where m, q, k, and h are the electron effective mass, the electron charge, Boltzmann's constant, and Plank constant, respectively, while E_{Fr} and E_{Fl} are the quasi-fermi levels on the right and left side of the barrier.

For the back-contacted structure, the dc analysis can be solved using (1). However, for on wafer and high-frequency measurements, the planar device shows noticeable advantages compared with the back-contacted device. For the planar device, the diode contacts in the simulation were designed to be planar instead of parallel. This, however, induces a R_{Spr} in the bottom ohmic layer [21], [22]. The R_{Spr} can be calculated using

$$R_{\mathrm{Spr}} = \frac{1}{\pi\sigma d}\ln\left(\frac{a}{a+d_{\mathrm{Gap}}}\right) \quad (2)$$

where σ is the conductivity of the material, d is the residual bottom ohmic layer thickness after etching, and the d_{Gap} is the distance between the contacts. By solving (1) and (2), the I–V characteristics of the planar device can be obtained.

B. Material Definition

The key parameters of the GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT are listed in Table II [23]–[25]. E_g (300), electron affinity, m_e^*, and $m_{e,t}$ represent the material bandgap at 300 K, electron affinity, electron conduction band effective mass, and tunneling effective mass, respectively.

Normally, thick (or bulk) AlAs has an indirect bandgap of 2.16 eV. Due to the thin ten ML AlAs barrier thickness,

TABLE II
MATERIAL SPECIFICATION DEFINITION IN ATLAS SIMULATOR

Material	AlAs	GaAs	$In_{0.53}Ga_{0.47}As$
E_g (300), eV	2.83	1.42	0.74
m_e^*	0.268	0.067	0.040
$m_{e,t}$	0.06	-	-
Electron Affinity, eV	3.01	4.07	4.51
Dielectric Permittivity	10	12.9	13.9

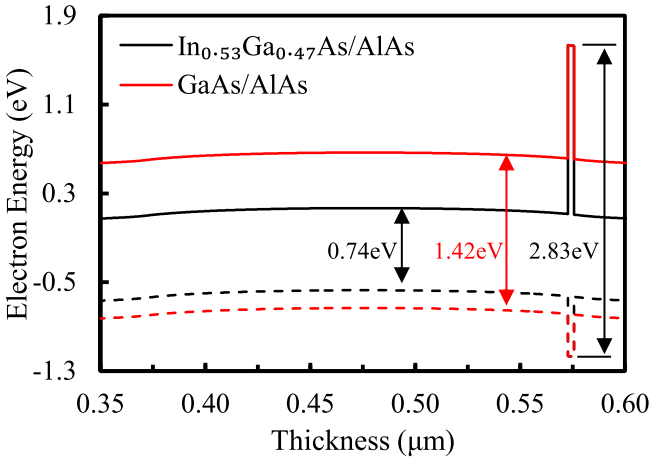

Fig. 3. Comparison of band profiles between GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT. Inset: barrier height (AlAs) difference between GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes.

near the middle of the Γ-Γ direct tunneling with a bandgap of 2.83 eV is significant, and the Γ-X current makes only a minor contribution, and so is neglected in the physical model. Additionally, the AlAs tunnelling effective mass ($m_{e,t}$), Γ-valley effective mass is low as the Γ curvature is much steeper compared to the X-valley.

The electron effective mass, m^* is determined by taking the curvature of the band into account for a given (E, k) relationship and given by $m^* = \hbar^2/(d^2E/dk^2)$ [26]. Compared to the binary material GaAs, the material definition for InGaAs uses the dependence of Ga composition fraction x in $In_{1-x}Ga_xAs$. The bandgap energy of this ternary alloy can be derived as $E_{\mathrm{InGaAs}}(x) = E_{\mathrm{InAs}} + [E_{\mathrm{GaAs}} - E_{\mathrm{InAs}}]x + Ax(1-x)$ where A is a bowing parameter with a value of 0.475 and x is the composition of $In_{1-x}Ga_xAs$ which equals 0.47 in this paper. The effective mass for InGaAs [27] can be written as $m_{\mathrm{InGaAs}} = m_{\mathrm{InAs}}x + m_{\mathrm{GaAs}}(1-x) + Cx(1-x)$, where C is the bowing parameter. The reported range of the effective mass ratio is 0.038–0.044. Moreover, the electron affinity is used for evaluating the band discontinuities at the semiconductor heterointerfaces [28].

The conduction band diagrams for both main active layers of the two ASPAT designs are illustrated in Fig. 3. The barrier height for $In_{0.53}Ga_{0.47}As$/AlAs is ∼1.5 eV while in the case of GaAs/AlAs it is ∼1 eV as depicted in Fig 4. The barrier height for $In_{0.53}Ga_{0.47}As$/AlAs is ∼1.5 eV while in the case of GaAs/AlAs it is ∼1 eV. Even though the major carrier transport is due to tunneling in the GaAs/AlAs ASPAT, the 0.5 eV higher AlAs barrier in the $In_{0.53}Ga_{0.47}As$/AlAs

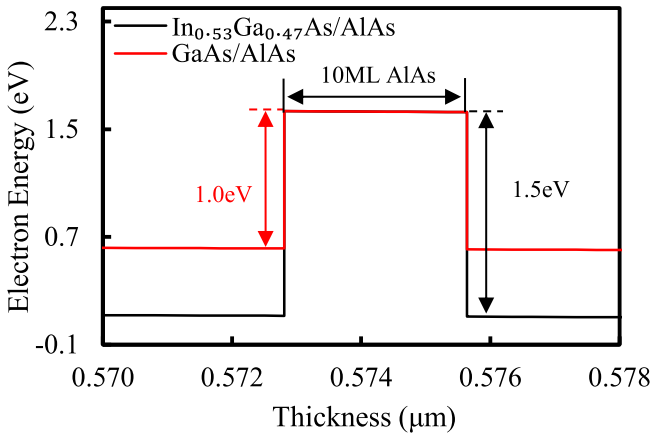

Fig. 4. Conduction band discontinuities between GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes.

ASPAT further suppresses and limits any thermionic emission. Hence the main transport mechanism for the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT is electron tunneling through the barrier from the $In_{0.53}Ga_{0.47}As$ spacer formed immediately adjacent to it.

There might be impacts due to the relatively large lattice mismatch between AlAs and InP. However, the ten ML AlAs barrier thickness is below the critical thickness for relaxation, and this is further evidenced by stable IV characteristics (over > two years) and which are very sensitive to any defects that might be present, especially in terms of leakage currents.

IV. RESULTS AND DISCUSSION

The 2-D physical models for both ASPAT diodes were used to reproduce the dc and RF characteristics. This robust program is used to analyze device performance which provides a simple extraction module for dc characteristic and S-parameters data. These were then compared with room temperature measured data.

A. DC Characteristics

Detailed examination of both structures shows that the asymmetry of the spacer thicknesses leads to an asymmetry in the current–voltage characteristics. The dc characteristics of the ASPAT diodes were measured using a semiconductor parameter analyzer (Agilent B1500). All dc measurements in this paper were taken at room temperature with a bias range from −1.5 to 1.5 V. The simulation results for a 4×4 μm^2 mesa area GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs devices with their respective back-contact and planar contacts structures are shown in Fig. 5.

The differences between simulated back-contacted and planar-contacted devices are depicted in Fig. 5. The total resistance of the ASPAT diode is the sum of all contact resistances, R_{Spr}, and the resistance of various epilayers. With the help of high doping of the ohmic layers, the contact resistance only contributes a small portion of the total resistance. Similarly, the resistance of the epilayers is only counted for the main active layers. Thus, it can be seen that R_{Spr} accounts for most of the total resistance under high bias.

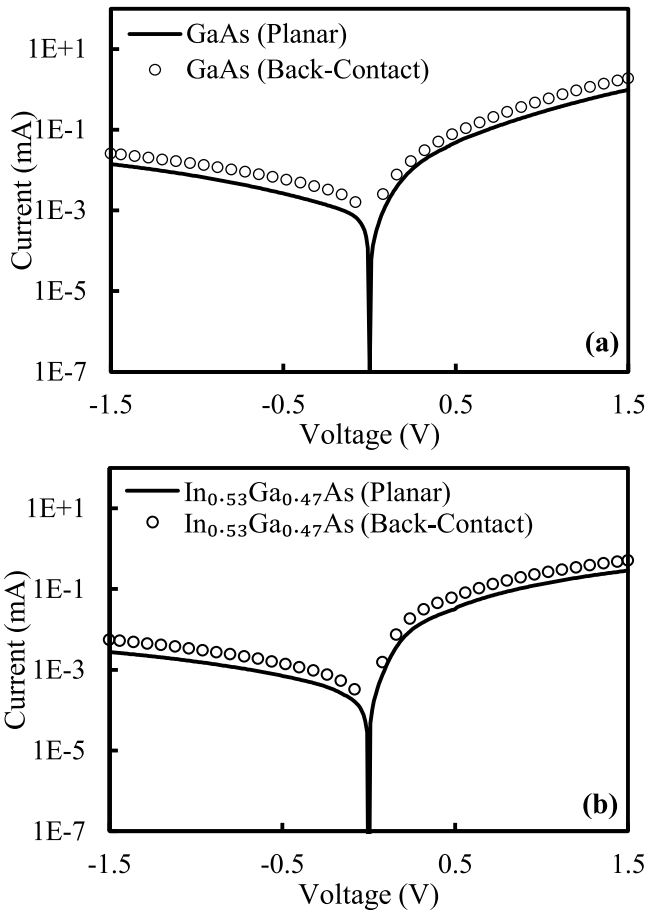

Fig. 5. Log (I)–V characteristic differences between back-contacted and planar-contacted dc simulations for (a) GaAs/AlAs and (b) $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes ($4 \times 4\ \mu m^2$).

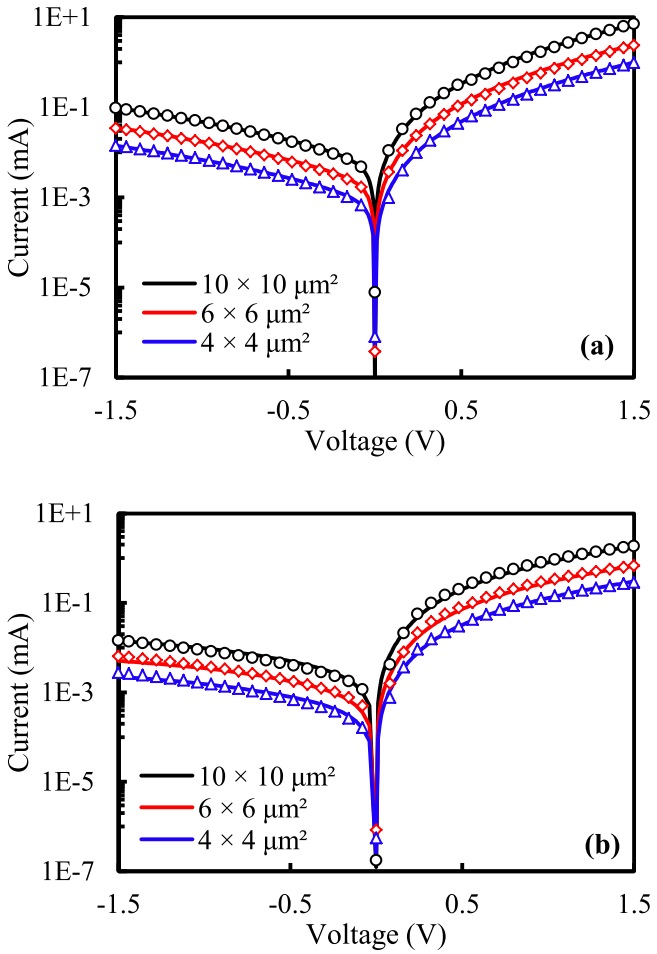

Fig. 6. Log (I)–V characteristics of ASPAT diodes for various mesa area for (a) GaAs/AlAs and (b) $In_{0.53}Ga_{0.47}As$/AlAs (planar structure). Blue, red, and black indicate simulated (symbols) and measured (solid lines) data for $10 \times 10\ \mu m^2$, $6 \times 6\ \mu m^2$, and $4 \times 4\ \mu m^2$ mesa areas, respectively.

In the structural definition of the simulation, the gap between the planar ohmic contacts (denoted as gap in Fig. 1) was designed to be 2 μm which was kept the same as in the fabricated devices. For bias below 1 V, the difference between the planar and back-contacted devices is ~44%. Minimizing the separation between contacts for the planar device minimizes R_{Spr}, and therefore leads to a corresponding increase in current.

The simulated and measured planar diodes I–V characterizes of both ASPAT material systems are shown in Fig. 6 using different mesa dimensions. The base model used was validated through the excellent fits with the measured data. Near zero bias, the reproduced characteristics of devices predict a smaller value compared to measured diodes, which was mainly due to the noise limitation of the semiconductor analyser setup.

Under forward bias, some of the voltage is dropped in the thick intrinsic spacer region and electron accumulation forms in the small triangular well, the electrons can then tunnel through the potential barrier. Under reverse bias, most of the voltage is dropped across the same region and causes only small amounts of electrons to reach the barrier. This phenomenon leads to a very slow rise in the reverse current with bias and is the reason for the asymmetric I–V characteristic between forward and reverse bias [13].

As can be shown in Fig. 6, the simulated data matches perfectly with the measured data for all device sizes for both GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPATs.

B. RF Characterization

Since the developed model can be used for all device sizes, the RF characterization will focus only on the smallest fabricated size ($4 \times 4\ \mu m^2$). For high-frequency applications, the performance of ASPAT diode can be predicted through RF simulation and thus, this becomes a useful tool for extracting key parameters for circuit application design purposes. In this section, the ac modeling steps for the ASPAT diode include parasitics and diode parameters extracted from measurements, parameters extracted from simulation followed by comparisons and analysis.

The RF characterizes of the ASPAT diodes were measured at room temperature using an Anritsu VNA, and the S-parameters were measured on-wafer under different bias conditions from 40 MHz to 40 GHz. As the diodes were designed to use GSG patterns, de-embedding techniques were used to extract accurate values of the extrinsic parameters. The extrinsic parameters are associated with the additional transmission lines and other parasitic elements.

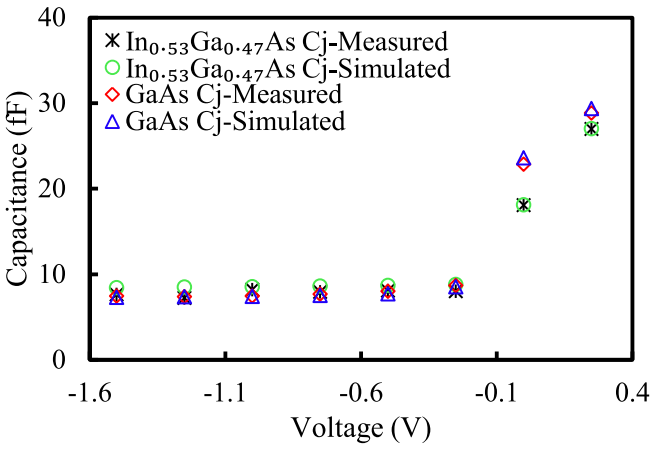

Fig. 7. Simulated and measured capacitances for GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes (4×4 μm^2).

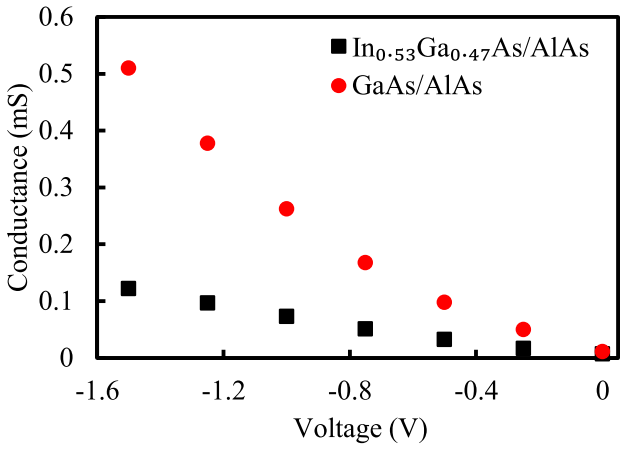

Fig. 8. Simulated conductance for GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diode (4×4 μm^2).

From the equivalent circuits of the open, short, and GSG-patterned devices, the parasitic capacitance, inductance, and the diode with parasitic elements can be extracted, respectively. Based on the two-step de-embedding technique reported in [29] and [30], the pad capacitance (C_{pad}), inductance (L_{pad}), and the junction capacitance (C_j) of the diode can all be extracted accurately from the measured S-parameters.

De-embedding the open equivalent circuit, the pad capacitance, C_{pad} can be extracted from the measurements of the open mode. This provides 15 and 10 fF for the GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes, respectively, depending on the CPW structure. Using the same method, the self-inductance of the signal line, which should be the same for both ASPAT diodes, yields an extracted inductance value of 50 pH with a negligible 2-pH fluctuation over different runs.

The measured capacitance is the total capacitance (C_{total}) summed up with pad capacitance and the junction capacitance of the diode. Thus, the later intrinsic element can be obtained from the measured CV characteristics after excluding the additional pad capacitance, $C_j = C_{total} - C_{Pad}$. Theoretically, this is calculated from the material permittivity, device size, and width of the depletion region. The minimum capacitance of the diode is normally obtained when the diode is fully depleted with the width of the depletion region being equal to the main active region thickness. Thus, the theoretical fully depleted capacitances are 8.8 and 9.5 fF for GaAs/AlAs ASPAT and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT, respectively.

The ac simulation can provide the intrinsic diode junction capacitance, conductance, and S-parameters. The modeling of ASPAT uses the small signal analysis method where linear and nonlinear elements are connected in an organized and established topology. In this paper, the simulated frequency was fixed in the range from 40 MHz to 40 GHz.

Fig. 7 shows the graphs the capacitance versus voltage and comparisons of the diode capacitance extracted from measurements and ac simulations. The total capacitance was measured from S-parameters, and the diode capacitance $C_{j-measured}$ is the difference between C_{total} and C_{pad}.

Through this comparison, the measured and simulated C_j show excellent agreement including the fully depleted capacitances. From Fig. 7, it can also be seen that both ASPAT diodes become fully depleted at a reverse bias of ~ -0.25 V.

Under zero bias, C_j of these devices show a noticeable difference. This is because the depletion width of the diode is proportional to the band discontinuity.

The diode conductance is an important parameter and is directly proportional to the leakage current under reverse bias. It is the key parameter when designing antiparallel diode mixers. This is because the negative cycle of the RF input power applied to the detector will be removed by the reverse bias of the I–V characteristic. Hence, an accurate value of the capacitance and conductance parameters is not only helpful to provide insights into the underlying device phenomena observed from the diode but also assists in optimizing the diode design which will further improve the diode performance in the circuit design process.

From Fig. 8, the conductance of the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diode is lower compared to that of GaAs/AlAs diode, especially at higher reverse bias. At low reverse bias, most of the voltage is dropped across the larger spacer for both devices. The conductance difference becomes significant when further reverse bias is applied, and this is largely due to the barrier height difference between the two devices.

When the GaAs/AlAs ASPAT is biased under high reverse voltages, the electrons have an increased probability of thermionic emission. A much higher barrier for the $In_{0.53}Ga_{0.47}As$/AlAs diode forces the electrons to tunnel through the barrier, thus making tunnelling the dominant transport mechanism and results in a much smaller conductance than GaAs/AlAs ASPAT diode under large reverse bias.

The S-parameters are solved from the physical modeling in Silvaco (excluding pad parasitic) and are then imported into advanced design system (ADS) software to validate the intrinsic components (R_s, C_j, and R_j) by comparison with measured data. In the ADS circuits, an intrinsic simulated block for the ASPAT S-parameters with parasitic capacitance and inductance were used as shown in Fig. 9. Both GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes show excellent fitting of the modeled and measured S-parameters under zero bias.

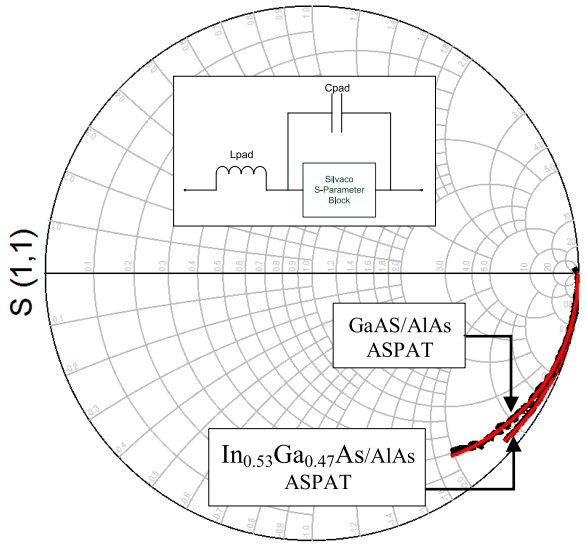

Fig. 9. Simulated and measured reflection coefficient for GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT Diode (4×4 μm^2) at zero. Black and red lines indicate the measured and simulated data, respectively. Inset is the Silvaco S-parameter block incorporating pad elements.

TABLE III
EXTRACTED VALUES FOR THE INTRINSIC COMPONENTS FOR A 4×4 μm^2 MESA AREA DEVICE AT ZERO BIAS

Device	Method	R_j (kΩ)	S_C (A/W)	R_s (Ω)	C_j (fF)	Theoretical intrinsic Cut-off Freq. (GHz)
GaAs/AlAs	Measured	95	14.3	11	22.8	633
	Silvaco Model	92	14.1	-	23.6	-
$In_{0.53}Ga_{0.47}As$ /AlAs	Measured	190	6.5	4.6	18.1	1911
	Silvaco Model	217	6.0	-	18.0	-

These are, to the best of our knowledge, the first report of S-parameters derived from the physical modeling of tunnel diodes. The ASPAT diode is a promising zero bias device, as its characteristics are optimized for zero-bias detection for reduced power consumption. The key parameters extracted from both dc and ac physical modeling of the intrinsic diode under zero bias are summarized in Table III.

The device parameters listed (i.e., R_j, C_j, and R_s) in Table III are important for designing the matching circuits in monolithic microwave integrated circuit detectors. The junction resistance, R_j from the measured data are calculated using the first derivative of the I–V characteristics, while for the Silvaco modeling, it was obtained from the reciprocal of the conductance. R_j is proportional to the device sensitivity and thus can help in evaluating detector circuit performance.

The diode curvature coefficient, k_v is computed using $k_v = (d^2I/dV^2)/(dI/dV)$. From the I–V characteristics, the calculated k_v for these ASPAT diodes are 28.6 and $13V^{-1}$. Previous works [31], [32] using InAs/AlGaSb tunnel diode and GaAsSb-based backward diode demonstrated k_v in the range of $40 - 50$ and $49.4V^{-1}$, respectively. The current responsivity, S_c was calculated using the classic Torrey–Whitmer expression [33]. The GaAs/AlAs ASPAT diode has a good S_c ($S_{c00} \approx 14A/W$) at zero-bias voltage and room temperature, which is comparable to other diodes [34]–[37]. Even though the $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diode has low S_c($S_{c_0} \approx$ 6 A/W), its high R_j can still provide high sensitivity but at the expenses of large sizes matching circuits. The highest current responsivities reported to date for other tunneling diode heterostructure [38] and Schottky diode [36] are 35 and 20 A/W, respectively, confirming that the ASPAT epitaxial layer must be carefully optimized to strike a balance between R_j and current responsivity.

The series resistances, R_s and C_j for both diodes are essential in order to extract the theoretical cut-off frequency by using the common expression [39], [40], $1/2\pi R_s C_j$. The series resistance R_s is the sum of the contacts, spreading and epilayer resistances [21].

As the maximum doping concentration is limited by a solid-solubility factor, the contact resistance for the GaAs/AlAs diode is higher than that for $In_{0.53}Ga_{0.47}As$/AlAs contributing to larger R_s for the former. Thus, the R_{Spr} for GaAs is higher compared to that of InGaAs. Due to the depletion width differences, the capacitance of the 4×4 μm^2 $In_{0.53}Ga_{0.47}As$/AlAs diode is ∼5 fF smaller than that of GaAs/AlAs when both devices are under zero bias. Because of these parameters values, a much lower cut-off frequency (633 GHz) is obtained for the GaAs/AlAs diode than the $In_{0.53}Ga_{0.47}As$/AlAs diode which approaches 2 THz.

V. CONCLUSION

In this paper, we successfully developed an accurate model for both GaAs/AlAs and $In_{0.53}Ga_{0.47}As$/AlAs ASPAT diodes which include structural material parameters and appropriate numerical methods. For dc modeling, the most precise structure for the simulations is observed from the planar device structures as it includes the spreading resistance influences as is the case in fabricated devices. The developed planar contact modeling was validated through different fabricated devices sizes. Following excellent agreements of the dc characteristics, an ac analysis model was then demonstrated for both ASPAT diodes. This latter is the first reported RF parameter extraction from the physical modeling for this type of tunneling heterostructure device. The simulated capacitances and S-parameter obtained, provided excellent fits to the measured data. This newly developed ac simulation can be implemented into millimeter-wave/terahertz frequency circuit designs for full optimization of zero-bias detector circuits.

REFERENCES

[1] N. Tuomisto, A. Zugarramurdi, and M. J. Puska, "Modeling of electron tunneling through a tilted potential barrier," *J. Appl. Phys.*, vol. 121, no. 13, p. 134304, 2017, doi: http://doi.org/10.1063/1.4979533

[2] R. T. Syme, M. J. Kelly, M. Robinson, R. S. Smith, and I. Dale, "Novel GaAs/AlAs tunnel structures as microwave detectors," *Proc. SPIE, Quantum Well Superlattice Phys. IV*, vol. 1675, pp. 46–56, Sep. 1992, doi: http://doi.org/10.1117/12.137622

[3] M. Baudrit and C. Algora, "Tunnel diode modeling, including nonlocal trap-assisted tunneling: A focus on III–V multijunction solar cell simulation," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2564–2571, Oct. 2010, doi: http://doi.org/10.1109/ted.2010.2061771

[4] G. McFarland and M. J. Flynn, *Limits of Scaling MOSFETs*. Stanford, CA, USA: Stanford Univ. Press, 1995.

[5] G. Fortunato, M. Rapisarda, A. Valletta, and L. Mariucci, "Contact effects in organic and inorganic thin film transistors," *ECS Trans.*, vol. 54, no. 1, pp. 171–185, 2013, doi: http://doi.org/10.1149/05401.0171ecst

[6] Y. Taur *et al.*, "CMOS scaling into the nanometer regime," *Proc. IEEE*, vol. 85, no. 4, pp. 486–504, Apr. 1997, doi: http://doi.org/10.1109/5.573737

[7] M. R. R. Abdullah, Y. K. Wang, J. Sexton, M. Missous, and M. J. Kelly, "GaAs/AlAs tunnelling structure: Temperature dependence of ASPAT detectors," in *Proc. 8th UK, Europe, China Millim. Waves THz Technol. Workshop (UCMMT)*, Sep. 2015, pp. 1–4, doi: http://doi.org/10.1109/UCMMT.2015.7460591

[8] Y. Wang, M. R. R. Abdullah, J. Sexton, and M. Missous, "Temperature dependence characteristics of $In_{0.53}Ga_{0.47}As$/AlAs asymmetric spacer-layer tunnel (ASPAT) diode detectors," in *Proc. 8th UK, Europe, China Millim. Waves THz Technol. Workshop (UCMMT)*, Sep. 2015, pp. 1–4, doi: http://doi.org/10.1109/ucmmt.2015.7460589

[9] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. New York, NY, USA: Wiley, 2006.

[10] N. Su, R. Rajavel, P. Deelman, J. N. Schulman, and P. Fay, "Sb-heterostructure millimeter-wave detectors with reduced capacitance and noise equivalent power," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 536–539, Jun. 2008, doi: http://doi.org/10.1109/LED.2008.922986

[11] S. Agarwal and E. Yablonovitch, "Band-edge steepness obtained from esaki/backward diode current–voltage characteristics," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1488–1493, May 2014, doi: http://doi.org/10.1109/TED.2014.2312731

[12] R. T. Syme, M. Kelly, R. S. Smith, A. Condie, and I. Dale, "Tunnel diode with asymmetric spacer layers for use as microwave detector," *Electron. Lett.*, vol. 27, pp. 2192–2194, 1991, doi: http://doi.org/10.1049/el:19911356

[13] R. T. Syme, "Tunnelling devices as microwave mixers and detectors," *Philos. Trans., Math., Phys. Eng. Sci.*, vol. 354, no. 1717, pp. 2351–2364, 1996, doi: http://doi.org/10.1098/rsta.1996.0104

[14] R. T. Syme, "Microwave detection using GaAs/AlAs tunnel structures," *GEC J. Res.*, vol. 11, pp. 12–23, Jan. 1993.

[15] P. Dasmahapatra, J. Sexton, M. Missous, C. Shao, and M. J. Kelly, "Thickness control of molecular beam epitaxy grown layers at the 0.01–0.1 monolayer level," *Semicond. Sci. Technol.*, vol. 27, no. 8, p. 085007, 2012, doi: http://doi.org/10.1088/0268-1242/27/8/085007

[16] R. T. Syme, "Novel semiconductor tunnelling devices for microwave applications," *Endeavour*, vol. 18, no. 3, pp. 90–95, 1994, doi: http://doi.org/10.1016/S0160-9327(05)80082-1

[17] *A. U. S. Manual*, Silvaco, Santa Clara, CA, USA, 2010.

[18] B. Jonsson and S. Eng, "Solving the Schrodinger equation in arbitrary quantum-well potential profiles using the transfer matrix method," *IEEE J. Quantum Electron.*, vol. 26, no. 11, pp. 2025–2035, Nov. 1990, doi: http://doi.org/10.1109/3.62122

[19] M. I. B. Shams, Y. Xie, Y. Lu, and P. Fay, "An accurate interband tunneling model for InAs/GaSb heterostructure devices," *Phys. Status Solidi C*, vol. 10, no. 5, pp. 740–743, 2013, doi: http://doi.org/10.1002/pssc.201200624

[20] H. Mizuta and T. Tanoue, *The Physics and Applications of Resonant Tunnelling Diodes*, vol. 2. Cambridge, U.K.: Cambridge Univ. Press, 2006.

[21] H. Kanaya, T. Maekawa, S. Suzuki, and M. Asada, "Structure dependence of oscillation characteristics of resonant-tunneling-diode terahertz oscillators associated with intrinsic and extrinsic delay times," *Jpn. J. Appl. Phys.*, vol. 54, no. 9, p. 094103, 2015, doi: http://doi.org/10.7567/JJAP.54.094103

[22] E. R. Brown, W. D. Goodhue, and T. C. L. G. Sollner, "Fundamental oscillations up to 200 GHz in resonant tunneling diodes and new estimates of their maximum oscillation frequency from stationary-state tunneling theory," *J. Appl. Phys.*, vol. 64, no. 3, pp. 1519–1529, 1988, doi: http://doi.org/10.1063/1.341827

[23] T. P. E. Broekaert and C. G. Fonstad, "$In_{0.53}Ga_{0.47}As$/AlAs resonant tunneling diodes with peak current densities in excess of 450 kA/cm^2," *J. Appl. Phys.*, vol. 68, no. 8, p. 4310, 1990, doi: http://doi.org/10.1063/1.346226

[24] O. Madelung, U. Rössler, and M. Schulz, Eds., "Aluminum arsenide (AlAs), effective masses," in *Group IV Elements, IV-IV and III-V Compounds. Part B—Electronic, Transport, Optical and Other Properties*. Berlin, Germany: Springer-Verlag, 2002.

[25] W. M. Yim, "Direct and indirect optical energy gaps of AlAs," *J. Appl. Phys.*, vol. 42, no. 7, pp. 2854–2856, 1971, doi: http://doi.org/10.1063/1.1660639

[26] Y. Tang *et al.*, "Convergence of multi-valley bands as the electronic origin of high thermoelectric performance in $CoSb_3$ skutterudites," *Nature Mater.*, vol. 14, pp. 1223–1228, Oct. 2015, doi: http://doi.org/10.1038/nmat4430

[27] A. C. Sharma, N. M. Ravindra, S. Auluck, and V. K. Srivastava, "Temperature-dependent effective masses in III–V compound semiconductors," *Phys. Status Solidi B*, vol. 120, no. 2, pp. 715–721, 1983, doi: http://doi.org/10.1002/pssb.2221200231

[28] R. L. Anderson, "Experiments on Ge-GaAs Heterojunctions," *Solid-State Electron.*, vol. 5, no. 5, pp. 341–344, 1962, doi: http://doi.org/10.1016/0038-1101(62)90115-6

[29] T. Ren, Y. Zhang, R. Xu, J. Zhou, C. Yang, and Z. Jin, "A 340–400 GHz zero-biased waveguide detector using an self-consistent method to extract the parameters of Schottky barrier diode," *Appl. Comput. Electromagn. Soc. J.*, vol. 30, no. 12, pp. 1334–1340, 2015.

[30] J. Cha, J. Cha, and S. Lee, "Uncertainty analysis of two-step and three-step methods for deembedding on-wafer RF transistor measurements," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2195–2201, Aug. 2008, doi: http://doi.org/10.1109/TED.2008.926752

[31] T. Takahashi, M. Sato, K. Makiyama, Y. Nakasha, N. Hara, and T. Iwai, "High-speed III-V devices for millimeter-wave receiver applications (Invited)," in *Proc. IEEE Int. Symp. Radio-Frequency Integr. Technol. (RFIT)*, Aug. 2015, pp. 238–240, doi: http://doi.org/10.1109/RFIT.2015.7377946

[32] L. Liu, S. M. Rahman, Z. Jiang, W. Li, and P. Fay, "Advanced terahertz sensing and imaging systems based on integrated III-V interband tunneling devices," *Proc. IEEE*, vol. 105, no. 6, pp. 1020–1034, Jun. 2017, doi: http://doi.org/10.1109/JPROC.2016.2636245

[33] E. R. Brown, "A system-level analysis of Schottky diodes for incoherent THz imaging arrays," *Solid-State Electron.*, vol. 48, nos. 10–11, pp. 2051–2053, 2004, doi: http://doi.org/10.1109/ISDRS.2003.1272144

[34] M. Patrashin *et al.*, "GaAsSb/InAlAs/InGaAs tunnel diodes for millimeter wave detection in 220–330-GHz band," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 1068–1071, Mar. 2015, doi: http://doi.org/10.1109/TED.2015.2393358

[35] J. N. Schulman *et al.*, "High frequency performance of Sb-heterostructure millimeter-wave diodes," in *Proc. 14th Indium Phosph. Rel. Mater. Conf. (IPRM)*, May 2002, pp. 151–154, doi: http://doi.org/10.1109/ICIPRM.2002.1014164

[36] P. Chahal, F. Morris, and G. Frazier, "Zero bias resonant tunnel Schottky contact diode for wide-band direct detection," *IEEE Electron Device Lett.*, vol. 26, no. 12, pp. 894–896, Dec. 2005, doi: http://doi.org/10.1109/LED.2005.859622

[37] V. Radisic, K. Leong, C. Zhang, K. K. Loi, and S. Sarkozy, "Demonstration of a micro-integrated sub-millimeter-wave pixel," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2949–2955, Aug. 2013, doi: http://doi.org/10.1109/tmtt.2013.2272379

[38] J. Karlovský, "The curvature coefficient of germanium tunnel and backward diodes," *Solid-State Electron.*, vol. 10, no. 11, pp. 1109–1111, 1967, doi: http://doi.org/10.1016/0038-1101(67)90131-1

[39] M. Shur, *Physics of Semiconductor Devices*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1990.

[40] S. Sankaran and Kenneth K. O, "Schottky barrier diodes for millimeter wave detection in a foundry CMOS process," *IEEE Electron Device Lett.*, vol. 26, no. 7, pp. 492–494, Jul. 2005, doi: http://doi.org/10.1109/led.2005.851127

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