Metallic Single Electron Transistors: Impact of Parasitic Capacitances on Small Circuits

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***Abstract*— A method of simulating metallic-island single electron transistors (SETs) and small circuits which speeds up the design-fabrication-characterization cycle is proposed. The method combines finite-elements method to extract device capacitance matrix and standard master equations solved by Monte Carlo to simulate device transport characteristics based on the fabrication geometry and materials. It allows simulation of SET circuits. The simulation method is detailed using two capacitively coupled SETs acting either as an electron box or a sensor. The method is also compared with isolated SETs fabricated using the *nanodamascene* process and characterized at low temperatures. Experimental devices show clear Coulomb blockade diamonds at 1.5 K and charging energies up to 3 meV. The simulation platform predicts the electrical behavior accurately with minimal fitting parameters. This method allows rapid and accurate design iterations before costly fabrication.**

***Index Terms*—Charge sensing devices, finite-element analysis, Monte Carlo methods, nanofabrication, single electron transistors (SETs).**

I. Introduction

THE on-going race to improve electronic device performance is now driven by the reduction of energy consumption. Single electron devices offer interesting properties like low-power operation and high charge sensitivity, which can complement state-of-the-art transistors in low-power and sensitive applications. The flagship single electron transistor (SET) used as a highly sensitive charge detector [1] has many applications such as gas sensing [2] or quantum-dot charge detection [3]. Only a few experimental demonstrations have shown room temperature operation [4]-[7], which limits the application range to cryogenic temperatures. Moreover, in most of these experiments, only single isolated devices are demonstrated. Since total capacitance of the SET island is the critical parameter in the charging energy, smaller devices are usually the path to higher operation temperatures. However, in SET circuits at small dimensions, parasitics need to be considered which may impact the devices performance significantly. Targeting material parameters and design through careful simulation can help achieve higher operating temperatures at lower costs. For the SET, the capacitance of complex nonparallel plate geometries needs to be taken into account [8] with their impact on transport properties of the device.

Modeling of semiconductor quantum dots including the capacitance matrix and transport characteristics was achieved in recent years using finite-elements modeling (FEM) [9] or similar methods [10] leading to accurate results for complex geometries. Several transport simulation models have also been developed using varied approaches like direct master equation solvers [11], [12], Monte Carlo [13]–[15], genetic algorithms [16] or SPICE methods [17]–[20]. In this paper, we propose to combine finite-elements simulation, to extract full capacitance matrix from a manufacturable geometry, with a Monte Carlo master equations solver (SIMON [15]), to capture the complete electrical transport characteristics of metallic single electron circuits. We use two SETs facing each other to demonstrate the simulation method and compare it to experimental devices. The validity of the platform is confirmed by the successful simulation of an isolated SET, and two capacitively coupled SET. The simulation shows good correspondence with experiment, further validating the design platform. We then show that reducing size even more than currently achievable gives limited improvement to the operating temperature when considering a realistic circuit and confines this technology to cryogenic applications.

II. Finite Elements and Monte Carlo Simulations

We use Comsol Multiphysics® for the FEM of the capacitance matrix of our device. Although FEM has its drawbacks [21], the ease of use of Comsol and the ability of generating the device geometry by importing the fabrication CAD and simple geometric operations such as extruding and

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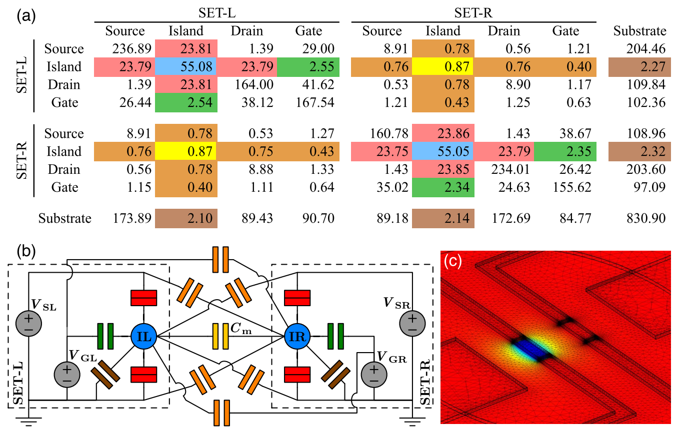
Boolean make it efficient for generating the full 3-D device geometry. To calculate the capacitance matrix $\mathbf{C}$ of a circuit, one must obtain the charges on all electrodes of the circuit for a potential distribution through

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \vdots \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \cdots \\ C_{21} & C_{22} & \cdots \\ \vdots & \vdots & \ddots \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \end{bmatrix} \tag{1}$$

where Q_i and V_i are, respectively, the charge and potential of one of the electrodes or islands. Electrostatic conditions and perfect insulators are assumed in the following. This means constant uniform potential of each metal electrode and non-polarizing insulators. The free charges on the metal electrodes (conduction electrons) are the only relevant charges considered here. In Comsol, we define the 3-D device geometry based on intended fabrication process and then set one electrode at a potential of 1 V and the others to ground. Solving Gauss's law, $\nabla \cdot \mathbf{D} = \rho_\mathbf{V}$, in these conditions, we obtain the complete system charge distribution. We then integrate the free charge density ρ_V over each electrode to obtain the total charge on the electrode, which is directly equal to the capacitance in this potential distribution. Integration over the 1-V element gives the diagonal elements of the matrix C_{ii} representing its self-capacitance. Integration over the other elements gives the off-diagonal elements C_{ij} representing the coupling capacitances between different elements. We finally repeat this process while cycling the 1-V electrode to get the full matrix. Solving this problem in iterations is required since vector division cannot be uniquely defined for matrix multiplication, i.e., we cannot divide vectors $\mathbf{Q}$ and $\mathbf{V}$. Using this method, we can account for all fringe fields in the device and the difference in electrical permittivity between the different insulators involved in all capacitances of the complete circuit. It is of importance to mention here that since the devices under consideration are metallic SETs, the obtained capacitance matrix is considered fixed for any bias conditions. Indeed the metal islands are large enough that the Fermi wavelength is much smaller than the dots themselves rendering the contribution of confinement negligible [1], [22].

Fig. 1(a) gives the full capacitance matrix (in aF) for the geometry of the two facing SETs, SET-L for the left SET and SET-R for the right SET, schematically represented in Fig. 1(b). The two diagonal elements in blue are the self-capacitances of importance here giving the charging energy of the SET ($E_c \approx 2.9$ meV). Other colored elements of the matrix represent the coupling capacitances between the line and column headers and correspond to the colors used in the circuit diagram of Fig. 1(b) where SET-L and SET-R are identified by the dashed boxes. The yellow cells represent the coupling between the two SETs islands which is used for the charge detection scheme described in Section V. Here the other cross couplings are also useful to compensate undesired couplings between an island and the neighboring sources ($V_{\mathrm{SL(SR)}}$), grounded drains, and gates ($V_{\mathrm{GL(GR)}}$). Fig. 1(c) shows the central part of the mesh used in the simulation for the facing SET. The full simulation includes an area of about 4 μm^2 around the center of the SETs. The underlying 150 nm of



(a)

		SET-L				SET-R				
		Source	Island	Drain	Gate	Source	Island	Drain	Gate	Substrate
SET-L	Source	236.89	23.81	1.39	29.00	8.91	0.78	0.56	1.21	204.46
	Island	23.79	55.08	23.79	2.55	0.76	0.87	0.76	0.40	2.27
	Drain	1.39	23.81	164.00	41.62	0.53	0.78	8.90	1.17	109.84
	Gate	26.44	2.54	38.12	167.54	1.21	0.43	1.25	0.63	102.36
SET-R	Source	8.91	0.78	0.53	1.27	160.78	23.86	1.43	38.67	108.96
	Island	0.76	0.87	0.75	0.43	23.75	55.05	23.79	2.35	2.32
	Drain	0.56	0.78	8.88	1.33	1.43	23.85	234.01	26.42	203.60
	Gate	1.15	0.40	1.11	0.64	35.02	2.34	24.63	155.62	97.09
	Substrate	173.89	2.10	89.43	90.70	89.18	2.14	172.69	84.77	830.90

Fig. 1. (a) Full capacitance matrix (in aF) of two capacitively coupled SETs as in (c). Coloring of the matrix elements corresponds to the circuit considered in (b) for the islands (blue), tunnel junctions (red), gates (green), substrate (brown), coupling (yellow), and parasitic (orange) capacitors. The two SETs are identified by the dashed lines. (c) 3-D mesh used for capacitance simulations superimposed on the potential gradient obtained from it.

SiO_2, 100 nm of Si_3N_4 cap, and an extra air layer on top are added to the device to complete the full 3-D geometry. The silicon substrate is modeled as the bottom plane of the SiO_2 substrate, whereas the top and sides of the model extend the materials of the layer to infinity. To achieve stable results with the simulation, meshing of the volume is critical and the best way of getting reasonable simulation time and accuracy is by using fast expanding free meshes with very high resolution only in the regions, where electric fields are highest, i.e., the tunnel junctions. Color in the image shows the potential gradient obtained for 1 V applied on the island of SET-L and ground applied on all other elements of the circuit giving the second line or column of the matrix of Fig. 1(a).

To obtain the device electrical transport properties, the equivalent circuit is implemented in the SIMON software [15] using capacitance values from the matrix extracted from Comsol. The circuit contains all relevant capacitances, including all parasitic couplings. Cross capacitances between leads were neglected since they only impact external voltage sources. SIMON is chosen for its capability of simulating general tunnelling and Coulomb blockade (CB) circuits with fast simulation of stability diagrams. Results obtained from this simulation are presented in Section IV alongside experimental results obtained from the fabricated devices.

III. Materials and Processes

The devices used to validate the simulation platform are SETs fabricated using the *nanodamascene* process from [7], [23], and [24]. The major steps are summarized here for readability. First, narrow trenches are patterned using electron beam lithography (EBL) in ZEP520 resist and etched in SiO_2 using an inductively coupled plasma with CF_4 chemistry [25]. Next, using a bilayer ZEP520/MMA resist stack, a narrow metallic Ti line is evaporated onto the sample followed by *in situ* oxidation creating the required tunnel oxide junctions. After a blanket Ti metal deposition, a chemical mechanical polishing (CMP) step is conducted to planarize

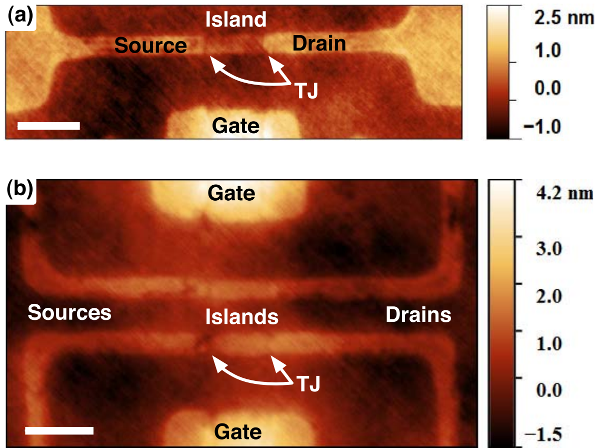


Fig. 2. AFM topography of single isolated SET (a) from [24], and (b) two capacitively coupled (side-by-side) SETs after the planarization step (CMP). TJ indicates the tunnel junctions. Scale bar is 100 nm.

the surface and isolate the initial trenches containing the leads, oxide tunnel junctions, and island. Devices are then passivated using a 100-nm Si_3N_4 layer deposited by plasma enhanced chemical vapor deposition. Contact vias are then etched and filled to allow electrical connection to the underlying devices. Measurements down to 1.5 K were conducted in a variable temperature cryostat using a semiconductor parametric analyser. Examples of the obtained uniformity after CMP are shown in Fig. 2. In Fig. 2(a), the typical topography of an isolated SET, measured by atomic force microscopy (AFM), is shown. This simple device is used as a reference for validation of the simulation method. Fig. 2(b) shows a similar image for two capacitively coupled SETs. Both images show the high surface uniformity (better than 5 nm) obtained from the CMP step over the relevant device area.

IV. Isolated SET Characterization and Simulation

Fig. 3(a) shows the Coulomb diamonds obtained from SET-1 at 1.5 K. Dimensions of this device, given in Table I, are measured with the following methods. The width of the trench w_T is extracted from the AFM topography of the device after the planarization step. The metal depth remaining in the trenches cannot be measured directly. Using a nearby trench without the metal island liftoff, we therefore create a nanowire. Combined to a model described in more details in [26], we use the resistance of this nanowire to extract the remaining metal thickness. The tunnel junction oxide thickness is measured indirectly by ellipsometry of thin blanket metal films oxidized *in situ* with the same parameters as final devices. The method and model used is described in [27]. C_S, C_D, and C_G, the source, drain, and gate capacitances, and the charging energy E_C are extracted from the negative slope, positive slope, and pitch of the Coulomb diamonds as described in [28].

Fig. 3(b) shows the simulated Coulomb diamonds obtained with our simulation platform using only the junction dielectric constant and tunnel resistance as variable parameters. Dielectric constant ϵ_r^J is adjusted to match the experimental charging energy. Tunnel resistances of the source (R_S) and drain (R_D) junctions are adjusted to get similar current amplitudes and

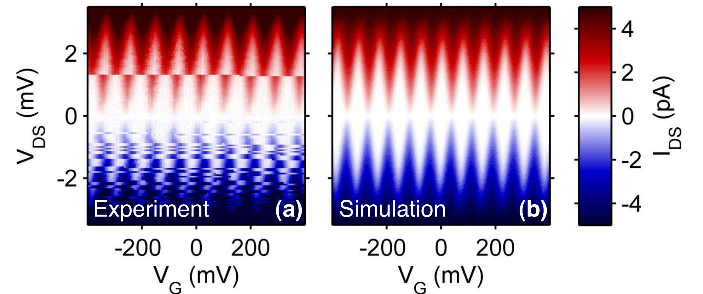


Fig. 3. (a) Experimental Coulomb diamonds measured at 1.5 K on SET-1. (b) Simulated Coulomb diamonds using the fabricated geometry of SET-1. Tunnel resistances and dielectric constant were adjusted to match the experimental results.

TABLE I
SET Parameters Extracted Experimentally

	SET-1		SET-2	
Device	Exp.	Sim.	Exp.	Sim.
w_T (nm)	30	-	20	-
t_{CMP} (nm)	13.4	-	8.5	-
t_{ox} (nm)	4.9	-	4.9	-
C_S (aF)	38	34	26	21
C_D (aF)	67	34	22	21
C_G (aF)	1.8	2.1	0.3	1.7
E_C (meV)	1.5	2.3	3.1	3.8
ϵ_r^J	40	-	45	-
R_S (MΩ)	145	-	200	-
R_D (MΩ)	180	-	100	-

Table Notes: w_T is the trench width; t_{CMP} is the metal thickness in the trench after CMP; t_{ox} is the tunnel junction oxide thickness; C_S, C_D, and C_G are the source, drain, and gate capacitances. $E_C = C_S + C_D + C_G$ is the charging energy.

with a ratio matching the shape drift observed at the tip of the diamonds. 3-D geometry of the simulation is directly based on the center 2-μm area of the drawn pattern with trench width, depth, and oxide thickness modified to correspond to in-process measurements as mentioned above. No other special adjustments are used to get good agreement with experiment.

Using the experimental geometric parameters, we obtain capacitance and energy values close to the experimental ones (Table I). Variations seen in Table I can be explained by differences between the actual and expected geometry of the island and junctions of the devices. Defects like the ones seen in Fig. 2(b) can significantly alter the microscopic geometry of the tunnel junctions, which is not taken into account in the capacitance simulation. We also note the low-measured gate capacitance of SET-2 compared to the simulation. This could be due to ripping off of the part of the gate metal deposited during the island patterning step. This would cause a lower than expected C_G by the effective distance being larger than designed. This does not, however, imply any changes on the measured C_S and C_D since C_G is part of the calculation and cancels out (see [28]). The dielectric constant obtained from the fitting is in the range of values found in literature for titanium oxide [7], [29]–[32]. The jumps (steps) seen in Fig. 3(a) are caused by random charge noise from defects in the vicinity of the island. These defects are expected for the SiO_2 system used here and their effect should be reduced by

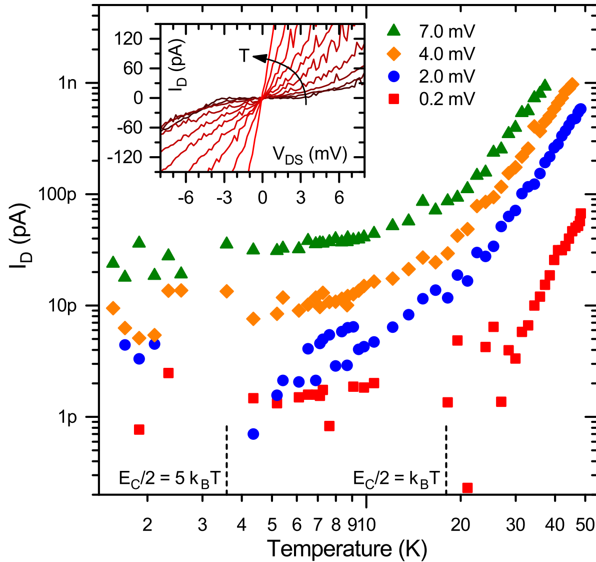


Fig. 4. Drain current at various V_{DS} for SET-2 as a function of temperature. Dashed lines represent the operating temperature criteria $E_C/2 = xk_BT$. Inset shows full I_D–V_{DS} curves for increasing temperature (dark to light color) from which the temperature curves were taken.

the use of careful annealing [33]–[35] after the critical EBL, etch, and CMP steps that mainly contribute to their creation. The number of jumps and their position at which they occur is not coherent confirming the defect nature of their origin. Devices fabricated with the same process but with improved stability and performances have been presented in [24]. The good overall correspondence of the simulation results with the *nanodamascene* fabricated devices shows the platform is useful for design and optimization of metallic single electron devices.

Fig. 4 gives current measurements as a function of temperature for different biases in SET-2. The curves show two clear regimes of operation. The low-temperature regime is flat since conduction slightly varies as a function of temperature due to the CB. At higher temperature, the power law increase in current is driven by the thermal broadening of the Fermi level above the CB gap. The current–voltage measurements at different temperatures in the inset show clear attenuation of the CB regime with the vanishing of the plateau around zero bias. As identified by the dashed lines, the transition from low to high temperature regimes happens at the temperature, where half of the charging energy $E_C/2$ is equal to the thermal energy k_BT. Here, this occurs at a temperature of 18 K, which corresponds to a charging energy of 3.1 meV. This value also corresponds to the width of the CB region in the inset, thus confirming that the device behavior is indeed governed by CB. As shown in the second column of Table I, capacitances obtained from the simulation for this SET are also similar to the experimentally extracted ones. Moreover, the charging energy value is also comparable to the experiment further validating the model.

V. SETs for Cryogenic Charge Detection

As previously reported in [24], charge sensitivity has been demonstrated for the two SET geometry of Fig. 2(b). The authors report successful measurement, at 50 mK, of the characteristic honeycomb structure for two Coulomb islands in proximity. Formalism for two tunnel-coupled quantum dots is used to extract the coupling capacitance of the two islands and yields reasonable agreement with the simulation described here. The experimental value of 0.1 aF is comparable to the simulated value of 0.9 aF obtained from the modeling presented in Section II. Similarly to Section IV, a large part of the difference observed here could be explained by the actual dimensions of the device. In Fig. 2(b) and on other similar devices, we observe some defects on the sides of the islands. If the actual island is smaller due to these defects, it would mean similar individual SET characteristics, but smaller coupling since the cross section of the two islands is smaller. A simulation of the device of Fig. 2(b) with half the island length (distance between C_S and C_D) gives a dot-to-dot coupling of 0.3 aF pointing to shorter than expected SET island due to process defects. Considering this, the comparison further confirms the validity of the simulation method developed here and allows further study of device sizes not yet reachable in the current state of development of the *nanodamascene* process.

We simulated two ultrascaled coupled SET with dimensions similar to those of a fabricated room temperature SET [7] but in a tighter configuration representing a densely integrated circuit. Trench width is 5 nm, trench depth is 2 nm, junction oxide thickness is 6 nm, gate-dot distance is 15 nm, and dot-dot distance is 40 nm. With these dimensions, we obtain a charging energy of 38 meV and an operating temperature of 45 K for the standard $E_C = 10k_BT$ criterion [1]. This shows that even though the island volume is reduced by a factor of 30, the charging energy dropped by a factor of 2. This is explained by the large difference in metal density around the islands including a closer gate. Although the source and drain capacitances have been reduced, parasitic capacitances have increased and start dominating in this size range. The use of modeling here is therefore critical to correctly optimize device and circuit architectures by accounting for parasitic capacitances in the regime, where the charging energy is not dominated by the tunnel capacitance anymore but by the island environment. This also has an impact on the maximum operating temperature that can be achieved with this technology.

As a more complex circuit example, with the constraints of our fabrication process, we designed the active area of a quantum-dot cellular automata (QCA) half-cell based on the proposition by Orlov *et al.* [36]. We scaled the geometry given in this proposition to similar dimensions of SET-1 as a starting point. Then for further scaling, tunnel junction cross sections were reduced from 30 nm × 10 nm to 5 nm × 2 nm as in the ultrascaled coupled SET above. The tunnel junction oxide thickness and dielectric constant were fixed to 6 nm and 3.5, respectively, similar to [7] improving the expected charging energy compared to the measured devices in this work. The complete set of geometric dimensions for the simulation is given in Table II. The geometric parameters used here do not translate directly to the geometry of [36], but their equivalent was used based on their publication. The complete geometry used in our simulation is given in Fig. 5(a)–(c). For all six

TABLE II
ISLAND DIMENSIONS FOR QCA HALF-CELL SCALING

Geometry		G1	G2	G3	[36]
Lateral QCA islands	w_T	5	10	30	60
	t_{CMP}	2	5	10	25
	L	32	42	172	5200
Central QCA islands	w_T	5	10	30	60
	t_{CMP}	2	5	10	50
	L	59	84	479	7800
SET islands	w_T	5	10	30	60
	t_{CMP}	2	5	10	50
	L	8	14	50	2500

Table Notes: L is the island length, i.e. distance between the two tunnel junctions. Other parameters are defined in Table I

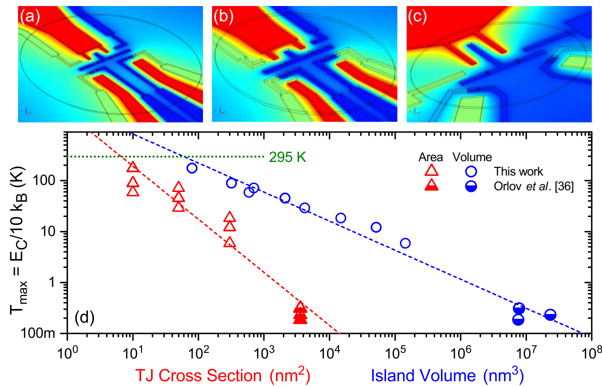


Fig. 5. Geometry used in simulation of the scaling of a model QCA half-cell with dimensions given in Table II for (a) G1, (b) G2, and (c) G3. (d) Plots of the charging energies of the islands in each design converted to operating temperature using $E_C = 10k_BT$. The half filled symbols correspond to the islands given in [36], other data are from simulations using the model presented here. Dashed lines are power law fits with exponents of -1.04 and -0.57 for the cross section and volume, respectively.

tunnel junctions, the dimensions are the same, but the lengths of the islands are different for the SET and, the center and lateral islands of the QCA. Given in Table II are also the values of the work shown in [36] as a reference point. Fig. 5(d) plots the calculated charging energies of each island converted to operating temperature using $E_C = 10k_BT$ as a function of tunnel junction cross section and island volume. All simulated points shown in Fig. 5(d) had no Si_3N_4 passivation layer to better compare to the reference work, which was also not passivated.

We observe power law dependence of the charging energy to the physical dimensions of the islands and junctions as expected. The exponents obtained here, -1.04 and -0.57 for the cross section and volume, respectively, correspond well to the expected dependency given by $T \propto E_c \propto C_\Sigma^{-1} \propto A^{-1} \propto V^{-2/3}$, where A is the tunnel junction cross section and V the island volume which proportionality exponent comes from unit considerations. We note that in both cases, there is a deviation from the power law fit at smaller dimensions which is explained by the combination of two things. The first is that the scaling of the dimensions is not completely uniform for all parts of the geometries. The second is that at small cross section, the island capacitance becomes dominated by the fringe capacitances of the large gates and leads.

Extrapolating from the power law fits, we find an island volume of 60 nm^3 and a cross section of 6.6 nm^2 as upper bounds for room temperature operation. This corresponds to 3.9 and 2.6 nm of critical dimensions, which are smaller than the limit of what fabrication techniques can and will allow. These dimensions are also in line with bounds predicted by [37]. This puts a limit on the application temperature range of this technology as a whole. However, charge detection can still be useful in the low temperature range, for instance, where quantum bits (qubits) generally operate. In this field, going to larger scale circuits will mean requiring more efficient space use and there, the *nanodamascene* SET might offer the benefit of not requiring a crystaline substrate. It can therefore be fabricated above the qubits and used as charge sensor and conversion stage from the quantum to the classical regime of information. The process described here can also be improved in several ways. EBL and liftoff can be replaced by the industry standard immersion lithography combined to etch-fill-planarize processes. Atomic layer deposition can also be used to optimize tunnel junction dielectric properties [38], [39] and help reducing trench size by partially filling them with atomic precision. Charging energies can also be improved by increasing the gate-island distance, using lower oxide dielectric constants or different design, where density of metal in the vicinity of the relevant islands is minimized.

VI. CONCLUSION

We have proposed a novel method for the design and simulation of electrical characteristics in metallic single electron devices and small circuits. An isolated SET and two facing SETs have been successfully simulated and fabricated with experimental data fitting the simulations. Using the *nanodamascene* process, we have obtained well behaved, individual SETs at cryogenic temperature with relaxed dimensions, and two SETs side-by-side demonstrating their operation as charge detectors [24]. In both studied cases, good correspondence of the simulated and experimentally measured device parameters is found with few fitting parameters. Finally, we conclude that parasitic capacitances in a realistic SET circuit, a QCA half-cell, will prevent room temperature operation even with sizes beyond those achievable today and in the foreseeable future. It does not, however, prevent the SET from being used as a dedicated cryogenic charge detection device in the quantum computing field. Our proposed design and simulation platform along with the *nanodamascene* fabrication process can be applied to more complex circuits of single electron nature like SET inverter, SRAM, or full adder [40], [41]. Improvement in speed of the simulation can be achieved with faster electric field solving methods provided that the complex geometries can be considered. Streamlining the full simulation path from capacitance calculation to Monte Carlo solving of the master equations in a single software would also greatly improve the efficiency of the simulation. Adding process simulation to the mix would also allow results accounting for the real geometry of the devices. The design and simulation

platform enables the study of the impact of most parameters (e.g., geometry, materials, and distances) on the electrical behavior of the devices and circuits. It can finally be exploited to determine suitable materials and architectures with faster and more efficient iteration loops than full fabrication runs.

VII. Acknowledgment

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