Exploring the Influence of Variability on Single-Electron Transistors Into SET-Based Circuits

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***Abstract*— We analyze the performance of hybrid single-electron transistor (SET)–FET circuits when different variability sources are considered, e.g., SET's quantum dot location and FET device dimension variations. For the FET device, FinFET and vertical nanowire configurations have been studied. The hybrid SET–FET circuits with both SET and FET in vertical topology depict the best circuit performance and the highest integration level. The variability impact on different SET-based circuits has been analyzed, including negative differential resistance and logic inverters.**

***Index Terms*— MOSFET, single-electron transistor (SET), variability.**

I. Introduction

CURRENTLY, the electronics industry is working to overcome two main challenges: device power consumption and scaling down of device dimensions. The former is related to the increasing relevance of the "Internet of Things," due to the growing use of tiny computers on many areas of the society. Thus, the exploration of a new technology for the fabrication of devices with less power consumption becomes of high relevance. The single-electron transistor (SET) appears as a promising device since it can work in small dimensions (<10 nm) and with significantly less power consumption than standard devices [1]–[3]. The channel of an SET is defined by a small island or quantum dot (QD), sandwiched between source and drain regions. The island is coupled to the source and drain through tunnel junctions. The core aspects of the SET's operation are the tunneling effect and Coulomb blockade, which are described by the "orthodox theory of single-electron tunneling." This is founded on three major assumptions.

1) Tunnel junction resistances, at drain and source regions (R_D and R_S), are greater than the quantum resistance (25.8 kΩ) to ensure the confinement of the electrons in the island.
2) The island charge is discrete, but the energy is continuous (for metallic SETs).
3) There is no co-tunneling [4]. For a feasible CMOS process integration of the SET, a silicon-based SET arises as a promising candidate; then, the energy quantization cannot be neglected [5].

Although significant benefits are provided by SETs, e.g., low power consumption, some drawbacks threaten their feasibility, such as background charge noise (BCN), low drive current, device stability, and the requirement of ultralow temperature operation. The first is highly relevant because it is related to random charge near the SET island that affects the device behavior, but it could be reduced by using silicon-based SETs [6], [7] or specific circuits [8]. Low drive current can be overcome by integration with MOSFETs. This is possible because both device fabrication processes (SET and FET) are compatible [9]. The SET's Coulomb blockade would be amplified at the drain terminal of the MOSFET, enlarging then the drive current capabilities at the output of the overall hybrid circuit. The hybrid CMOS-SET circuit is an interesting configuration, seeking to combine the benefits of both devices (e.g., SET's ultralow power consumption and scalability and FET's high speed and voltage gain) and allowing to design circuits with enhanced functionality [7], [10]. Besides, the suitability of both devices for a co-integration into a CMOS process [9], [11] is a real benefit for a feasible manufacturing process. When the SET conducting island is large, the device can only operate at cryogenic temperatures, but by reducing the dimensions below 10 nm, single electron effects appear even at room temperature [7], overcoming this drawback of SETs.

In the context of scaling down device dimensions, the conventional planar MOSFET is usually discarded for technology nodes beyond 32 nm, since its reliability is highly affected due to unacceptable leakage currents and large device performance variability [12]. Different FET types have substituted it. The FinFET has been one of the preferred industry solutions, as it presents a performance enhancement and larger device variability tolerance [13]. But for technology nodes beyond 10 nm, the vertical nanowire (vNW) transistor also appears as a feasible substitute of the MOSFET. Its low

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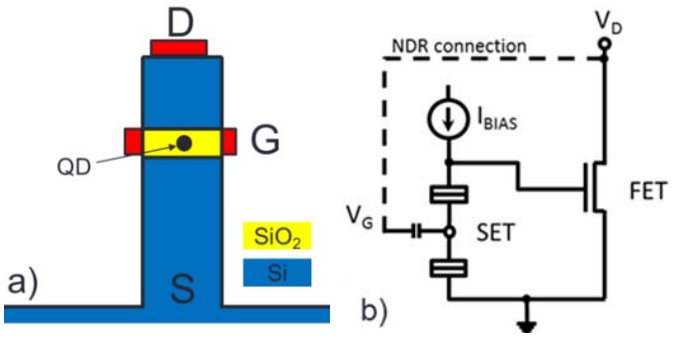

Fig. 1. (a) Topology of the SET device. (b) Schematic configurations for a hybrid SET–FET and NDR circuits.

footprint significantly reduces the area cost together with a high device performance and lower variability level [14].

So, in this paper, we study the feasibility of SET–FET circuits, operative at room temperature. Several approaches are presently being addressed to provide integral room temperature SET devices [9], [15]. The feasibility of a vertical SET (vSET) device has been studied in [16], which shows a relevant benefit on area footprint reduction, although this proposal is not able to operate at room temperature. A valid proposal for a vSET is a silicon-based nanopillar structure with an intermediate SiO_2 layer thinner than 10 nm [Fig. 1(a)], where the QD would be self-assembled after the annealing of a silicon ion implantation into the oxide layer [17], [18]. Although it is still under evaluation [18], [19], this vSET implementation could be a promising option for larger device density integration and room temperature operation. In terms of fabrication, this device is especially suitable for integration in CMOS circuit. This paper explores the benefits of the use of different FET types (FinFET and NW) within SET-based circuits. These FET options appear more promising [20] in terms of device reliability and power consumption. In these simulations, the QD's position is varied to study the effect on the final SET-based circuits' behavior, as the SET parameters could shift.

The remainder of this paper is organized as follows. Section II explains the device models used to simulate the SET-based circuits and the overall simulation environment. Section III studies the impact of both devices parameter variations on the hybrid circuit behavior. Section IV presents the influence of the parameter variability on the current variability of the hybrid SET–FET circuit. Section V explores the variability impact on different SET-based circuits. Section VI summarizes the conclusions of the whole analysis.

II. SET–FET Simulation Framework

This section describes how we define and simulate the different circuits studied, and the conditions of the analysis that has been performed.

A. Definition of the SET and FET Device Characteristics

To address a correct analysis of SET-based circuits, it is necessary to have good electrical models. Different models exist to simulate the SET behavior, among others.

TABLE I
SET and FET Devices Main Parameters

SET	FinFET	NW
$C_G = 0.37a$ $C_{S,D} = 0.12a$ $R_D = 1M$ $R_S = 19M$	$L = 24n$ $h_{FIN} = 28n$ $t_{FIN} = 15n$	$D = 40n$ $L = 30n$

1) Uchida's model [2] is more accurate at higher temperatures than the other models, and over a wide range of drain voltages.
2) The MIB model [1] is more flexible and less time consuming for simulations, as fewer exponential terms are required.
3) Finally, Inokawa's model [3] extends Uchida's model to include simulations of asymmetric SETs.

The sources of asymmetry could be related to the QD location and the device topology. For this, the asymmetric characteristic of Inokawa's model is important for our study as it allows to study the impact of SET behavioral variations due to the QD location. Although this model does not consider the BCN, we have simulated it as a flicker noise, with a voltage source in series with the gate terminal [21], with values extracted from [6].

We simulate vertical pillars with the structure shown in Fig. 1(a) [18]. In this device, the source and drain region resistances are different. Only a few studies have analyzed the behavior of a vSET [16], and none of them has simulated their suitability to implement different SET-based circuits at room temperature, neither analyzed the introduction of device variations on SET-based circuits' performance. Fig. 1(b) presents a hybrid SET–FET circuit which is usually composed of two devices (SET and FET), a current source (I_{BIAS}), and a voltage source (V_D) [1]. This circuit is very convenient for the experimental characterization of the SET performance.

The SET model is based on different parameters that refer to the capacitance and resistance of the source/drain tunnel junctions ($C_{D,S}$ and $R_{D,S}$) and the gate capacitance (C_G). To properly simulate a vSET which is able to operate at room temperature, we have defined the SET parameters as shown in Table I, by adapting the values to those described in [7]. Note that to ensure the SET's characteristics independence in front of the capacitances of the neighboring devices, we assume that the interconnect capacitances associated with the SET terminals are much larger than the own device capacitances. Then, the total SET island capacitance (C_Σ) will be equal to the summation of the device tunnel capacitances. So, the SET characteristics will be solely dependent on the nodal voltages of the SET terminals. For operation at room temperature, an island capacitance, which is related to its size, below 1 aF is required [7]. Note that the values assumed here and shown in Table I fulfill this condition.

In the case of FETs, we have simulated those that could show the highest level of integration, i.e., the vNW and the FinFET. Both have been simulated by using BSIM models [22], and their dimensions are also listed in Table I,

by using the nominal BSIM values. Nominal FET dimensions have been considered for the simulations; then, for a more fair comparison, the output hybrid SET–FET drive current has been normalized by the FET device area (A/μm^2), obtaining the current density (J) for each circuit configuration. In addition, our studies also provide the amplitude of the Coulomb blockade oscillations, expressed by the h_{ID} parameter ($h_{\mathrm{ID}} = J_{D,\max}/J_{D,\min}$), which describes the contribution of the SET into the whole hybrid circuit current. Another important building block parameter is the current source [I_{BIAS}, Fig. 1(b)]. This element generates a voltage between gate and source terminals to switch ON the FET, which operates in the subthreshold region. The correct I_{BIAS} value is determined by the SET parameters [1]

$$I_{\mathrm{BIAS}} < \frac{e}{10C_{\sum}(\sqrt{R_D}+\sqrt{R_S})^2} \tag{1}$$

where $C_{\sum}$ is the total island capacitance with respect to the ground, and e is the elementary charge. The SET is biased by a constant current source (I_{BIAS}) of 0.16 nA. The design of the current source is not the goal of this contribution. As the SET is biased by a constant current source, the voltage V_D can be higher than $e/C_{\sum}$ [1]; therefore, it is set to 1 V.

B. Variability Influence on the SET–FET Performance

The continuous device scaling of technology nodes has increased the impact of several reliability effects on the electronic devices behavior. In particular, the device variability arises as the most detrimental factor that leads to a reliability reduction. To determine the variability influence on the hybrid SET–FET circuit behavior, we have considered different scenarios: 1) study of the impact of the variation of the SET parameters; 2) analysis of the relevance of both FET configurations on the hybrid circuit performance; and 3) relevance of the environmental conditions (I_{BIAS}, V_D, and temperature) into the SET-based circuits. To do so, 10 000 sample Monte Carlo analyses were carried out per parameter change. For the variability study, the working point is set at $V_G = 0.6$ V, which corresponds to the maximum value of the density current oscillation [Fig. 2(a)]. The impact of variability was modeled by using the corresponding FET parameters into BSIM models, and in the case of the SETs as a shift of the different design parameters ($R_{S,D}$ and $C_{G,S,D}$). Due to the use of an asymmetric SET model, we could study the impact of the QD location and its impact on the SET–FET circuit behavior. The process variation level is arbitrarily defined at a 10% shift of all SET and FET parameters. However, depending on the FET type (FinFET and vNW) [23], [24] and its dimensions [12], a different FET variability level has been considered. The variability impact was evaluated using a statistical distribution with mean (μ) and standard deviation (σ), obtaining the ratio 3 σ/μ (%).

III. Device Variations Influence on SET–FET Circuits

We have analyzed the behavioral impact of process variations into the hybrid SET–FET circuit, e.g., the QD location influence on SET behavior and the FET simulation by vNW or FinFET. As discussed above, the circuit output current has been normalized by the FET area (current density), which would allow a more correct comparison between the different SET–FET configurations. Note that the use of an asymmetric SET's model allows us to simulate the impact of the variation of the QD location.

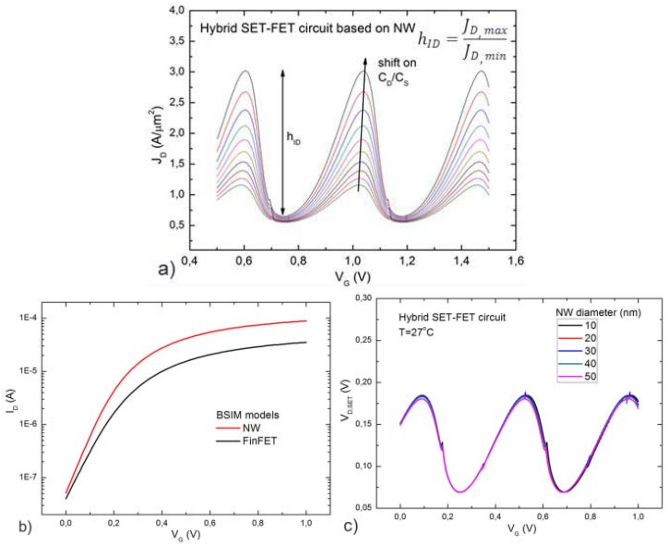

Fig. 2. (a) J_D–V_G curves obtained by varying the C_D/C_S relation, where h_{ID} relation could be observed. (b) I_D–V_G curves of the NW and FinFET devices. (c) Voltage at the drain terminal of the SET device ($V_{D,\mathrm{SET}}$) in the case of a hybrid SET–FET circuit when using an NW FET.

A. Relevance of the SET's Variations in SET–FET Behavior

We have analyzed the impact of the SET variations on the SET–FET circuit behavior, by considering a change in the ratio between the different SET parameters. For instance, Fig. 2(a) shows the J_D–V_G relation when the C_D/C_S is modified. To better understand the performance of the hybrid SET–FET circuit, Fig. 2(b) presents I_D–V_G curves of both FET devices (NW and FinFET). Fig. 2(c) points out the V_D values of the SET ($V_{D,\mathrm{SET}}$) in a normal operation mode of a hybrid SET–FET circuit as a function of NW diameter, showing the operation of the FET device at subthreshold level.

Then, we have studied the relevance of a change in the ratio between the SET resistance values R_S and R_D. This modification can be related to the manufactured SET pillar (e.g., dimensions, doping, and contact location) and to the QD location, simulated by using asymmetric SET. Thus, Fig. 3(a) shows a larger current density for the vNW-based SET FET in comparison with the FinFET-based one. Note that, the threshold voltage of both FET devices has been normalized too. Furthermore, for both cases, as larger R_S values are defined the current density continuously increases. This increase is larger for the NW-based circuits (2×) than for the FinFET ones (1.4×), which could be related to the better conduction of the NW in comparison with the FinFET. While a slight h_{ID} parameter modification is observed for the FinFET, negligible change is obtained for the NW-based hybrid circuit.

The QD location into the device channel region (e.g., thin SiO_2 layer) has also been explored as a source of SET behavior

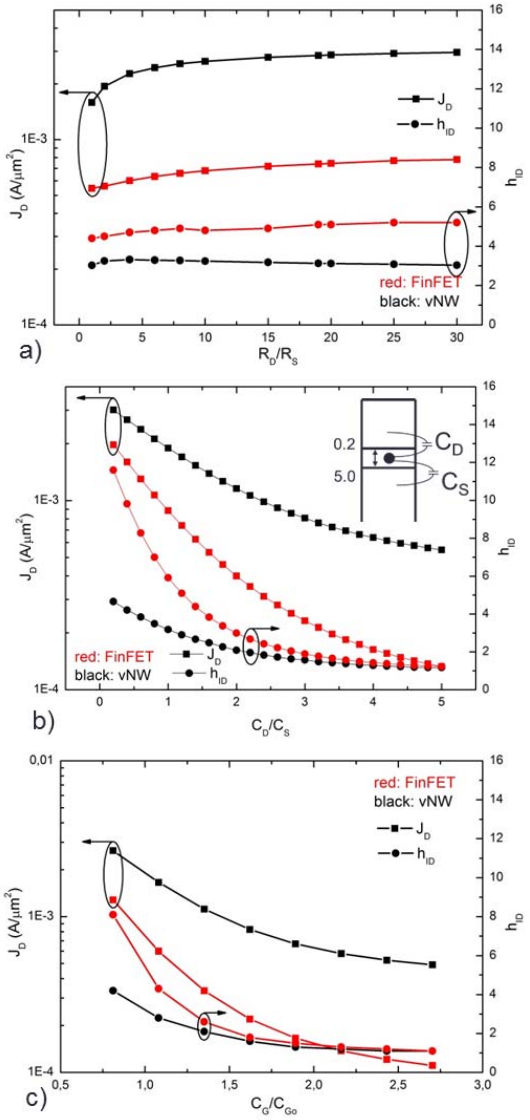

Fig. 3. Influence of (a) R_D/R_S, (b) C_D/C_S ratios, and (c) C_G/C_{GO} relation on J_D values for SET FET based on vNW and FinFETs.

variation, by using the asymmetric Inokawa SET's model. To do this, the ratio between source and drain capacitances has been modified by a factor 'x' which determines the QD location in the channel region [inset Fig. 3(b)]. The range of values has been changed from 0.2 (QD close to the drain region) to 5 (QD located near the source), keeping constant C_D and modifying C_S. Then, as seen in Fig. 3(b), a lower influence of the QD location for the NW-based SET FET is observed, as the current density (square) shrinks 5.5×, while the current density for the FinFET is reduced 15×. For the h_{ID} parameter, higher values and larger relevance are observed for the FinFET-based configuration (9×) as compared to the NW one (4×). So, a larger influence of the SET is observed on the hybrid circuit based on FinFETs, which can be related to a lower current level for this configuration.

Finally, the relevance of the gate capacitance (C_G) into the hybrid circuit performance has also been analyzed. Fig. 3(c) shows again how the NW-based circuits present the largest drive current and the lowest h_{ID} relation, expressing the higher impact of the NW current over the whole SET–FET

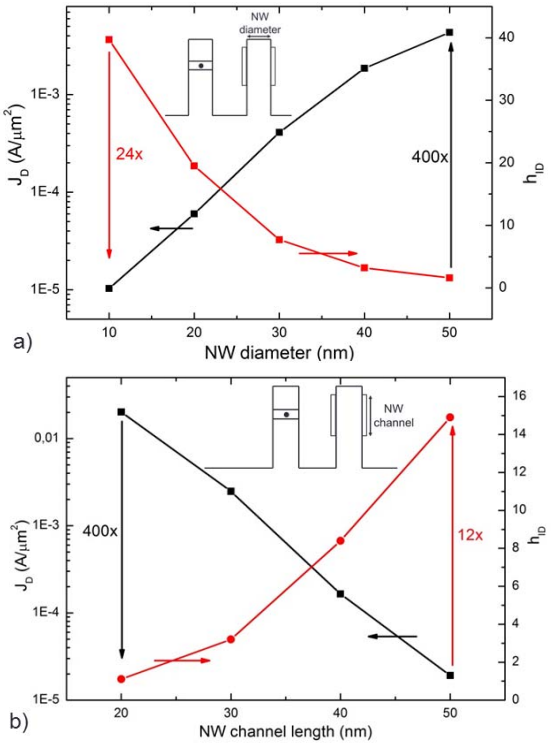

Fig. 4. Impact of the variation of vertical NW parameters, e.g., (a) diameter and (b) channel length on J_D and h_{ID} of a hybrid SET-NW circuit.

circuit behavior. While the NW-based configuration shows a reduction of the current density (5.5×) for larger C_G/C_{GO} relation, the FinFET's current density reduces by 11.5×. The h_{ID} for the FinFET configuration shows a higher reduction than the vNW case (8× and 4×, respectively). In general, the C_G value appears to be more relevant over the hybrid SET–FET circuit behavior, than the observed for the $C_{D,S}$ variation, as higher influence on the circuit performance is obtained.

B. Impact of NW Dimension Variations in SET–FET Behavior

The variation of the FET dimensions could also involve an influence on the hybrid circuit performance. So, we have analyzed how the variations of the vNW dimensions, e.g., NW diameter and channel length, affect the overall SET–FET behavior. The insets in Fig. 4 describe the NW parameters that are varied. Fig. 4(a) analyzes the impact of the diameter variation, and Fig. 4(b) studies the influence of the NW channel length modification. Note that larger NW diameter involves larger width of the FETs. So, Fig. 4(a) points out that larger NW diameter involve higher current density of the SET FET (400×). In contrast, the h_{ID} value reduces significantly (24×), showing the larger relevance of the NW current component in comparison with the SET one. Concerning the NW channel length, Fig. 4(b) depicts the opposite behavior: for larger channel lengths the current density is lower. Equally for the h_{ID} parameter, i.e., the larger the channel length, the higher the h_{ID} ratio (12×). The larger (smaller) is the NW diameter, the lower (higher) is the influence of the NW into the overall hybrid SET–FET circuit performance.

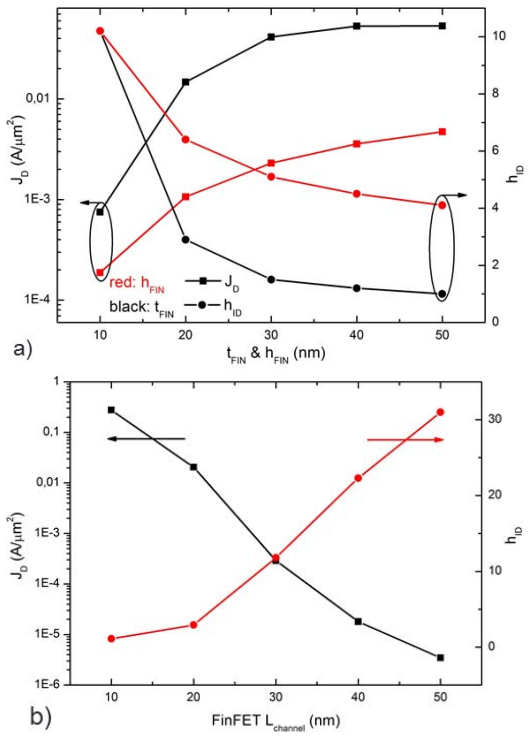

Fig. 5. Impact of the variation of FinFET parameters. (a) Fin topology and (b) channel length on J_D and the h_{ID} ratio of a hybrid SET–FET circuit.

C. FinFET Variations Relevance in the SET–FET Behavior

In the case of the SET–FET circuits based on FinFETs, the modified FET parameters have been the fin topology [Fig. 5(a)], e.g., height, thickness, and the channel length [Fig. 5(b)]. Again, the baseline SET device is used and we have not modified it for this aspect of this paper, to observe the impact of the FinFET variations. Larger values of the fin topology parameters have involved larger FinFET width. Fig. 5(a) points out that larger current density of the SET FET is observed (200×) for larger FinFET widths. In contrast, the h_{ID} value is significantly reduced (5×), which means a larger influence on the overall hybrid circuit current of the FET in comparison with the SET. Regarding the FinFET channel length, Fig. 5(b) shows that for larger channel lengths the current density is significantly lower. In the case of the h_{ID}, the larger channel length entails a larger h_{ID} ratio (30×). Larger FinFET topology (t_{FIN} and h_{FIN}) entails lower influence into the overall SET–FET circuit; in contrast, smaller channel shows higher influence on the hybrid circuit.

IV. Variability Relevance on SET–FET Behavior

Process variability has become one of the main reliability problems which affects all the electronic devices when their dimensions scale to tens of nanometer (<32 nm). Few studies have analyzed the impact of SET variations. For instance, a previous study [25] investigated the variability impact on the SET–FET behavior pointing out that the dopants in the S/D junctions as the main source of SET variation. Thus, in this section, we describe a more detailed analysis of the influence of the device variability on the hybrid circuit performance.

A. Variability Relevance on a Single Asymmetric SET

We have studied the influence of the device variability solely related to the variation in a single asymmetric SET at room temperature. First, a 10% variation is independently defined to the SET parameters ($R_{S,D}$ and $C_{G,S,D}$) and the BCN, all modeled as mentioned in Section II. Then, the effect of the variation of all parameters simultaneously (global) has been studied. Fig. 6(a) depicts the variation of the output current of the SET FET. While the highest impact on SET–FET variability comes from the gate capacitance and BCN, the lowest influence is observed for the source and drain resistances. Regarding the C_G variation, it could come from different sources, e.g., QD location. Note that a relevant impact of BCN has been observed, but their influence can be minimized by using better silicon islands (less trapped charge) or specific circuits. Analysis of the other parameters shows that the variability produced at the source region of the SET appears slightly more detrimental than that produced at the drain region, which can be more specifically related to the change to use an asymmetric SET.

B. Impact of External Parameters Variability on SET FET

External parameters, mainly temperature and voltage, always entail a relevant impact on every electronic circuit. In the case of the SET–FET circuits, this influence could be even more relevant as the SET is highly sensitive to these variations, and the FET operates in the subthreshold level, which makes it weaker against variability. So, in this section, we have solely regarded the influence of the variation of the experimental conditions (i.e., I_{BIAS}, V_D, and temperature). The baseline circuit for this analysis has been selected as an NW-based hybrid SET–FET circuit at room temperature. A 10% variation on the main external parameters has been considered. Fig. 6(b) shows the variation on the current density of the hybrid circuit regarding individual parameter variation scenarios and when all together are considered (global). While the lowest impact on the overall device behavior is observed by the I_{BIAS} parameter, the highest impact is obtained for the environment temperature, which can be related to the significant impact of the thermal energy on electron tunneling of the SET device and the FET subthreshold level operation, where FETs are highly sensitive to temperature variations at this working regime. Note that similar impact is observed for hybrid SET FET based on symmetric SETs [20].

C. Variability Impact of Both SET and FET Into the Whole Hybrid SET–FET Circuit

Next, we investigate the individual variability contribution of both devices (SET and FET) into the whole hybrid vSET–FET behavior. A 10% shift of the FET and SET parameters is considered. FETs are simulated by using the two analyzed types (FinFET and NW). In general, for both studied cases, Fig. 6(c) presents the variability contribution of the FET with the lowest impact on the overall hybrid circuit variability. So, the largest variability contribution is the one produced by the asymmetric SET. The NW-based configuration presents

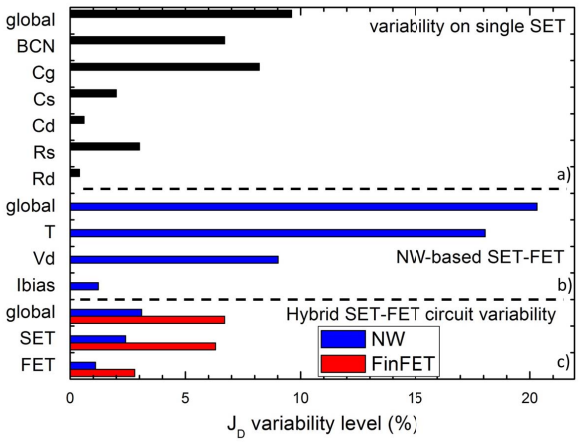

Fig. 6. Impact of the different device variability scenarios at room temperature. (a) When the BCN and asymmetric SET parameters ($R_{D,S}$ and $C_{D,S,G}$) are individually considered. (b) Environmental conditions (I_{BIAS}, V_D, and T) variability. (c) When both SET and FET variability contribution are taken into account within the SET–FET behavior.

the lowest level of variability in comparison with the FinFET one, but both cases show a variability level lower than 10%. In comparison with a previous SET–FET study [20] based on a symmetric SET, a higher level of variability is obtained, and this can be related to the significantly smaller SET parameter values. Note that the FETs present the lowest variability level, but in relation of the use of the proposed FET, the NW is the one that presents the lowest variability level.

V. Other SET-Based Circuits' Proposals

Besides the hybrid SET–FET configuration, there are other SET-based circuits that present interesting and useful functionalities. The main ones are the negative differential resistance (NDR) [10] and the SET-based logic inverter [7], [26]. For both cases, the relevance of the use of vNW and FinFET has been analyzed.

A. Relevance of NDR Implementation With NW and FinFET

An NDR is an element with a wide variety of circuit applications such as oscillators, amplifiers, logic cells, and memories. The NDR characteristics are obtained only for a limited range of values of V_D. The dotted line that shorts the SET's gate terminal and drain's FET terminal on Fig. 1(b) depicts the change to be made on the hybrid SET–FET circuit. The NDR circuit behavior can be explained by the fact that the bias current source and the SET create a feedback loop that decreases the gate-to-source voltage of the FET for a certain range of increasing V_D, and from that a decrease in the drain current follows. In this section, we are interested in analyzing the relevance to use NW and FinFET as an FET together with an asymmetric SET into the NDR performance at room temperature. An intrinsic parameter used to compare different circuits is the peak-to-valley current ratio (PVR), the ratio of the current at the top of the negative resistance region to the current at the bottom. Fig. 7(a) shows the NDR behavior of both NW and FinFET-based configurations. The FinFET one presents the lower current density, but the highest

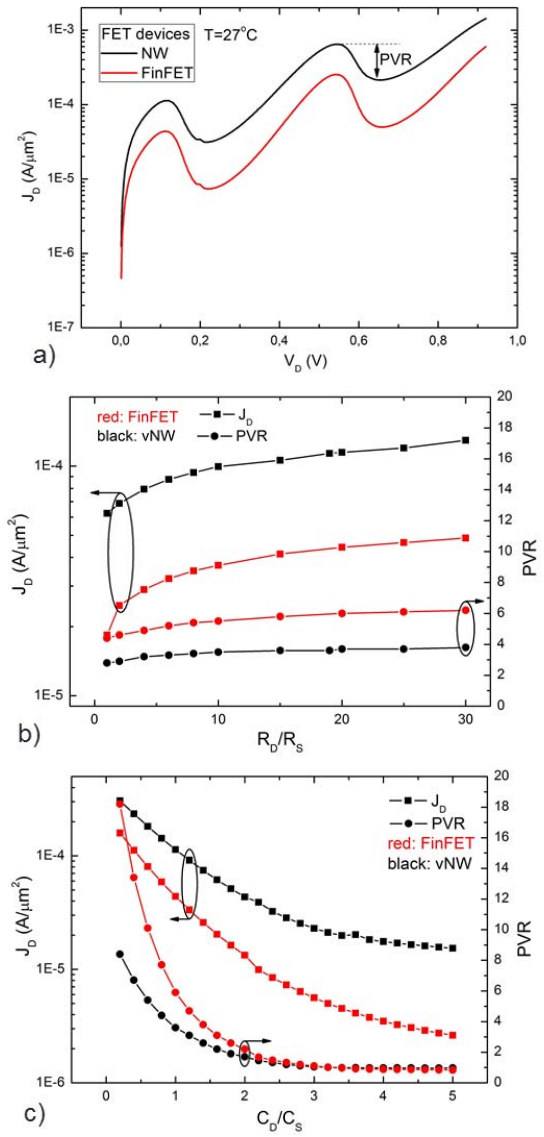

Fig. 7. (a) NDR characteristics when the circuit is based on NW and FinFET, larger PVR is obtained for the FinFET configuration. Relevance of (b) R_D/R_S and (c) C_D/C_S relations on J_D and PVR values for hybrid SET FET based on vertical NW and FinFETs.

PVR value (15), in comparison with a PVR of 3 for the NW-based NDR circuit. In relation of the use of the asymmetric SET model, we are able to analyze the influence of the QD variations into both NDR performances; e.g., R_D/R_S relation [Fig. 7(b)] and C_D/C_S relation [Fig. 7(c)]. While for all cases the NW-based NDR presents the largest current density values, the FinFET configuration depicts the highest PVR values. In the case of the R_D/R_S study, the larger the ratio is, the higher are the current and PVR values. Regarding the C_D/C_S ratio, as the QD is closer to the drain region the current density and the PVR are larger. In comparison with previous NDR studies [10], our results provide larger PVR values for asymmetric SET-based circuits, able to be operative at room temperature, due to the use of FET devices with lower leakage current level.

Furthermore, the impact of both devices variability (FET and SET) has also been analyzed in an NDR circuit. Fig. 8 points out the current density variability when the NDR is

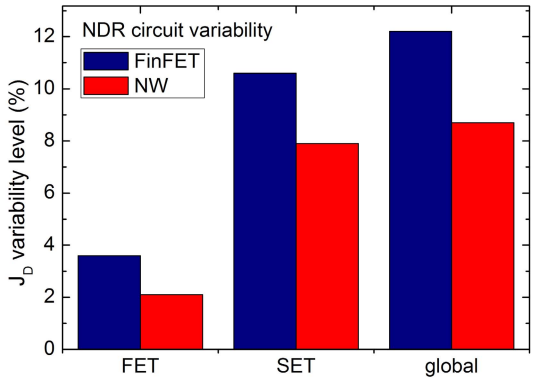

Fig. 8. Device variability relevance at room temperature, when both SET and FET variabilities are taken into account within the entire NDR behavior.

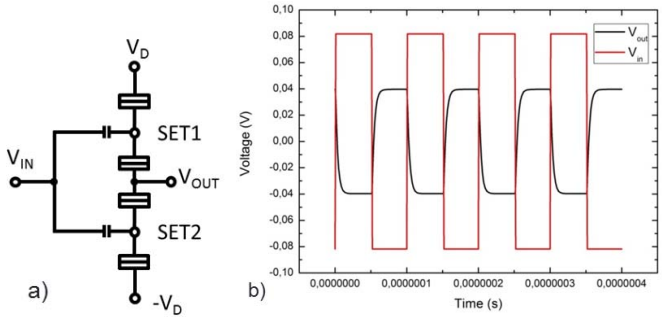

Fig. 9. (a) Schematic configuration for an SET-based inverter. (b) Transient characteristics for a logic inverter based on SET devices at room temperature.

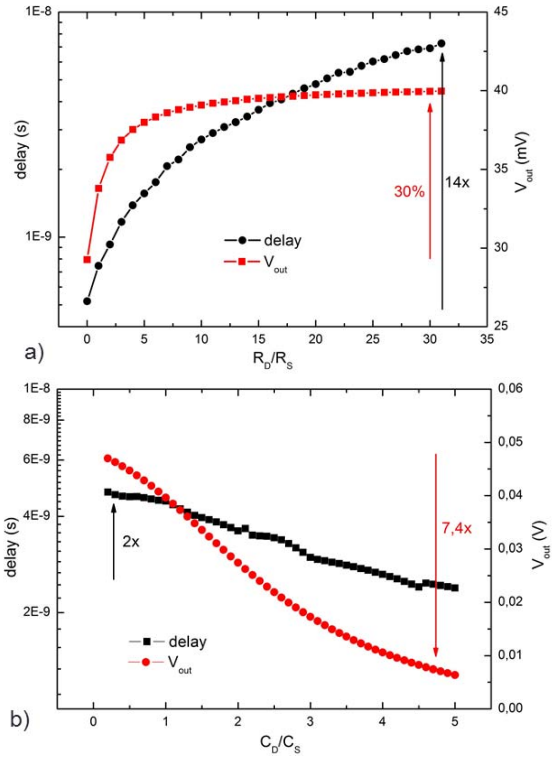

Fig. 10. Relevance of (a) R_D/R_S and (b) C_D/C_S ratios on the inverter delay and output voltage (V_{out}) values for an SET-based logic inverter.

based on FinFET and NW. Similar to the hybrid SET–FET circuit, for this paper, a 10% variation on the asymmetric SET and FET devices parameters is considered for both FETs-based

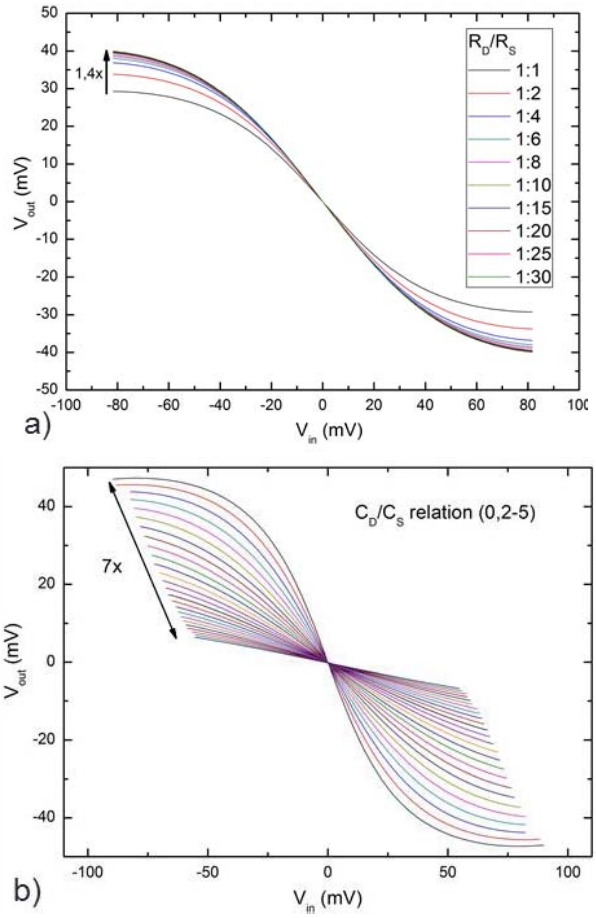

Fig. 11. Influence of (a) R_D/R_S and (b) C_D/C_S ratios on V_{out}/V_{in} characteristics for an SET-based logic inverter.

hybrid circuits. A larger level of variability is obtained for the FinFET-based NDR configuration, as it was expected from the previous results (Fig. 6). But, note that a larger variability level is slightly observed for both NDR options in comparison with both SET–FET hybrid circuits.

B. Logic Inverter Implementation Based on SETs

SETs are suitable devices to implement logic circuits, e.g., inverter or memory cells. In this section, we will focus on the simulation of an SET-based inverter. First, we note that in contrast to the CMOS-based logic inverter, the SET-based one [Fig. 10(a)] is composed by two identical SETs [26]. Other characteristics of this inverter are: 1) their low inverter gain mainly determined by the C_G/C_T ratio, where $C_T = C_D = C_S$ and 2) the power dissipation in SET logic is mainly dominated by static power dissipation. It has been observed that the use of asymmetric SET configurations could involve a reduction of power dissipation [26]. When we define the SET-based inverter, we use again asymmetric SETs operating at room temperature. The input voltage (V_{in}) is switched between high and low values ($\pm V_D$, respectively). The V_D values that supply the logic inverter are based on [26]

$$V_D = \pm \frac{e}{2(C_G + C_T)} \tag{2}$$

Fig. 9(b) shows the transient characteristics for the logic inverter when it is based on asymmetric SETs operating at room temperature.

The process variations on the SET manufacture would also affect the overall logic inverter behavior. In this sense, Fig. 10 depicts how the variations on R_D/R_S and C_D/C_S ratios, introduced by using the asymmetric SET model, could impact on the SET-based inverter. For this, the analyzed parameters have been the inverter delay and the voltage at the inverter output (V_{out}). Fig. 10(a) presents the impact of the variation of the R_D and R_S ratio, and while a continuous increase of the output voltage is observed as a function of the R_S/R_D ratio variation, a saturation of the delay increase is observed as the ratio shifts 14×. Furthermore, in Fig. 10(b), we have analyzed the C_D and C_S ratio, and the same tendency has been obtained for the delay and output voltage of the SET-based inverter. A larger (smaller) delay increase has been obtained when the QD is shifted to the drain (source) side.

Finally, the static characteristics ($V_{\text{out}}/V_{\text{in}}$ ratio) of the SET-based inverter have been also studied. Fig. 11 presents the variation influence, due to the (a) R_D/R_S and (b) C_D/C_S ratios. Regarding a variation on the ratio between the SET resistances, an increase of 1.4× is observed on the static characteristic, as shown in Fig. 11(a). When the SET asymmetry is larger, the SET inverter gain is higher. Fig. 11(b) considers the QD location as a shift in the C_D/C_S ratio, and in this case a relevant variation (7×) into the SET inverter gain is observed, as well.

VI. Conclusion

We have analyzed the variability impact on different SET-based circuits (SET–FET, NDR, and logic inverter) when they are designed to operate at room temperature. The use of different FET configurations (vNW and FinFET) to implement hybrid SET–FET and an NDR circuits has also been studied. The process variations on both SET (QD location) and FET (dimensions) device and parameters have been considered. The NW-based SET–FET circuit provides the highest level of current density. When the variability of both FET and SET is introduced, the larger contribution is supplied by the SET. In terms of variability of a single SET, the SET capacitances present the highest impact on the device performance. The operative temperature arises as the most relevant of the external conditions (I_{BIAS}, V_D, and T). For the NDR circuit, the largest gain is observed for the FinFET-based circuit. The NW-based FET is proposed as the most suitable option to implement an SET–FET circuit, due to the larger drive current, higher level of integration, and the lowest level of device variability.

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