High-R Poly Resistance Deviation Improvement From Suppressions of Back-End Mechanical Stresses

Tingyou Lin, Yingchieh Ho, *Member, IEEE*, and Chauchin Su, *Member, IEEE*

***Abstract*— This paper investigates techniques for N-type high-resistance polysilicon resistors to reduce the resistance deviation which is caused by the back-end mechanical stress. In the back-end layers of the wafer, a top metal thickness equal to 3 μm is provided to increase the heat allowing current density in the metal routes of power ICs. The top metal processing yields the mechanical stress to increase the resistance by the piezoresistance effect. To eliminate the mechanical stresses, a new layout is proposed with the full passivation cutting (FPC). The resistor with an FPC uses the passivation film separation to create a physical empty room for suppressing the mechanical stresses on the polysilicon. The proposed layout has been verified in the 0.4-μm bipolar-CMOS-DMOS process, and the resistance shifts were compared with other four-type layouts. Compared to those original layouts, the proposed layout exhibits the improvements in the resistance deviation reduction in the maximum ratio 20.80%.**

***Index Terms*— Full passivation cutting (FPC), mechanical stress, N-type high resistance (high-R) polysilicon (NHRPO).**

I. Introduction

IN THE modern semiconductor industry, the smart power integrated circuit (SPIC) integrates passive and high-voltage MOSFET transistors with a large thickness of the top metal layer. Decreasing the number of metal layers and increasing the thickness of top metal layer is commonly applied to reduce the cost and allow a higher current density in power chips. The resistor, one of the most basic form of passive devices, is applied in analog circuits, those associated with filters, bandgap voltage references, amplifiers, digital to analog, and analog to digital converters [1]–[4].

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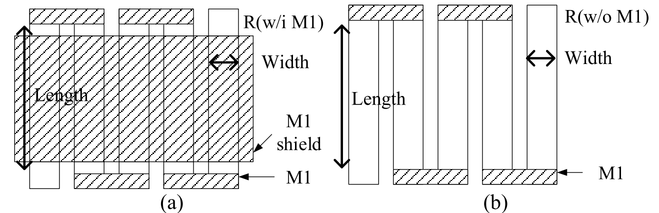

Fig. 1. General resistor layout diagrams of (a) with M1 coverage and (b) without M1 coverage.

However, a resistance deviation in the integrated resistor is inevitable because the piezoresistance effect related to mechanical stresses from the processing and thermal expansion of the back-end layers adversely affects the design cycle. Hence, it is critical to reducing the back-end related resistance deviation for accurately integrated resistors.

Fig. 1 shows the general resistor layouts, where the series resistors in Fig. 1(a) and (b) were connected by metal one (M1) layer and covered with or without covering M1, respectively. Some studies of mismatch improvements, resistance modifications, and resistor modelings have been published for high-valued poly resistors. Among the above studies, the poly resistor layout achieves mismatch of less than 1%, which is sized with the effective poly width W_{eff} less than the minimal poly width $W_{\min}$ and the effective poly length L_{eff} great than or equal to $5 \times W_{\mathrm{eff}}$ have been recommended [5]–[8]. Dimension variations of $\pm 20\% \times W_{\min}/W_{\mathrm{eff}}$ are used to demonstrate the resistance mismatch for the polysilicon resistor [9]–[12]. However, the resistance deviation is not often discussed. Table I lists the status quo and available techniques for resistor implementation. The resistance can be varied by 20% during the processing of ICs [13]. Here, the resistor trimming techniques are used to modify the resistance; a large die area is necessary for the trimming by numerous Zener diodes, resistor fingers, pads, or fuses if there is a possibility of large resistance deviation [14]. The area overhead is required for those resistor trimming techniques. In addition, the resistivity can be modified in the pulse current and the doping polysilicon, which can change the temperature coefficient and voltage coefficient of resistances [14], [15]. Thus, the design resistor is not matched to the simulation model.

For the SPICs, a poly resistor is manufactured on the silicon wafer and processed in the back-end layers. Here, a stress effect is verified in the silicon under the metal coverage [16].

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TABLE I
COMPARISON OF ACCURATELY RESISTOR DESIGN

Methods	Maker	Accuracy	Size	Time	Complex
Model tuning	Foundry	Good	Small	Long	High
Low deposition intensity	Foundry	-	Small	Long	High
Low-R resistor	Designer	Good	Large	Short	Low
Resistance tuning	Designer	High	Large	Middle	Middle
External resistor	Designer	Better	-	Short	Low

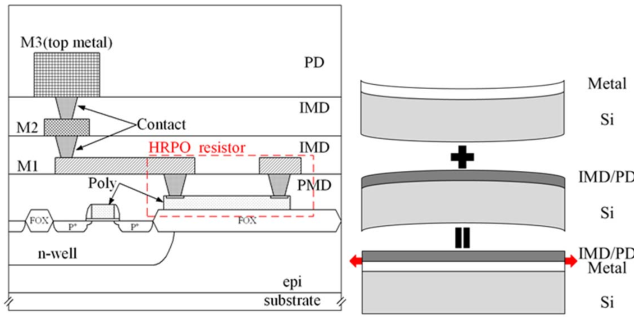

Fig. 2. Cross-sectional view of an HRPO resistor in an end-of-line wafer and the schematic of the films deposition stress and warp.

The piezoresistance effect is related to the mechanical stress and involves a change in the resistance. It has been exploited to estimate the mechanical stress from the changes in the resistivity [17]–[19]. However, the impacts in all back-end layers are not discussed. A standard wafer cross section including the layers of silicon, polysilicon (Poly), premetal dielectric, metals, intermetal dielectric, and passivation dielectric are depicted as in the left of Fig. 2. There are many thin films with internal stresses in back-end layers. As the thin films of metal are sputtered or the dielectrics are deposited on the silicon wafer, they warped the wafer in contrast as shown in the right of Fig. 2 [20]. In both films, the warp is canceled as displayed at the bottom of Fig. 2. However, the stress is retained, changing the resistivity of the silicon and polysilicon under the back-end layers, especially the high-resistance (high-R) resistors. Moreover, it is predicted to impact on the resistance deviation as the different metal layers and top metal thickness.

Since high-accuracy integrated resistors are important for high-end products, the resistance deviation must be concerned. Thus, the cost of the engineering try-error times needs to be reduced. To study the back-end related resistance deviation, this paper presents five-type layouts under different back-end wafers and step by step. To reduce the resistance deviation, this paper presents a new layout of the N-type high-R polysilicon (NHRPO) resistor that allows the back-end layer change with an appropriate top metal layer thickness. The experimental resistor has the full passivation cutting (FPC) coverage in a thickness of 3 μm of the top metal layer on the NHRPO resistor. NHRPO resistor with an FPC (RFPC, proposed) includes an empty space to reduce the mechanical stress. Other layouts of NHRPO resistor are designed to compare the resistance deviation including a passivation-ring cutting (RPRC), a passivation and all-metals coverage (RPAM), a passivation and metal-one coverage (RPM1, typical), and a passivation coverage (RP) layouts.

The rest of this paper is organized as follows. Section II analyzes the influence of back-end processes on the poly resistor accuracy. Section III introduces five-type layouts of NHRPO resistor in wafers with a thick top metal layer of 3 μm and the use of the proposed stress separation method to suppress the resistance deviation from the new layout structure with an FPC. Section IV presents experimental results of five-type resistor layouts and compares the cross-sectional view of the proposed RFPC and the typical RPM1. Finally, Section V draws conclusions.

II. PROCESS-BASED RESISTOR VARIATIONS

Fig. 2 shows a poly resistor that is fabricated using a bipolar-CMOS-DMOS (BCD) process. Process variations are included the dimension, doping concentration, and internal stress. The mechanical stress affected resistance is mainly in the back-end layers if the errors from the dimension and doping concentration are small. Usually, a thick top metal layer of 3 μm is replace a thin top metal layer of 0.8 μm to increase the allowable current density. In our previous studies, the processes of passivation layer are responsible for the most of the influence affects the resistance and that can be reduced the resistance deviation by covered in metal. To reduce the resistance deviation, the resistor coverage with different metal structures and removing the passivation film are considered. A new layout of NHRPO RFPC is introduced, and it is manufactured in the wafer with a thick top metal layer of 3 μm to measure the resistance deviation.

In back-end processes, many steps are optional and customized to the number of metal layers and the thickness of the top metal layer. In Fig. 2, only shows three metals, it will mismatch with the changed of "four" metal layers includes metal sputtering, dielectric deposition, 0.8-μm top metal sputtering, and passivation deposition with the spin-on-glass planarization. The dielectrics and passivation layers are deposited by plasma-enhanced chemical vapor deposition. To meet the high-current density, the top metal layer is sputtered to a thickness of 3 μm. A thicker passivation film needs to deposit by the high-density plasma chemical vapor deposition to fill the deep gaps and plenaries it using the chemical mechanical planarization method. Thus, the back-end layers cause varying stresses on the wafer. The piezoresistance terms are modeled for integrating the poly/silicon resistor [16]

$$\frac{\Delta R}{R} = \frac{(\pi_{11}+\pi_{12}+\pi_{44})}{2}\cdot\sigma_{XX} + \frac{(\pi_{11}+\pi_{12}-\pi_{44})}{2}\cdot\sigma_{YY} + \pi_{12}\cdot\sigma_{ZZ}. \quad (1)$$

If the resistors in the poly/silicon are not covered by the metal, then the resistance deviation can be modeled as

$$\frac{\Delta R_{\mathrm{RP}}}{R_{\mathrm{RP}}} = (\pi_{11}+\pi_{12})\cdot\sigma_{\mathrm{RP}}. \quad (2)$$

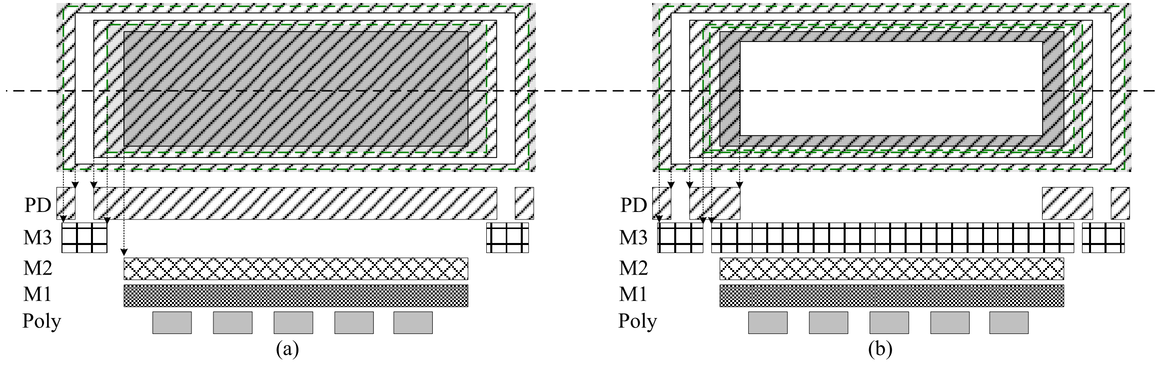

Fig. 3. Top view and cross section of the proposed structures of (a) RPRC and (b) RFPC in 2P3M thick wafer.

The resistance deviation of an N-type resistor with the metal coverage can be derived as

$$\frac{\Delta R_{\mathrm{RPM1}}}{R_{\mathrm{RPM1}}} = \frac{\pi_{11}+\pi_{12}}{2}\cdot\left(\sigma_{XX,\mathrm{RPM1}}+\sigma_{YY,\mathrm{RPM1}}\right). \quad (3)$$

Here, the piezoresistance tensor of π_{11}, π_{12}, and π_{44} of the resistor had mutually independent components and depended on the wafer manufacturing. They are related to the crystallographic direction and material. The passivation stress tensor of σ_{RP} and σ_{RPM1} changes as the back-end layer shapes. σ_{RP} is the tensor of the resistor only covering the passivation film and σ_{RPM1} is covered with M1 and passivation.

Owing to the mechanical stress that is generated in back-end layers to affect the polysilicon or silicon devices in the front-end process. Equation (3) models the resistance deviation of the integrated poly resistor. Based on a 2-polysilicons-4-metals (2P4M) 0.4-μm high-voltage BCD technology, an NHRPO resistor uses the layer of polysilicon-2 (PO2), which is an N-type doping nonsilicide polysilicon. The series resistor consists of 20 multifingers, each resistor finger with $W = 2\ \mu$m and $L = 10\ \mu$m, and has a sheet resistance of 3 kΩ/sq. Both in Fig. 1(a) and (b), the resistors have a passivation film on the top of wafers.

To model a resistance with back-end considerations, it is complicated for the mechanical stress change behavior to change the resistivity of the polysilicon/silicon. The change in resistance is a function of the stress and piezoresistance tensor in (1), which is proportional to the mechanical stress. The wafer with a thin top metal layer of 0.8 μm has a different total stress from that with a thick top metal layer of 3 μm. In this paper, the sheet resistance of 3 kΩ/sq of RPM1 is normalized to 0% ($\Delta R_0/R_0 = 0$) of resistance deviation in the wafers with a thin top metal layer of 0.8 μm as the baseline. In the manufacture of back-end layers, the end of stresses in those thin films are modeled as

$$\sigma_{\mathrm{RPM1},0.8\mu m} = \frac{P_{m1}+P_d+P_{p,0.8\mu m}}{\mathrm{A}} \approx \sigma_{p,0.8\mu m}+\sigma_{m1} \quad (4)$$

where $\sigma_{\mathrm{RPM1},0.8\mu m} = \sigma_0$ is the normalized stress in the wafer with a thin top metal layer of 0.8 μm, P is the force that acts on the vertical surface, and A is the area to which the force is applied. At $\sigma_0 = 0$, they are the inverse stresses between metal and passivation layers, thus $\sigma_{p,0.8\mu m} \approx -\sigma_{m1}$. Based on (2) and (4), the resistor RP has stressed

$$\sigma_{\mathrm{RP},0.8\mu m} = \sigma_0 - \sigma_{m1} \approx \sigma_{p,0.8\mu m}. \quad (5)$$

The stress in RP changes the total stress to $\sigma_{\mathrm{RP},0.8\mu m} \approx \sigma_{p,0.8\mu m}$ for the NHRPO RPM1. Moreover, the stress for the resistor in wafer with a thick top metal layer of 3 μm is given by

$$\sigma_{\mathrm{RPM1},3\mu m} = \sigma_0 - \sigma_{p,0.8\mu m} + \sigma_{p,3\mu m} \approx \sigma_{p,3\mu m} - \sigma_{p,0.8\mu m} \quad (6)$$

and the resistor RP is

$$\sigma_{\mathrm{RP},3\mu m} = \sigma_{p,3\mu m} - \sigma_{p,0.8\mu m} - \sigma_{m1} \approx \sigma_{p,3\mu m}. \quad (7)$$

The above discussion can be summarized as follows. The resistance deviation is $|\Delta R_{3\mu m}| > |\Delta R_{0.8\mu m}|$, $|\Delta \mathrm{RP}_{3\mu m}| > |\Delta \mathrm{RPM1}_{3\mu m}|$, and $|\Delta \mathrm{RP}_{0.8\mu m}| > |\Delta \mathrm{RPM1}_{0.8\mu m}|$, if $\sigma_{p,3\mu m}$ is larger than $\sigma_{p,0.8\mu m}$ for the wafers with 3- or 0.8-μm top metal. Thus, the resistance deviation is worse for using 3-μm layer, and the stress is from the passivation layer.

III. NHRPO Resistor With Passivation Cut

A passivation layer is an outer layer that is made of a shield material, such as metal oxide or silicon oxide. It is formed by a chemical reaction. After the passivation process, the stress is generated to change the resistance error. To reduce the resistance deviation, two resistor layouts with passivation cut methods are proposed in this paper. Comparisons with others three types only changing the metal layers are shown in the section as well.

One of the proposed resistor with a passivation ring cutting removes the passivation area, which surrounding the resistor, as shown in Fig. 3(a). The other one is the RFPC to reduce the stress from the passivation layer, as shown in Fig. 3(b). They cover the metals and remove the specific passivation areas to create an empty space for the stress from the passivation layer. The white areas in Fig. 4 are removed to separate the stress from the full passivation film and put M3 metal areas at the removed region for reliability. The filled metal is used to prevent the corrosion by water and oxidation of silicon.

The resistors of the proposed RPRC and RFPC are compared with other three-type layouts of RPM1, RP, and RPAM. Five-type layouts of NHRPO resistor are designed, as shown in Fig. 4. The experiments of mechanical stress-related resistance

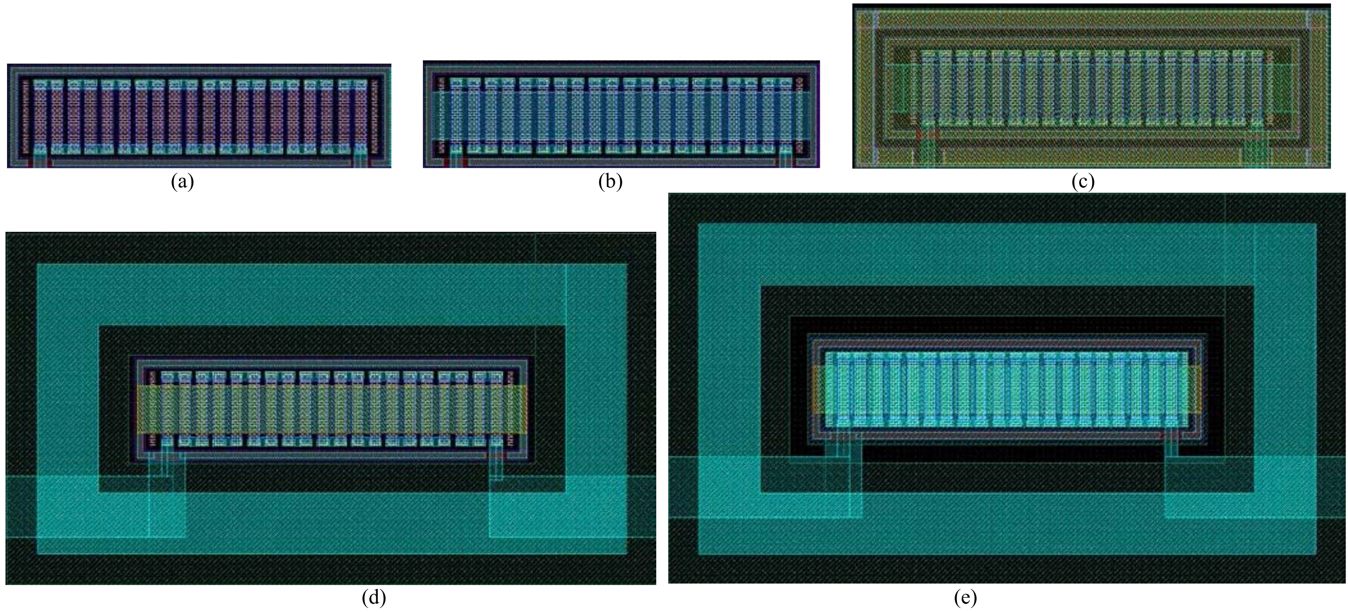

Fig. 4. NHRPO resistor test structures. (a) RPM1. (b) RP. (c) RPAM. (d) RPRC. (e) RFPC.

TABLE II
WAFER CONDITIONS

wafer	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Process	2P3M	2P3M	2P2M	2P2M	2P3M	2P3M	2P3M	2P4M	2P4M	2P4M
Top metal thickness	0.8μm	0.8μm	3μm	3μm	3μm	3μm	3μm	3μm	3μm	3μm
Nr. of samples	62	62	62	62	62	62	62	62	62	62

deviation and the verification of the passivation cut methods are as follows. These resistors are manufactured to 2PxM wafers, which have a sheet resistance of 3 kΩ/sq, a top metal thickness of 0.8 or 3 μm, and two to four metal layers. In the experiments, the resistance was measured and used to obtain a sheet resistance (R_S). The resistance is defined as $R = V_R/I_R$, measured at $V_R = 5$ V. The resistance deviation of the NHRPO resistor is defined as a ratio of $(R_{S,\text{Meas}} - R_{S,\text{Model}})/R_{S,\text{Model}}$.

IV. RESULTS AND DISCUSSION

In this section, several experiments have been designed to verify the effects of back-end mechanical stress-related resistance deviation on five-type layouts of NHRPO resistor. All the wafers for verification are fabricated in 0.4-μm BCD technology. To verify the resistance consistency, two or three wafers are measured with each back-end condition. All the wafer-testing conditions are listed in Table II. The resistors are placed on a 22-pin test-line pattern. The probing layout is shown in Fig. 5, which is for wafer acceptance test machine with the 22-pin probing. Based on the experiments, the wafer mapping results are used to analyze the resistance error related to the back-end layers, then yielding the average resistance deviation (MEAN) and standard deviation (StDev). The mapping results are obtained in the 2P2M, 2P3M, and 2P4M wafers with 0.8 or 3-μm top metal layer. The five-type

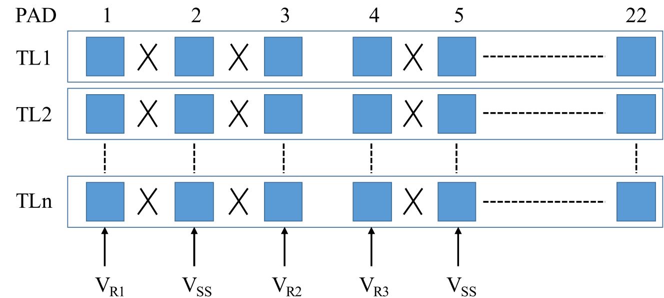

Fig. 5. Layout for 22-pin probing.

layouts of NHRPO resistor in Section III were designed and measured. The detailed experiments of the resistance deviation related to back-end layers are expressed as five parts as follows:

1) the resistance deviation of RPM1 and RP in 0.8- and 3-μm thickness of top metal layer processing;
2) the resistance deviation of five-type layouts in the processing of multilayer metals;
3) the resistance deviation of RPM1 and an FPC resistors in geometries of resistor length;
4) the temperature coefficient of RPM1 and fully passivation cutting resistors;
5) the discussion of mechanical stress-related resistance deviations.

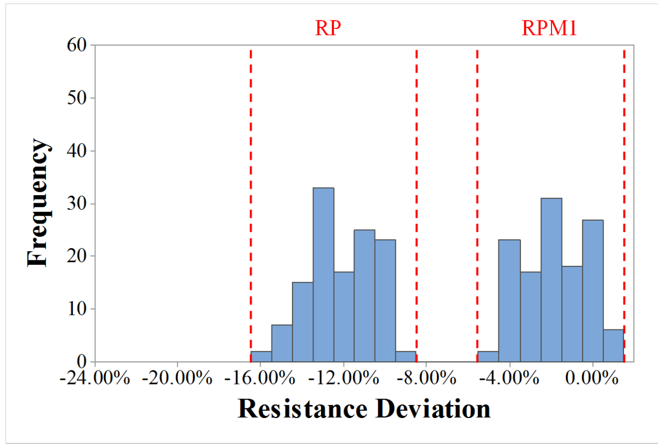

Fig. 6. Histogram of resistance deviations of the N-type HRPO resistor (289 kΩ, $Rs = 3$ kΩ) in 2P3M 0.8-μm top metal wafers.

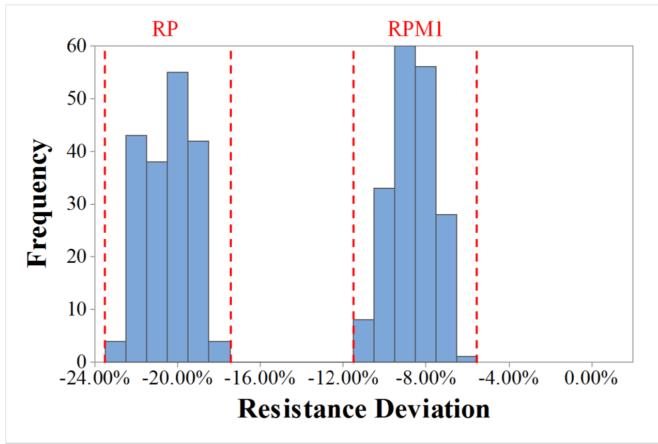

Fig. 7. Histogram of resistance deviations of the N-type HRPO resistor (289 kΩ, $Rs = 3$ kΩ) in 2P3M 3-μm top metal wafers.

A. Top Metal Layer Processing

The mechanical stress on the resistance deviation under the top metal layer process is discussed. First, a thin top metal layer of 0.8 μm with its passivation film is verified to reduce the resistance deviation for RPM1 and RP resistors. Measurements of the typical resistor of RPM1 and the original resistor of RP in the 2P3M wafers with a top metal thickness of 0.8 and 3 μm are made to ensure the stress effect. In this experiment, the resistance deviation of 124 samples in two wafers for 0.8-μm thin top metal layer and 186 samples in three wafers for 3-μm thick top metal layer were measured. Figs. 6 and 7 plot the histogram of resistance deviation for five wafers. The resistance deviation is presented in Table III. The resistance deviation and three times of the StDev in RPM1 and RP resistors are $-1.79 \pm 4.65\%$ and $-12.08 \pm 4.73\%$ for 0.8-μm process and $-8.63 \pm 3.06\%$ and $-20.44 \pm 3.54\%$ for 3-μm process. For both RPM1 and RP, the deviations in the wafer with a thick top metal layer of 3 μm are worse than the wafer with a thin top metal layer of 0.8 μm.

The average of resistance deviation in the 0.8-μm thin wafer is based on the sheet resistance of NHRPO resistor which yields an error of -2.8%. The accuracy of RPM1 resistor for the 0.8-μm thin wafer is better than others in this experiment.

TABLE III
SHIFT OF N-TYPE HRPO RESISTOR (289 kΩ, $Rs = 3$ kΩ) IN 2P3M WAFERS

Types	Thickness (µm)	Mean (%)	StDev (%)	Samples
RP	0.8	-12.08	1.58	124
RPM1 (Typical)	0.8	-1.79	1.55	124
RP	3	-20.44	1.18	186
RPM1	3	-8.63	1.02	186

TABLE IV
RESISTANCE DEVIATION OF FIVE-TYPE LAYOUTS IN 3-μm TOP METAL WAFERS ($Rs = 3$ kΩ)

	2P2M (124 samples)		2P3M (186 samples)		2P4M (186 samples)	
Types	Mean (%)	StDev (%)	Mean (%)	StDev (%)	Mean (%)	StDev (%)
RP	-21.32	0.77	-20.44	1.18	-20.82	0.79
RPM1	-12.92	1.20	-8.61	1.03	-9.13	1.18
RPAM	-19.21	1.04	-16.44	1.06	-14.82	1.30
RPRC	-7.97	1.19	-3.07	1.14	-3.63	1.17
RFPC (Proposed)	-0.31	1.09	0.31	1.05	0.07	1.25

Accordingly, the piezoresistance tensor can be predicted to $\sigma_{\mathrm{RP},3\mu m} > \sigma_{\mathrm{RP},0.8\mu m} > \sigma_{\mathrm{RPM1},3\mu m} > \sigma_{\mathrm{RPM1},0.8\mu m}$ by (3). Therefore, the mechanical stresses of the top metal layer with its passivation layer are 7.3, 4.6, and 3.1 times that of a standard device.

B. Processing of Multilayer Metal

In this experiment, the wafers with different metal layers are performed to find a correlation between the resistance deviation and the distance from poly resistor to passivation film. The deviation results of five layouts are summerized in Table IV. The process in this paper provides the metal layers of 2M, 3M, and 4M and uses a thick top metal layer of 3 μm. Based on that, the experiment of multilayer metals yields various spaces between the passivation layer and poly layer. In Fig. 8, the histogram of resistance deviation of five test resistors is shown with the average and StDev. All of the deviations in the test resistors as a result of each process are about 1%, respectively. However, the deviations of RPM1, a passivation and all-metal coverage and a passivation ring cutting resistors are more than 2%, and only RP and an FPC resistors at 1% when we merge all of the processes in Fig. 8. The average resistance deviation is also compared to full processes. The deviations have -20.8% for passivation coverage layout, -9.9% for passivation and M1 coverage layout, -16.5% for passivation and all-metal coverage layout, -4.5% for passivation ring cutting layout, and 0.07% for fully passivation cutting layout. Overall, the average resistance deviation follows the order RP > RPAM > RPM1 > RPRC > RFPC and the StDevs

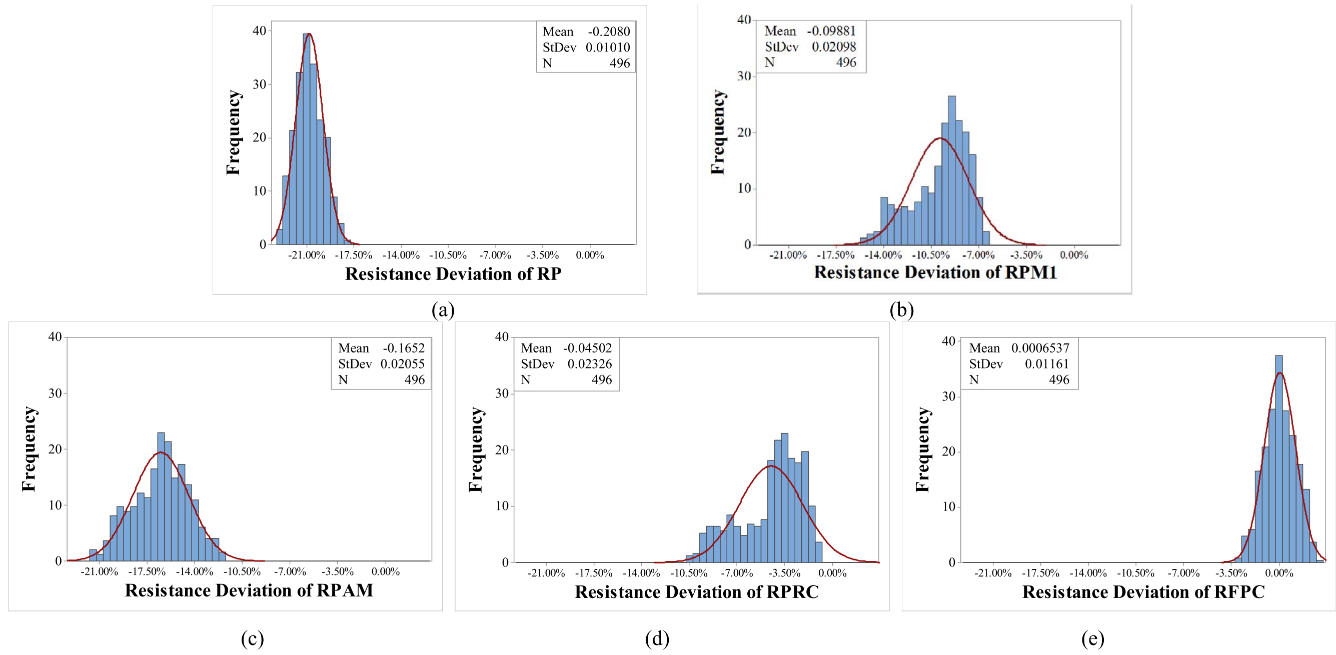

Fig. 8. Histogram of resistance deviation results for 2P2M, 2P3M, and 2P4M 3-μm top metal wafers for (a) RP, (b) RPM1, (c) RPAM, (d) RPRC, and (e) RFPC.

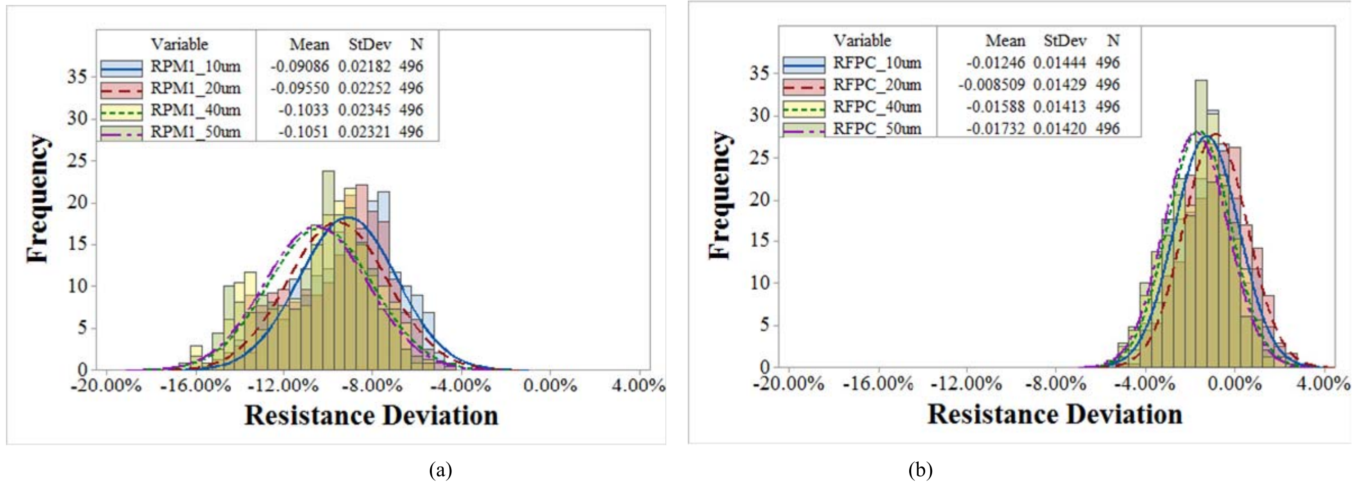

Fig. 9. Histogram of resistance deviation results versus length in 2P2M, 2P3M, and 2P4M 3-μm top metal wafers for (a) RPAM and (b) RFPC.

follow the order RFPC < RP < RPM1 < RPAM < RPRC. The proposed resistor with fully passivation cutting has significant improvement at the resistance deviation. The stress release method is verified to reduce the resistance deviation in any back-end processing.

C. Geometries

In the geometry variation tests, one finger of NHRPO resistor is used to obtain the relationship between the resistance deviation and finger length of resistors. The typical and proposed layouts are compared in this part. The dimensions of finger strip are $L = 10$, 20, 40, and 50 μm with $W = 2$ μm for RPM1 and RFPC. Fig. 9 shows the measured results of average resistance deviations and StDevs. The fabrication process used in this experiment provides the 2M, 3M, and 4M metal layers and uses a thick top metal layer of 3 μm.

According to Fig. 9, the geometry experiment has no significant variation with respect to the size of the finger length. However, the back-end mechanical stress-related resistance deviation is similar between the multifingers resistor and one finger resistor measurements. The RFPC has significantly improved at the average resistance deviation of around -1% and better than the standard layout of around -10%. Therefore, the NHRPO in the FPC layout achieves independency of the geometry.

D. Resistance Deviation Over Temperature

The temperature coefficient of the integrated resistor is important to the resistance variations. Fig. 10 shows the resistance deviation versus operation temperatures and compares to the original NHRPO resistor with RPM1 normalized at 25°C. To measure the temperature coefficient of RPM1 and RFPC,

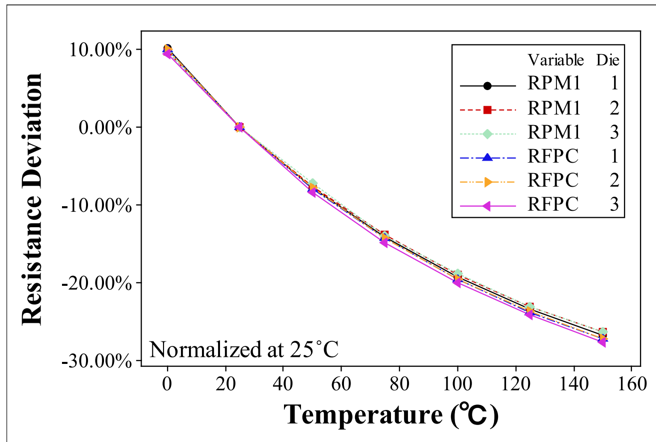

Fig. 10. Resistance deviation results of RPM1 and RFPC versus temperature in 2P3M 3-μm top metal wafers with normalized at 25 °C.

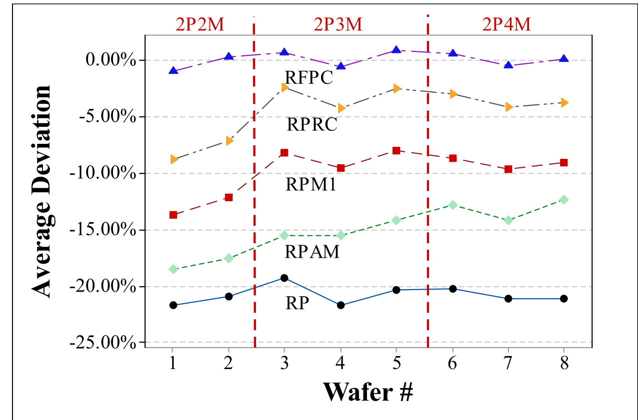

Fig. 11. Resistance deviation of five-type layouts versus different back-end processing in 3-μm top metal wafers.

TABLE V
COMPARISON WITH FIVE NHRPO RESISTOR STRUCTURES

Resistance deviation	RFPC < RPRC < RPM1 < RPAM < RP
Standard deviation	RP > RFPC > RPAM > RPM1 > RPRC
Layout size	RFPC > RPRC > RPAM > RPM1 > RP

wafer chamber is used with increasing the temperatures. For an integrated resistor, the change in resistance is given by

$$R(T) = R_0 \times (1 + TC1 \cdot \Delta T + TC2 \cdot \Delta T^2) \quad (8)$$

where R_0 is the resistance at the room temperature, TC1 and TC2 are the first- and second-order temperature coefficients, and ΔT is the temperature difference. The resistivity varies with temperature in a way that depends on the doping concentration and thickness of polysilicon, as revealed by the studies of the electrical characteristics of polysilicon [5]. According to the results in Fig. 10, the measured resistance deviation versus the function of temperature from 0 °C to 150 °C is similar to test dies of RPM1 and RFPC. As a result, the resistance deviations while normalized at 25 °C are close, even the proposed resistor layout with the better linearity.

E. Discussion

In the experiments, we study the shift behavior for an NHRPO resistor and consider the different layout in back-end layers. The methods of top metal sputtering and passivation deposition were verified to change the resistance because the generated stress was different. The resistance variation performed consistent characters in the same wafer and layout. However, each back-end processing change had a different shift of resistance deviation, especially with metals through the resistor. The resistance deviation comparison is shown in Fig. 11. Five structures are compared with respect to the mean resistance deviation, StDev, and layout size in Table V. As compared to the wafers with 3-μm top metal layer, which covered without any metals was the worst with the maximum shift RP. RPAM and RPM1 were 5%–10% better than RP.

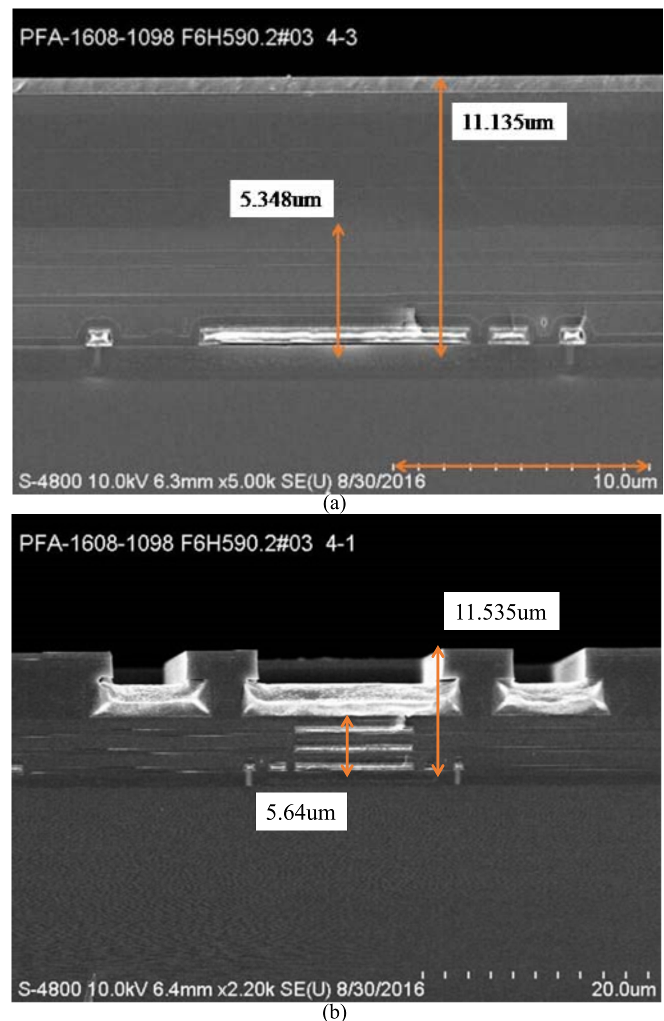

Fig. 12. Cross-sectional view of SEM is Scanning Electron Microscope. Microscopy graphs of (a) RPM1 and (b) RFPC resistors.

Accordingly, the proposed RFPC and RPRC achieved much better performance than others. The same result was also confirmed in a single finger of the NHRPO resistor. As compared with the typical resistor to our proposal, the proposed layout has the advantages of resistance model keeping, linearity

improvement in the temperature coefficient, and no resistance deviation under the back-end process changes in the wafers with a thick top metal layer of 3 μm.

As mentioned in Fig. 11, the resistance deviations show at $0\% \sim -21\%$ in five-type layouts. The resistor with different layouts yields a wide range resistance deviation; it only changed the back-end layers after poly. To further understand the fabrication of the NHRPO resistor in typical and the proposed layouts, microphotographs of their cross sections are taken and shown in Fig. 12. As we can see, more than two dielectric layers are stacked to a high thickness with or without a metal cover on the poly resistor. The stress from the passivation will be passed to the poly or silicon film is owing to their physical space in Fig. 12(a) and (b). Thus, the passivation film is cut to prevent the processing stress. A stack of metals and dielectrics form a buffer against the mechanical stress. Accordingly, both RPM1 and RFPC were hardly found obvious differences at the poly layer by human-eye vision, even the stress and strain was the main problem causing the resistance shift. As a result in Fig. 12, it is difficult to verify any strain on the poly strip by the microscopy graphs. Thus, an integrated resistor is widely used to sense the internal stress as the pressure sensor and piezoresistance sensor. The back-end stress effect results in significant resistance deviation, which is hardly found by visual tests. In addition, the proposed of the nonresistance deviation RFPC method can match the typical resistor model without back-end stress effect.

V. Conclusion

In many power applications, thick top metal layer is used for high-current density, which results in large variations of resistance. For example, as compared to resistors with a 0.8-μm thickness of top metal layer has a smaller average resistance deviation than 3 μm one. In order to reduce resistance deviation by a cost-effective way, this paper developed a method of passivation film separation to create a physical empty room for suppressing the mechanical stresses. Based on this concept, both RPRC and RFPC two NHRPO resistors are proposed. According to the measured results, RFPC achieved only 0.07% resistance deviation, which manufactured on the silicon wafer with $3-\mu$m thickness of the top metal layer. Experimental results showed the proposed RFPC and RPRC with the FPC and an internal coverage of metals form a nondeviation of resistance of high-R polysilicon resistor.

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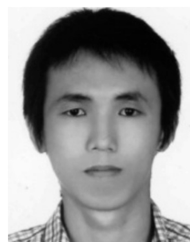

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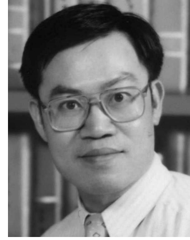

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