Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology

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***Abstract*— State-of-the-art silicon interposer technology of chip-on-wafer-on-substrate (CoWoS) containing the second-generation high bandwidth memory (HBM) has been applied for the first time in fabricating high-performance wafer-level system-in-package. An ultralarge Si interposer up to 1200 mm^2 made by a two-mask stitching process is used to form the basis of the second-generation CoWoS (CoWoS-2) to accommodate chips of logic and memory and achieve the highest possible performance. Yield challenges associated with the high warpage of such a large heterogeneous system are resolved to achieve high package yield. Compared to alternative interposer integration approaches such as chip-on-substrate, CoWoS offers more competitive design rule which results in better power consumption, transmission loss, and eye diagram. CoWoS-2 has positioned itself as a flexible 3-D IC platform for logic-memory heterogeneous integration between logic system-on-chip and HBM for various high-performance computing applications.**

***Index Terms*— 3-D IC, chip-on-wafer-on-substrate (CoWoS), high bandwidth memory (HBM), interposer, through silicon via (TSV).**

I. Introduction

CHIP-on-wafer-on-substrate (CoWoS) is a through silicon via (TSV) interposer-based multipledie wafer-level-system integration (WLSI) to achieve higher system performance in parallel with Moore's Law [1]. The momentum for development on CoWoS has been high in recent years. The goal is to further perfect the technology for a wider application envelope and to extend its integration compatibility. The first-generation CoWoS products are high-end field-programmable gate array (FPGA) with a Si interposer die area up to ~800 mm^2, very close to the maximum area of a reticle field [2], [3]. The limitation for interposer die area was soon extended and a CoWoS-based FPGA product with interposer size ~1200 mm^2 has been proposed [4]. In 2016, with the advent of second-generation high bandwidth memory (HBM2) [5], CoWoS capability has been extended to include logic and third-party memory dies (Fig. 1).

Total number of transistors in a package can be used as an index to gauge the performance of a system-in-package (SiP). In CoWoS, the transistors count increases dramatically by nearly two orders of magnitude in recent years (Fig. 2). This unique integration capability of CoWoS has enabled a new category of super high-end products for cutting-edge high-performance computing (HPC) applications.

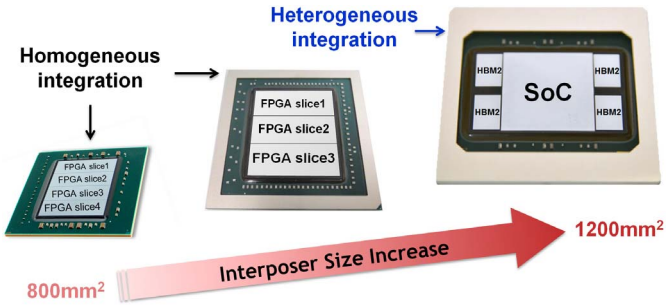

Fig. 1. Interposer size has been increased in the past few years to extend the technology envelope of CoWoS.

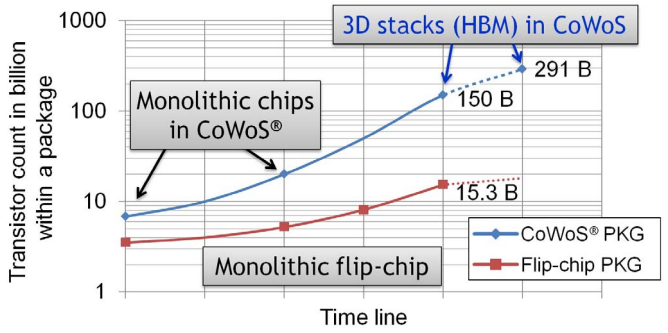

Fig. 2. Performance advancement for CoWoS versus flip chip using the total number of transistors as the performance index.

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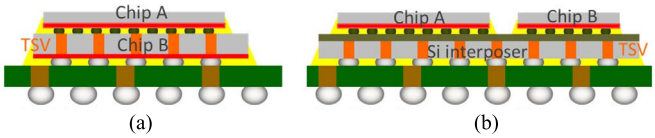


Fig. 3. Basic 3-D IC schemes with TSV. (a) Vertical logic-on-logic. (b) Side-by-side on Si interposer.

In this paper, we will summarize the work on CoWoS envelope extension to make a Si interposer beyond a full reticle size. We will also elaborate the advances of other technology features such as fine pitch C4 Cu bump, HBM integration, and embedded high density metal–insulator–metal (HD-MIM) capacitors in the interposer. Performance comparisons by electrical and mechanical simulations are made to compare CoWoS with other Si interposer integration options such as chip-on-substrate (CoS) [6]–[8].

II. CoWoS Technology Overview

The 3-D integrated circuits (3-D ICs) were envisioned to have many structural schemes for a wide range of applications. The vertical stack of multiple chips and the planar, side-by-side, integration on Si interposer is two generic 3-D IC schemes (Fig. 3) [9]. Compared with the logic-on-logic vertical stack, the Si interposer integration has several merits to gain early adoption in the industry. First, the TSV is inserted in the Si interposer where a mature Si technology is used, so it does not take extra effort for TSV characterization after a new technology node is available which will affect the time to market. Second, all the top dies in CoWoS are independent functional units of known-good-die (KGD) before stacking. The KGD die thickness will remain essentially the same throughout the packaging process. This will ensure a higher integration yield in the Si interposer than that in the vertical stack, where the chips after KGD test are thinned down significantly during the subsequent process due to the presence of TSV, as shown in Fig. 3. Third, vertical stack has challenges in a heterogeneous system with dies of different sizes, which is common for logic functional partition, while Si interposer is of better flexibility. Last but not least, CoWoS can leverage the existing thermal solutions developed by flip-chip packaging, whereas vertical logic stacks will require new thermal dissipation solutions to resolve the issue.

Fig. 4 shows the main types of SiP in WLSI, including the wafer-level chip-scale package, integrated fan out (InFO), InFO with package-on-package (InFO), and CoWoS. CoWoS holds a unique position in the application space of very high IO pin count and very large integrated Si area.

The very large Si die and package sizes pose more concerns for chip-package interaction (CPI). However, CoWoS is essentially immune from the CPI concern. Si interposer plays a unique and important role to suppress the CPI. The mechanically sensitive top dies, often with extreme low-k (ELK) dielectric layers, are bonded on the Si interposer, typically 100-μm thick, which is thermally matched with each other. The package stress from the organic substrate is relaxed by a great extent at the top die ELK interface. In addition,

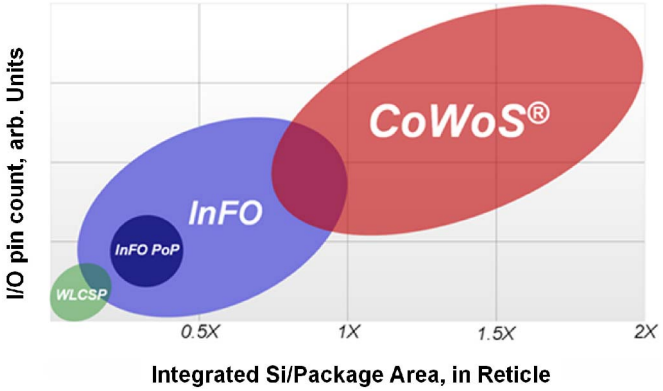


Fig. 4. Main types of WLSI plotted in the application space by integration area and IO count.

Si interposer enables the proven fab-class submicrometer interconnects for die-to-die routing. The large area and fine pitch routing capabilities make CoWoS an ideal platform for very high-end HPC applications.

III. Second-Generation CoWoS

In the CoWoS process, chips of same or different functions are bonded side-by-side on a Si interposer wafer through micro- bumps (uBump) to form chip-on-wafer (CoW). The CoW, in a 300 mm wafer form, is then subjected to C4 bump formation after thinning to reveal the TSV preformed in the Si interposer. Finally the wafer is diced and flip-chip bonded to a package substrate to complete the CoWoS.

There are several ways to pack more transistors in a CoWoS package besides the device shrink which is generally achieved by the Moore's law. Increasing the interposer die area is an obvious option in addition to vertical stacking. To extend the interposer die area limitation beyond a full reticle field, we developed the second-generation CoWoS (CoWoS-2) technology. A two-mask stitching photolithography was developed to fabricate the ultralarge interposer. 1200 mm^2 interposer area, which is about 1.5 times of a full reticle size, is set as a reasonable goal of CoWoS-2. This is combined with other technical features including fine pitch Cu bump, multiple metal options, HBM2 integration, and HD-MIM capacitors to empower CoWoS-2 as a state-of-the-art SiP solution.

A. Mask Stitching Technology

The success of the two-mask stitching process is demonstrated by the excellent continuity performance of stitched interconnect lines or the so-called redistribution layer (RDL). The stitched RDL in CoWoS-2 has been qualified with a 0.4/0.4 μm width/space metal scheme throughout the entire ultralarge interposer area. Fig. 5 shows the cumulative sheet resistance (Rs) of stitched RDL across the stitching boundary. The Rs distribution plots for stitched and nonstitched meander structures completely overlapped with each other, showing the resistance contribution from the dimension variation in the stitching zone is negligible. The reliability of such stitched RDL has been verified by electro migration, stress migration, and time-to-dielectric breakdown tests.

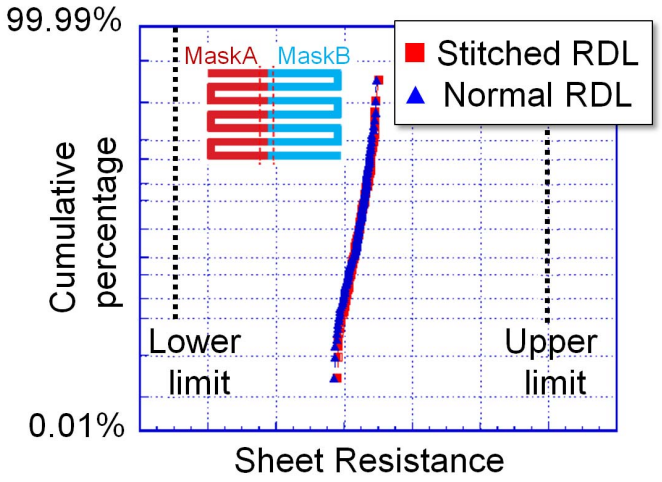


Fig. 5. Rs of normal and stitched 0.4/0.4 μm width/space RDL in ultralarge Si interposer.

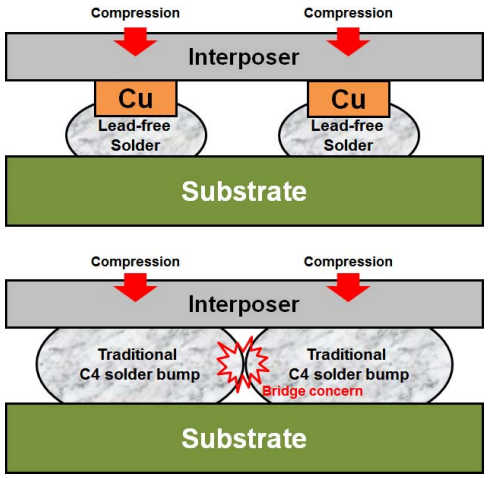


Fig. 6. Schematic showing the superior bridging window for (a) Cu bumps as compared with (b) traditional solder bumps.

B. Fine Pitch Cu Bump

To comply with lead-free requirements and to provide room for future C4 bump scaling, Cu bump is introduced as a baseline feature in CoWoS-2. Cu bump reduces bump bridge risk by using a reduced amount of lead-free solder over the Cu bump. In contrast, the traditional Sn-Pb-based solder bumps are prone to solder bridging upon die attach reflow (Fig. 6). Yield challenges associated with high warpage induced by various polymer filler materials in the CoW wafer were resolved by a thorough process tuning. The X-ray images in Fig. 7 show undistorted C4 Cu bump shape even at the corners of such a large Si interposer.

C. RDL Options in Si Interposer

The capability of providing sub-micrometer pitch RDL between different dies is a key advantage for Si interposer that can directly leverage the fab processes. However, due to the tradeoff between routing density and *RC* delay, the choice of appropriate RDL metal option is product dependent.

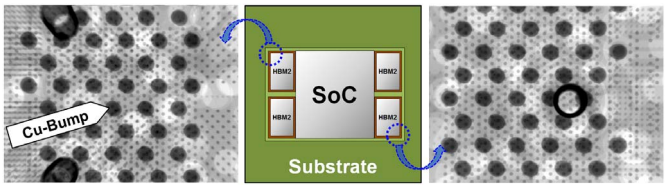


Fig. 7. X-Ray images of CoWoS package showing C4 Cu bumps at interposer corners remain undistorted after flip-chip bond process on a substrate.

TABLE I
METAL SCHEMES PROVIDED BY TSMC FOR Si INTERPOSER RDL

	Mz	Mi	Mu
Thickness	8.5k	15k	34k
Width	0.4 um	0.8 um	2 um
Length	4 mm		

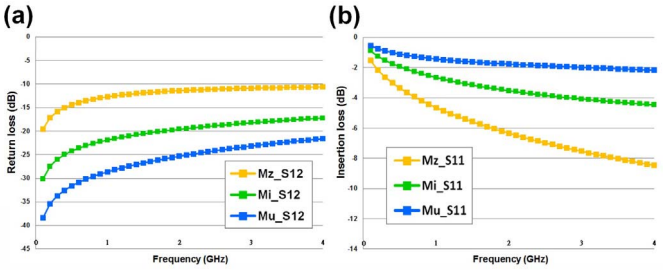


Fig. 8. HFSS simulation results of (a) return loss and (b) insertion loss on different RDL schemes.

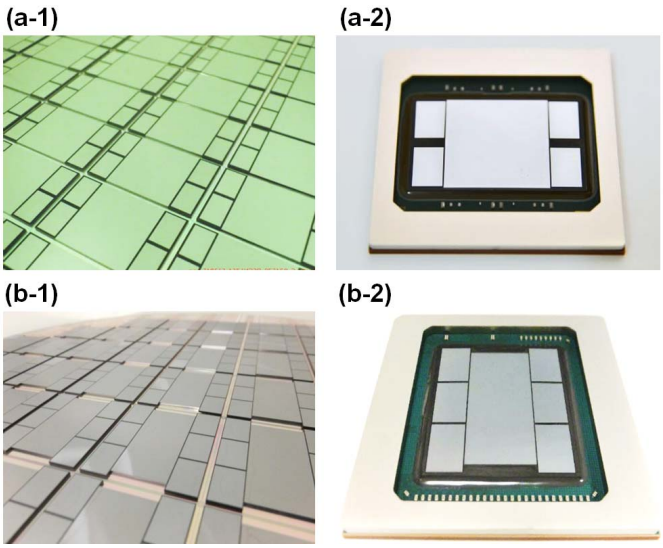


Fig. 9. CoW wafer and CoWoS package views showing two types of interposer floor plans. (a-1) and (a-2) One SoC and four HBM2, or "1 + 4." (b-1) and (b-2) One SoC and six HBM2, or "1 + 6" (courtesy of Broadcom/NEC).

Three metal schemes (Table I) were evaluated for performance comparison by high-frequency structure simulator (HFSS). Signal return loss and insertion loss in each metal scheme

Fig. 10. Optical cross-sectional image of CoWoS-2 package showing all the components and a well-controlled package coplanarity.

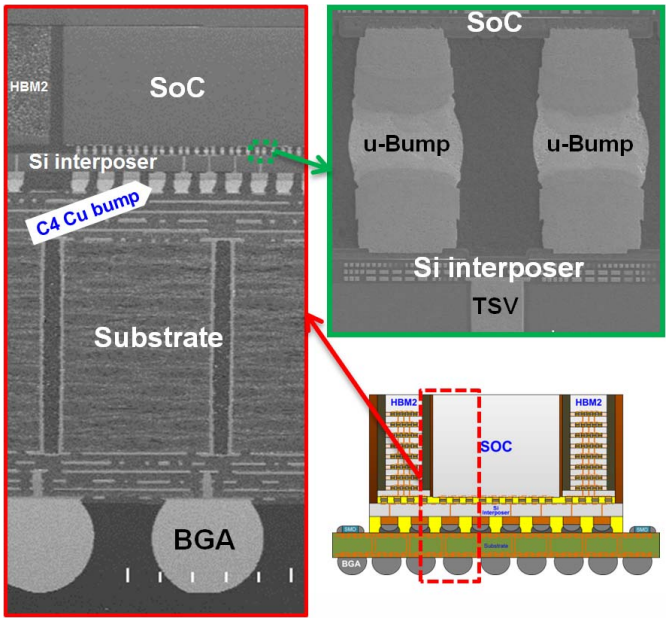


Fig. 11. SEM cross-sectional image showing uBump, Si interposer, TSV, C4 Cu bump, substrate, ball grid array and an advanced node SoC as well as HBM2 in a CoWoS-2 package.

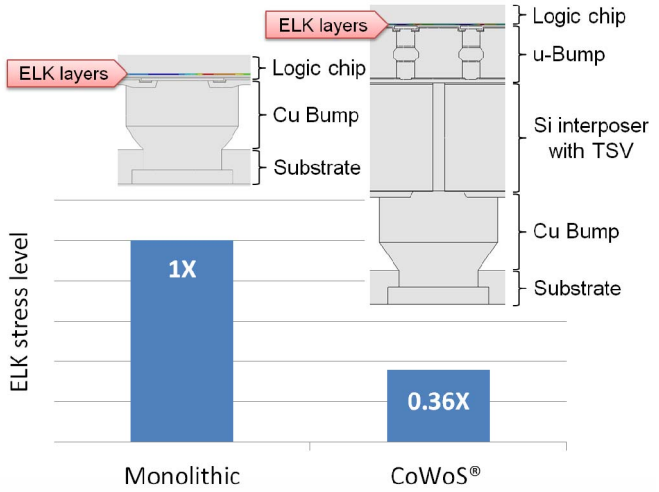


Fig. 12. Simulation comparisons showing the ELK stress of SoC over the TSV interposer is much smaller than that of traditional flip chip.

were characterized in Fig. 8 and showing that thicker metal delivers a better signal integrity. However, thicker metal means worse width/space and results in a lower routing density. This is not preferred in products with a heavy die-to-die routing requirement, such as large die partition. Therefore, selecting an appropriate RDL scheme by considering both operation condition and bandwidth for different products is an important task for circuit designers. In general, CoWoS with Si interposer is compatible with any type of metal scheme available in a Si fab to meet the overall performance and routing demand for die-to-die interconnection.

D. Integration of HBM2

The flexibility of accommodating HBM2 under different interposer floor plans has also been demonstrated. Fig. 9 shows the inline photographs of post CoW and post on-substrate (oS), for two different floor plan arrangements. Fig. 10 shows the global view of the package cross-sectional image with all the components of HBM2, system-on-chip (SoC), interposer, and substrate. Fig. 11 revealed the key features of uBump, TSV, C4 Cu bump on the Si interposer in CoWoS-2.

E. Integration of HD-MIM Capacitors

To reduce signal noise from power source and ensure a stable voltage supply, Si interposer with HD MIM capacitors has been implemented in CoWoS-2 [10]. In terms of scalability and unit-area capacitance density, MIM capacitors are superior to metal-oxide-metal and metal-oxide-semiconductor. The integration of HD-MIM capacitors is an advantage for Si interposer that is processed in an advanced fab. Besides, it is independent of top die technology node and can eliminate the yield impacts of capacitors embedded in top dies. HD-MIM is an attractive feature to enhance the power and/or signal integrity in the CoWoS applications.

IV. Performance

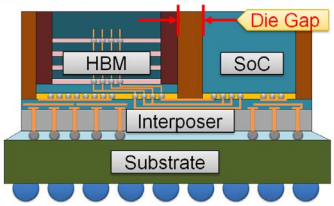
Given the target HBM2 memory bandwidth of 256 GB/s [5], a CoWoS-2 SiP can deliver up to 1 and 1.5 TB/s total memory bandwidth with four and six HBM2 on an interposer, respectively. This is much higher than the bandwidth that can be achieved by traditional on-board dynamic random access memory architectures. The ultralarge interposer area, fine top die gap, Cu bump for pitch scaling flexibility, and robust reliability performance have differentiated CoWoS from other multidie integration solutions.

A. Electrical Performance

Signal transmission between SoC and HBM was simulated by an HFSS 3-D full-wave model to compare CoWoS and a CoS package. CoWoS delivers favorable electrical results due to the fine top die gap of less than 70 μm, whereas CoS has a much larger top die gap because of its inherent process limits. Table II shows that the transmission loss, eye height, and power consumption of CoWoS product are 22%, 20%, and 5% superior than those of the assumed CoS product, respectively.

TABLE II
SIMULATION RESULTS SHOWING COWOS PRODUCT CONTRIBUTES BETTER SIGNAL INTEGRITY BY THE FINE TOP DIE GAP ARCHITECTURE

	CoWoS® Product	CoS Product
Transmission loss at 1GHz	0.78X	1X
Eye diagram height	1.20X	1X
Power consumption	0.95X	1X



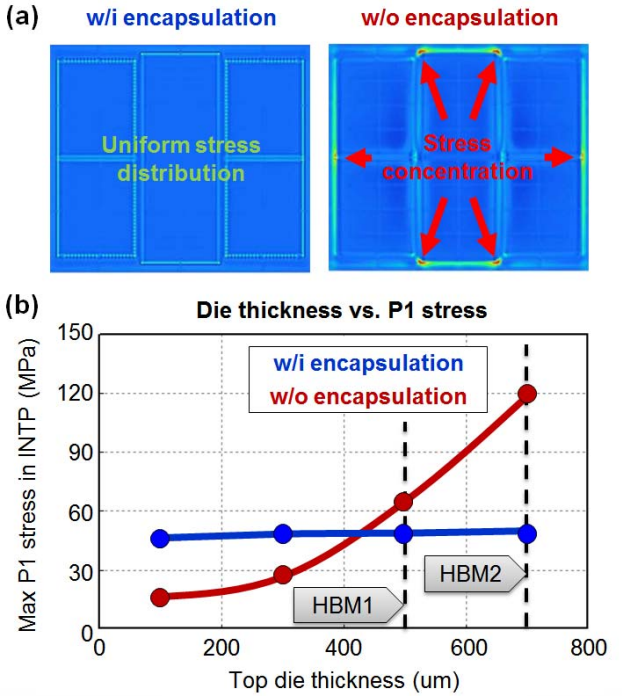


Fig. 13. Simulation results showing (a) stress distributions and (b) relationships between top die thickness and maximum stress with or without the existence of encapsulation.

B. Mechanical Performance

Mechanical stress simulation has been done to show the thermal stress in the SoC ELK dielectric layers with and without an interposer (Fig. 12). Under the corner bump of a large SoC die of 675 mm^2 assumed in this simulation, the stress in the ELK layers in the interposer case is less than 40% of that occurs in a flip chip case. These data support our real Si finding that no CPI damage has ever been found in CoWoS. The interposer stress distribution was compared between CoWoS with encapsulation and CoS without encapsulation. Fig. 13(a) shows the package structure with encapsulation, as in the CoWoS case, has a more uniform stress than that without, such as CoS. Fig. 13(b) shows that CoWoS with encapsulation is more favorable than those without to be compatible with a wider choice of top die thicknesses, as is required in HBM2 integration.

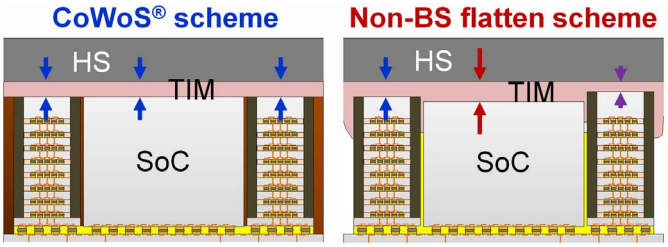


Fig. 14. Schemes showing that CoWoS with flatten backside surface benefits the BLT uniformity of thermal interface material whereas the ones with discontinuous surface trap voids and cause various BLT among top dies.

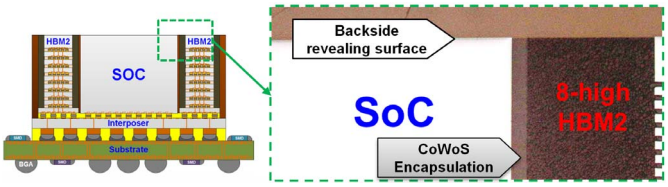


Fig. 15. Cross-sectional image showing CoWoS benefits BLT uniformity by a flat and smooth backside revealing surface.

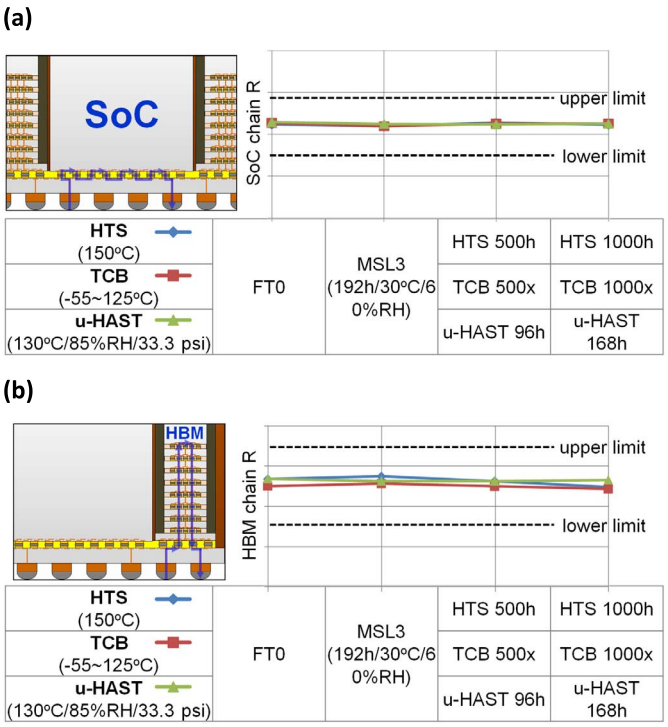


Fig. 16. Continuity of CoWoS packages after reliability tests. (a) SoC and (b) HBM daisy chain resistance are stable after HTS, TCB, and u-HAST tests.

C. Thermal Performance

CoWoS benefits the thermal performance by providing a well-controlled bond line thickness (BLT) due to its excellent backside surface coplanarity. Fig. 14 schematically expresses the impacts on BLT by the backside conditions of packages. CoWoS with an ideal backside surface leveling helps to achieve good BLT control. On the contrary, backside surface leveling is not ensured in certain integration approaches

such as CoS. The compromised BLT uniformity adds more challenges to the thermal dissipation task which is extremely demanding by itself due to very high-power consumption. Fig. 15 shows that the backside surface of CoWoS reveals SoC and HBM2 in the same plane and thus benefiting the uniformity of BLT among all top dies.

V. Reliability

Qualification items compliant to the Joint Electron Device Engineering Council (JEDEC) were performed to ensure the CoWoS-2 component with one SoC and four HBM2 can meet industry-wide reliability standards. Moisture sensitive level 3 (MSL3), high-temperature storage (HTS), temperature cycling classification B (TCB), and unbiased highly accelerated stress testing (u-HAST) were performed on CoWoS-2. Our test vehicle passed all JEDEC qualification items with more than 50% margins left. Fig. 16 shows the detailed qualification criteria of reliability and the electrical continuity performances for each item.

VI. Summary

CoWoS-2 with an interposer die area up to 1200 mm^2 has been developed to extend the capability and level of integration by a two-mask stitching approach. This not only marks a breakthrough in the Si die size used in a package, but facilitates a new family of extremely high-end products that require a package level multidie integration between high-performance logic SoC and memory of HBM2. We also analyzed that from many aspects including electrical, mechanical, and thermal, CoWoS is indeed a superior integration approach compared with other interposer integration options such as CoS. Finally, at this size, CoWoS-2 maintains a robust integration platform with good reliability performance. The technology still has not reached the limitation yet. It is highly expected that the envelope of the CoWoS WLSI technology will be further developed for a larger area, higher level of integration complexity, more enriched device features, and with better thermal dissipation solutions within one component to meet growing demands in the HPC and AI era.

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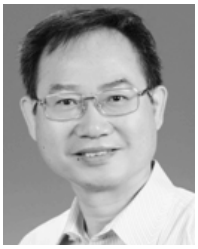

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