Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs

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***Abstract*—This paper reports on the impact of soft- and hard-switching conditions on the dynamic ON-resistance of AlGaN/GaN high-electron mobility transistors. For this study, we used a special double pulse setup, which controls the overlapping of the drain and gate waveforms (thus inducing soft and hard switching), while measuring the corresponding impact on the ON-resistance, drain current, and electroluminescence (EL). The results demonstrate that the analyzed devices do not suffer from dynamic R_{ON} increase when they are submitted to soft switching up to $V_{DS} = 600$ V. On the contrary, hard-switching conditions lead to a measurable increase in the dynamic ON-resistance (dynamic-R_{ON}). The increase in dynamic R_{ON} induced by hard switching is ascribed to hot-electrons effects: during each switching event, the electrons in the channel are accelerated by the high electric field and subsequently trapped in the AlGaN/GaN heterostructure or at the surface. This hypothesis is supported by the following results: 1) the increase in R_{ON} is correlated with the EL signal measured under hard-switching conditions and 2) the impact of hard switching on dynamic R_{ON} becomes weaker at high-temperature levels, as the average energy of hot electrons decreases due to the increase scattering with the lattice.**

***Index Terms*—Dynamic on-resistance, GaN, hard switching, high-electron mobility transistors (HEMTs), trapping effects.**

I. INTRODUCTION

GAN-BASED high-electron mobility transistors (HEMTs) have excellent performance for application in the power conversion field. Thanks to the high breakdown electric field (3.3 MV/cm), the low ON-resistance (R_{ON}) and the low gate capacitance, GaN-based devices represent an almost ideal solution for high-voltage (650–1200 V) switching applications. The ON-resistance of these devices has recently reached the record level of $R_{ON} \sim 6$ mΩ (for 100 A devices, [1]), thus clearing the way for a massive market penetration of GaN-HEMTs. Moens *et al.* [1] moreover discuss the possibility of extending the technology up to 1.2 kV/ $R_{ON} < 10$ mΩ by means of a variation in the strain-relief layer and optimization of the top passivation layer.

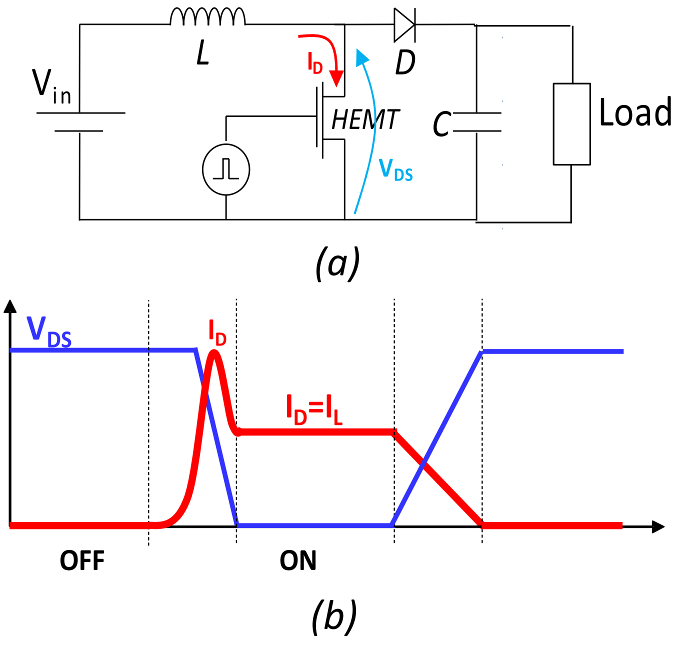

Fig. 1. (a) Schematic representation of a boost power converter. (b) Schematic representation of the waveforms of V_{DS} and I_D during a switching event.

Recent reports (see [2], [3]) demonstrated that GaN-based metal–insulator-semiconductor (MIS)-HEMTs have high reliability and stability under high-temperature reverse-bias conditions, i.e., when the devices are biased in the OFF-state, with a high drain voltage and high temperatures (typically 150 °C). Under these conditions, a high electric field is present between gate and drain, with negligible drain current.

Another stress regime, relatively unexplored in the literature [4], [5], occurs during hard switching, from OFF-state to ON-state. To understand this problem, we can consider the simple example of a boost power converter (see the schematic in Fig. 1). When the HEMT is in the OFF-state, the input voltage V_{in} (for instance 600 V) appears between drain and source, and no current flows through the transistor. During the turn-ON transient, the voltage on the drain (V_{DS}) has to rapidly drop from V_{in} to (almost) zero, while the drain current (I_D)

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has to increase and become equal to the inductor current [see Fig. 1, (Bottom)], after a quick current spike related to the discharge of the drain–source capacitance [5]. This transition is not instantaneous, and there exists a brief time interval during which high current and high voltage are simultaneously present. This results in the presence of hot electrons, which are known to accelerate degradation [6], [7] and charge trapping [8]. Trapping effects can strongly be affected by the presence of hot electrons. The corresponding trap levels can be in principle located both under the gate (inducing a shift of the V_{TH}) and in the access region (leading to a decrease of the transconductance peak) [9]. Bahl *et al.* [5] furthermore demonstrated by TCAD simulations that under hard switching, hot electrons generated in correspondence of the field plates can be injected into the buffer and/or dielectric layer, leading to a significant increase of the dynamic ON-resistance.

The effects related to hot electrons are influenced by several aspects, namely the number of electrons in the channel, the temperature (which increases the scattering, and thus limits the energy of electrons), and the electric field. Several approaches discussed in the literature, such as the use of field-plate structures and/or optimized buffer design, were found to significantly reduce the electric field and, thus, to crucially limit the effects related to the hot electrons [1], [9], [10].

Despite the importance of this topic, only few reports discussed the effect of hard switching on the dynamic performance of GaN HEMTs [4], [5], [11]. The most quantitative results were presented by Joh *et al.* [4], who reported a detailed comparison of the current collapse under soft and hard switching, up to 200 V. By means of a novel technique drain and gate pulses were adjusted to mimic different load lines and perform pulsed measurements with different switching conditions. The results show that—for the samples under investigation—the current collapse significantly decreases under hard-switching conditions. The authors suggest that in this case the trapping, mainly determined by electrons trapped at the device surface through gate leakage, is compensated by holes generated by impact ionization.

The aim of this paper is to improve the understanding of the impact of hard-switching conditions on the dynamic performance of GaN-based HEMTs. We developed a novel setup which allows to modify the overlapping between gate and drain waveforms (thus favoring or reducing hard switching), to quantitatively monitor the gate and drain pulse waveforms, to measure the resulting dynamic R_{ON} increase, and to evaluate the EL signal generated by hot electrons during the hard-switching events. The study was carried out on 650-V GaN-based MIS HEMTs with low dynamic R_{ON}; we analyzed the transition from soft- to hard-switching condition by focusing on the correlation between drain/gate pulse overlapping, dynamic R_{ON} increase and variation in the EL signal detected by means of emission microscopy. Results demonstrated that: 1) hard-switching results in a measurable increase in dynamic R_{ON} (at 600 V, we measured 15 Ω·mm in soft switching and 16.5 Ω·mm in hard switching); 2) the increase in dynamic R_{ON} is strongly related to the hot-electron luminescence signal detected by EL measurements, thus confirming the important role of hot electrons; and 3) the impact of hard switching on dynamic R_{on} becomes weaker at higher temperatures. The experimental results collected within this paper indicate that the additional trapping processes induced by hard switching originate from hot electrons.

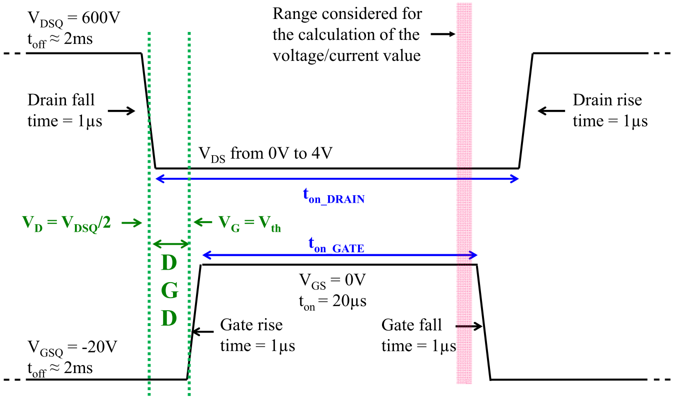

Fig. 2. Representative schematic of the drain and gate pulses applied during the analysis of the dynamic ON-resistance. The DGD is defined as the time range between $V_D = V_{\mathrm{DSQ}}/2$ and $V_G = V_{\mathrm{TH}}$. The range of the pulse considered for the calculation of the current–voltage curve is highlighted in shaded pink.

II. EXPERIMENTAL DETAILS

The devices under test are normally on GaN MIS HEMTs grown on a p-type silicon substrate. The GaN metal–organic chemical vapor deposition structure consists of (from top to bottom) an AlN nucleation layer, a superlattice strain-relief layer, a C-doped layer, and a GaN unintentionally doped layer. On top, an $\mathrm{Al_{0.25}Ga_{0.75}N}$ barrier layer and an *in situ* SiN are grown. R_{hosheet} of the two-dimensional electron gas (2DEG) as measured from TLM and Van Der Pauw structures is ∼420 Ω/sq. Hall mobility and 2DEG density are $\sim$1800 $\mathrm{cm^2/V{\cdot}s}$ and $\sim 9 \times 10^{12}$ $\mathrm{cm^{-2}}$, respectively. The MIS-HEMT gate structure consists of the *in situ* SiN as gate dielectric, with an Al-based gate-stack. A gate field plate as well as two source field plates is present. The devices are passivated using plasma-enhanced chemical vapor deposition SiN and polyimide. The samples have a pinch-off voltage of −12.5 V, a dc ON-resistance of ≈ 15 Ω·mm ($V_{\mathrm{GS}} = 0$ V, $W_{\mathrm{G}} = 0.2$ mm), and an OFF-state breakdown voltage higher than $V_{\mathrm{D}} = 650$ V. The pulsed measurements, taken in soft-switching conditions, show a negligible increase of the dynamic R_{ON} after OFF-state drain bias at 600 V and high ambient temperature (up to $T = 150$ °C).

For this study, we developed a novel experimental setup, which allows to carry out pulsed measurements while independently controlling and monitoring the intervals between the gate and drain pulses. At the same time, the luminescence signal emitted by the samples during hard-switching events can be monitored by means of a cooled charge-coupled device (CCD) camera synchronized with the driving waveforms (detection range of the system constituted by the microscope and the camera is 350–1100 nm).

Fig. 2 depicts a schematic of the applied pulses. In order to study the trapping effects, several (OFF-state) quiescent bias points are used: a null bias point ($V_{\mathrm{GSQ}} = V_{\mathrm{DSQ}} = 0$ V),

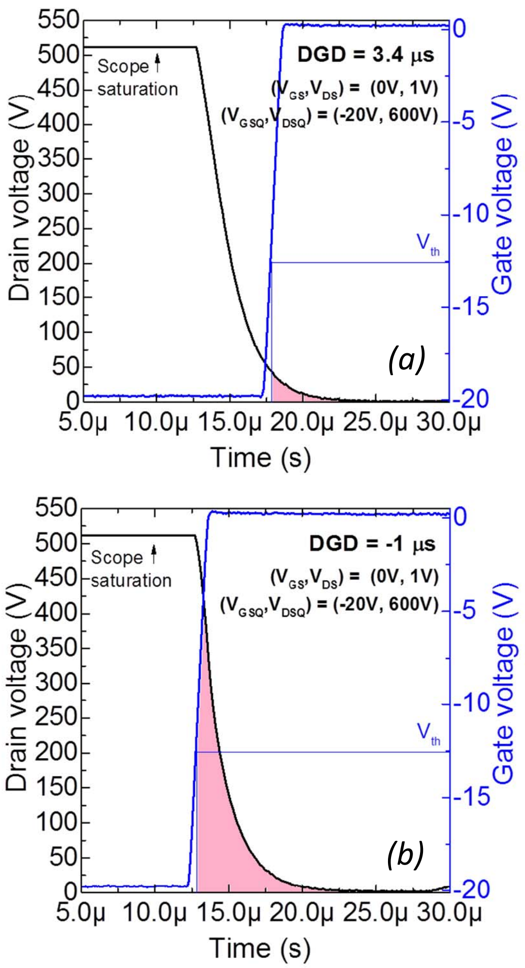

Fig. 3. Overlapping between the gate and the drain pulses applied at (V_{GSQ}, V_{DSQ}) = (−20 V, 600 V) and (V_{GS}, V_{DS}) = (0 V, 1 V). The overlapping is showed for a DGD corresponding to (a) 3.4 and (b) −1 μs.

a gate-lag condition to favor trapping under the gate ($V_{\text{GSQ}} = -20$ V, $V_{\text{DSQ}} = 0$ V), a drain-lag condition to favor trapping between gate and drain ($V_{\text{GSQ}} = -20$ V) with several drain bias levels ranging from 100 to 600 V. During the ON-pulse, the device is kept in linear region in ON-state by a $V_{\text{GS}} = 0$ V and a V_{DS} ranging from 0 to 4 V. A (gate) pulsewidth of 20 μs with a duty cycle of 1% was used for the analysis. It is worth mentioning that the rise and fall time are intentionally long ($= 1$ μs) with the aim of studying with more accuracy the influence of the overlapping between the two pulses. In an actual application, a slew rate of 10–100 V/ns is more realistic.

In order to test different switching conditions, several drain-to-gate delays (DGD) were used by varying from soft switching (DGD > 0 μs) to hard switching (DGD < 0 μs). The DGD is defined as the interval of time range between a drain voltage (V_D) equal to $V_{\text{DSQ}}/2$ and a gate level (V_G) equal to the threshold voltage (V_{TH}).

Fig. 3 reports the overlapping (representative example for $V_{\text{DSQ}} = 600$ V and $V_{\text{DS}} = 1$ V) between the gate and drain pulses for two DGD values, equal to 3.4 and −1 μs, respectively. During soft switching [Fig. 3(a)], a low drain voltage is measured when the device crosses the threshold voltage, resulting in a negligible drain current and power dissipation. Conversely, during hard switching [Fig. 3(b)] the device is submitted, for a short time, to high voltage and high current simultaneously. The drain current and voltage values are measured in the last portion of the pulse, where the signal is more stable, as indicated in Fig. 2.

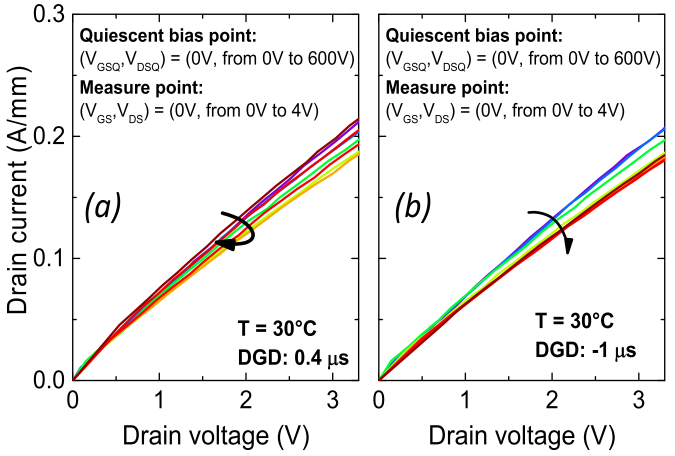

Fig. 4. Pulsed output curve ($I_D V_D$) measured at room temperature with two representative DGD values, namely, (a) 0.4 and (b) −1 μs. At DGD = 0.4 μs, the ON-resistance dynamic variation faces a non-monotonic trend with a maximum at $V_{\text{DSQ}} = 300$ V.

III. EXPERIMENTAL RESULTS

Fig. 4 shows the pulsed $I - V$ measurements taken at room temperature under soft- (DGD $= 0.4$ μs) and hard switching (DGD $= -1$ μs), respectively, starting from several quiescent bias points. In the soft switching conditions [Fig. 4(a)], the R_{ON} faces a nonmonotonic variation with a negligible influence of the DGD value. The maximum dynamic-R_{ON} variation, observed at $V_{\text{DSQ}} = 300$ V, is lower than 10%. At $V_{\text{DSQ}} = 600$ V, a negligible R_{ON} decrease is observed (less than 5%). Under hard switching [Fig. 4(b)], the dynamic curves show an almost monotonic change up to $V_{\text{DSQ}} = 600$ V. A more quantitative description is shown in Fig. 5, that reports the variation of dynamic R_{ON} induced by different gate voltages and different drain/gate overlapping. With soft switching (DGD $= 2.4$ μs), the dynamic R_{ON} shows a nonmonotonic variation with increasing trapping bias. This result is consistent with [12]: for $0 \text{ V} < V_{\text{DS}} < 300$ V, buffer acceptors (probably C_N defects) are ionized, and this results in an increase in dynamic R_{ON}. For higher voltages ($V_{\text{DS}} > 300$ V), the increasing vertical leakage [13], trapping at donor defects [14], and the generation of a 2-D hole gas at the C-GaN/strain-relief layer interface [15], lead to a decrease in the overall amount of trapped electrons, and thus to a reduction of the dynamic R_{ON}. As can be noticed that the use of hard-switching transients does not significantly impact on the dynamic R_{ON} for $V_{\text{DS}} < 300$ V. On the other hand, hard switching has a severe impact on dynamic R_{ON} for $V_{\text{DS}} > 300$ V, i.e., when high voltage/field and drain current are simultaneously present during the switching transient. At $V_{\text{DSQ}} = 600$ V and DGD $= -1$ μs, the dynamic R_{ON} has a value 15%–20% higher with respect to the soft-switching

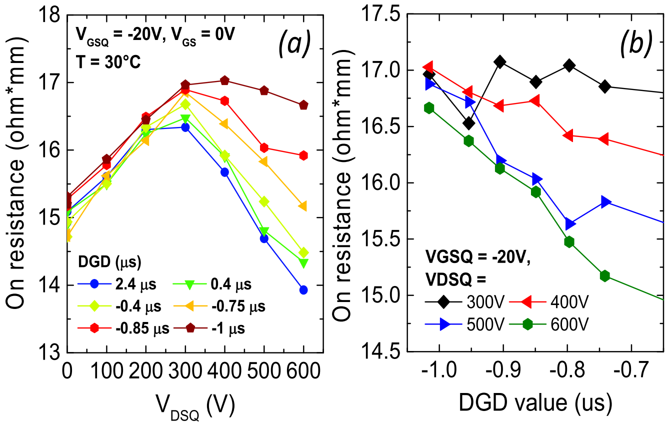

Fig. 5. (a) ON-resistance dynamic variation plotted as a function of the drain quiescent bias point (V_{DSQ}) for several DGD values. The dynamic change of the ON-resistance has a nonmonotonic trend with the V_{DSQ}, showing a maximum for $V_{DSQ} = 300$ V. (b) Variation of the dynamic ON-resistance with a different overlapping (DGD).

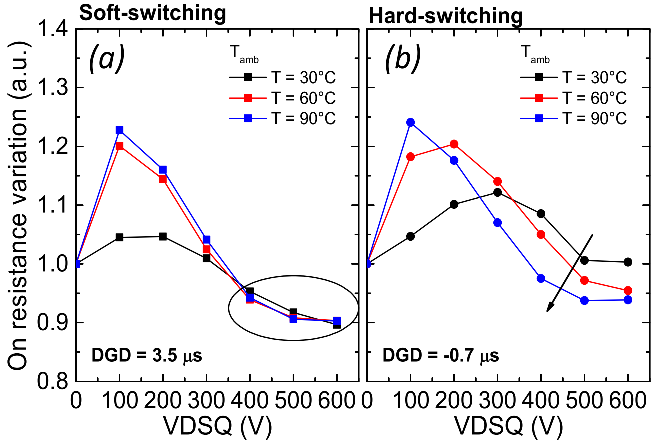

Fig. 6. Dynamic variation of the ON-resistance measured at different ambient temperatures applied ranging from 30 °C to 90 °C. The influence of the ambient temperature (a) at high DGD (3.5 μs) (b) and at low DGD (−0.7 μs) is compared.

case. Repetitive measurements clarified that all the noticed variations are fully recoverable (Fig. 10).

Fig. 5(b) shows the variation of the ON-resistance plotted as a function of the V_{DSQ} for several DGD values, and as a function of the DGD for high drain bias points. Results confirm that under hard switching the dynamic R_{ON} variation is strongly influenced by the overlapping between gate and drain waveforms (linear increase with the DGD < -0.75 μs). In addition, the slope of the above-mentioned variation increases with V_{DSQ}, indicating that the trapping mechanism during hard switching depends on the drain bias level. This result is consistent with the hypothesis that the additional trapping observed during hard switching is due to hot-electron effects.

IV. DISCUSSION

In order to confirm the role of hot electrons in favoring the increase in R_{ON} under hard switching, we investigated 1) the impact of temperature on the total variation of ON-resistance and 2) the EL signal emitted by the devices during hard switching, and its correlation with the overall R_{ON} increase. The results are described in the following.

A. Influence of the Temperature on the Variation of Dynamic on-Resistance

The dynamic behavior of the devices is evaluated under both soft and hard switching at different ambient temperatures (Fig. 6). Normalized values of R_{ON} were plotted to minimize the effect of the reduction of the mobility at higher temperatures. Analysis at high DGD values [soft switching, Fig. 6(a)] demonstrates that temperature has a negligible influence on the Dynamic R_{ON} at high V_{DSQ} levels ($V_{DSQ} > 300$ V). An opposite trend was observed in hard switching [representative example for DGD $= -0.7$ μs, Fig. 6(b)]. At high voltages ($V_{DSQ} > 300$ V), the dynamic R_{ON} decreases with temperature, following a monotonic trend.

These results are consistent with the hypothesis that hot electrons play a major role in the trapping effects under hard switching, according to the following model. During hard switching, high drain voltage and current are present, and the device crosses the semi-ON state. Electrons flowing from source to drain are significantly accelerated by the high electric field, and can be trapped in the AlGaN/SiN layer and/or in the buffer, thus leading to an increase in dynamic R_{ON}. At higher temperatures, the hot-electron effects become less prominent, due to the increased scattering, which leads to a reduction of the mean-free path over which hot electrons are accelerated and—consequently—to a reduction of the average energy of the electrons.

It is worth noting that in hard switching the peak of the variation of dynamic R_{ON} moves toward lower V_{DSQ} values. This may be due to an easier ionization of buffer traps (typically C_N acceptors, having a high activation energy of 0.9 eV).

B. Correlation Between the Increase of Dynamic on-Resistance and the EL Signal

EL measurements were carried out in order to confirm the impact of hot electrons on the increase of the dynamic ON-resistance. During (semi)-ON state, the devices can emit a weak light emission induced by the deceleration (bremsstrahlung) of electrons, which are highly energetic due to the high gate–drain electric field [9], [16], [17]. A CCD camera was used in order to detect the number of photons emitted. With the aim of reducing the signal noise, the CCD camera was cooled at −50 °C, the electro-multiplication (EM) gain was set to 200 with an acquisition time of 60 s. The EL system was used in combination with the soft/hard-switching pulser, in order to detect the weak EL signal generated by the devices during hard-switching transitions.

Fig. 7(a) shows that the intensity of the EL signal increases with increasing overlapping between gate and drain waveforms, i.e., with decreasing DGD. The EL doubles when the devices moves from soft switching to hard switching (i.e., when DGD is reduced from −0.75 to −1μs).

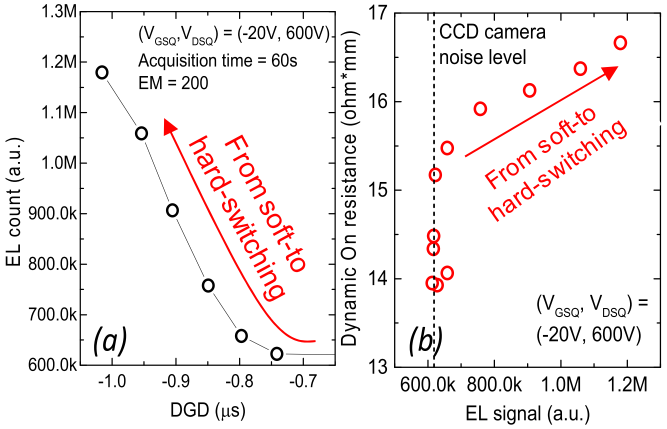

Fig. 7. (a) EL signal monitored with a CCD camera during the pulsed measurements performed with a different DGD. At low DGD (< -0.7 μs), the EL signal increases with the drain–gate overlapping. (b) Correlation between the increase in the EL signal and the increase in the dynamic ON-resistance with a low DGD value applied.

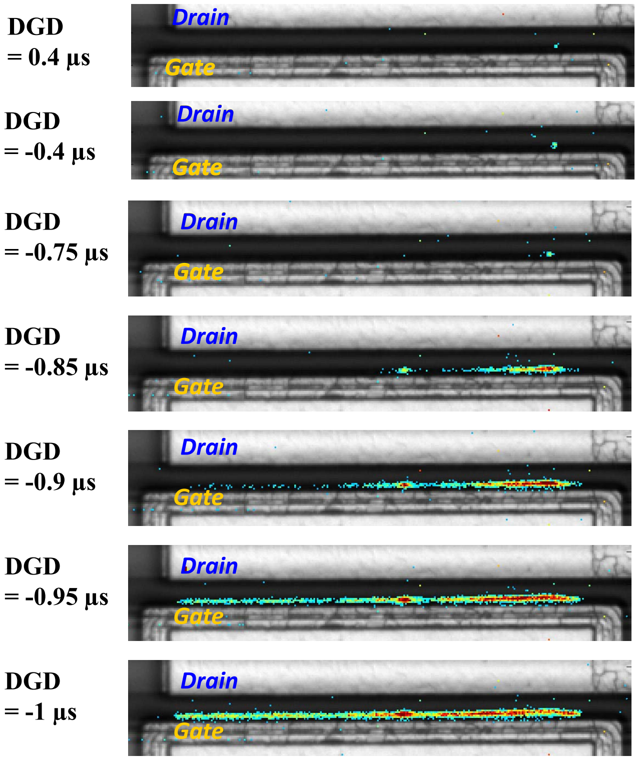

Fig. 8. EL signal detected during the pulsed measurements for several DGD values applied ranging from 0.4 to -1 μs. The EL signal is detected with a CCD camera, an acquisition time of 60 s and an EM gain = 200. $V_{\mathrm{DSQ}} = 600$ V.

Fig. 9. EL signal detected during the pulsed measurements in soft switching (DGD = 3.3 μs) after the evaluation in hard switching. Low EL intensity clarifies the absence of permanent degradation.

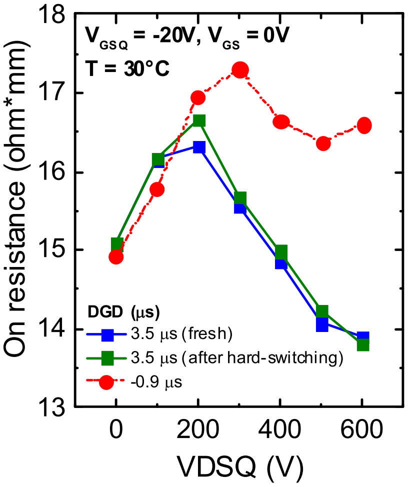

Fig. 10. Dynamic ON-resistance measured in soft switching before (blue line) and after (green line) evaluation in hard switching. Pulsed measurements performed with DGD <0 μs are shown (red line).

Fig. 7(b) moreover demonstrates that there is a strong correlation between the EL signal measured during hard switching and the increase in dynamic ON-resistance. This result further confirms the role of the hot electrons in the worsening of the dynamic performance under hard switching. The above-mentioned correlation was detected independently of the V_{DSQ} value applied down to $V_{\mathrm{DSQ}} = 400$ V (not shown). For lower values, the EL signal is below the noise level of the CCD camera.

Fig. 8 reports the spatially resolved EL patterns measured under different soft- and hard-switching conditions, i.e., for several values of DGD, with a $V_{\mathrm{DSQ}} = 600$ V. The images correspond to the average EL signal measured over 60 s of operation, while the device switches repeatedly from OFF-state to ON-state. In soft switching (e.g., DGD = 0.4 μs), a small hot spot is observed, possibly emitted during the OFF-state phase, and indicating the presence of a localized leakage paths responsible for gate leakage. When moving toward hard switching (i.e., to negative DGD values) the intensity of the signal increases, and the emission pattern becomes almost uniform. Such a pattern is consistent with hot-electron luminescence: electrons are injected uniformly from the source, and accelerated by the high electric field toward the drain. The electric field peaks at the drain side of the gate, and so does the EL signal.

Repetitive measurements were performed under soft switching after the analysis of the EL in hard switching. The low intensity demonstrates in soft switching remain unchanged (Fig. 9), thus indicating that the increase in the EL intensity detected in hard switching is recoverable and not ascribed to permanent degradation. Consistent results were evaluated by means of pulsed measurements performed, under soft switching, after the analysis in hard switching (Fig. 10).

V. CONCLUSION

In this paper, we discuss the dynamic behavior of AlGaN/GaN MIS HEMTs under soft- and hard-switching conditions. In soft-switching conditions, the devices demonstrate excellent performance, with negligible increase of the dynamic R_{ON} up to 600 V even at high temperature ($T = 150$ °C).

By means of a novel experimental setup designed to monitor the electrical and EL characteristics under soft switching and hard switching, we demonstrate that under hard-switching conditions, the samples show a measurable increase in dynamic R_{ON}, which is well correlated with the drain bias level applied and to the overlapping between the gate and drain pulses.

Results suggest that hot-electron effects play a major role in the dynamic performance under hard switching. This hypothesis was validated by investigating the dependence of dynamic R_{ON} increase on temperature, and by studying the correlation between the change in dynamic R_{ON} and the increase in the EL intensity.

REFERENCES

[1] P. Moens, A. Banerjee, P. Coppens, F. Declercq, and M. Tack, “AlGaN/GaN power device technology for high current (100+A) and high voltage (1.2 kV),” in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs*, Jun. 2016, pp. 455–458.

[2] A. Banerjee, P. Vanmeerbeek, L. De Schepper, S. Vandeweghe, P. Coppens, and P. Moens, “On conduction mechanisms through SiN/AlGaN based gate dielectric and assessment of intrinsic reliability,” in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2016, pp. 1–5.

[3] T. Wu *et al.*, “Time dependent dielectric breakdown (TDDB) evaluation of PE-ALD SiN gate dielectrics on AlGaN/GaN recessed gate D-mode MIS-HEMTs and E-mode MIS-FETs,” in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2015, pp. 4–9.

[4] J. Joh, N. Tipirneni, S. Pendharkar, and S. Krishnan, “Current collapse in GaN heterojunction field effect transistors for high-voltage switching applications,” in *Proc. IEEE Int. Rel. Phys. Symp.*, Jun. 2014, pp. 4–7.

[5] S. R. Bahl, D. Ruiz, and D. S. Lee, “Product-level reliability of GaN devices,” in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2016, pp. 1–6.

[6] M. Meneghini, G. Meneghesso, and E. Zanoni, “Analysis of the reliability of AlGaN/GaN HEMTs submitted to on-state stress based on electroluminescence investigation,” *IEEE Trans. Device Mater. Rel.*, vol. 13, no. 2, pp. 357–361, Jun. 2013.

[7] Y. S. Puzyrev, “Modeling of hot-carrier degradation in GaN transistors,” in *Proc. IEEE Int. Integr. Rel. Workshop*, Oct. 2015, pp. 160–166.

[8] M. Meneghini *et al.*, “Trapping in GaN-based metal-insulator-semiconductor transistors: Role of high drain bias and hot electrons,” *Appl. Phys. Lett.*, vol. 104, p. 143505, Apr. 2014.

[9] M. Meneghini *et al.*, “Investigation of trapping and hot-electron effects in GaN HEMTs by means of a combined electrooptical method,” *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2996–3003, Sep. 2011.

[10] P. Moens *et al.*, “On the impact of carbon-doping on the dynamic Ron and off-state leakage current of 650 V GaN power devices,” in *Proc. Int. Symp. Power Semiconductor Devices ICs*, May 2015, pp. 37–40.

[11] S. R. Bahl, J. Joh, L. Fu, A. Sasikumar, T. Chatterjee, and S. Pendharkar, “Application reliability validation of GaN power devices,” in *IEDM Tech. Dig.*, Dec. 2016, pp. 544–547.

[12] G. Meneghesso *et al.*, “Reliability and parasitic issues in GaN-based power HEMTs: A review,” *Semicond. Sci. Technol.*, vol. 31, no. 9, p. 093004, 2016.

[13] D. Cornigli *et al.*, “Numerical investigation of the lateral and vertical leakage currents and breakdown regimes in GaN-on-silicon vertical structures,” in *IEDM Tech. Dig.*, Dec. 2015, pp. 109–112.

[14] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, “Vertical leakage/breakdown mechanisms in AlGaN/GaN-on-Si devices,” in *Proc. 24th Int. Symp. Power Semiconductor Devices ICs*, Bruges, Belgium, Jun. 2012, pp. 1132–1134.

[15] I. Chatterjee *et al.*, “Lateral charge transport in the carbon-doped buffer in AlGaN/GaN-on-Si HEMTs,” *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 977–983, Mar. 2017.

[16] M. Meneghini, A. Stocco, R. Silvestri, N. Ronchi, G. Meneghesso, and E. Zanoni, “Impact of hot electrons on the reliability of AlGaN/GaN high electron mobility transistors,” in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2012, pp. 2C.2.1–2C.2.5.

[17] T. Brazzini *et al.*, “Mechanism of hot electron electroluminescence in GaN-based transistors,” *J. Phys. D, Appl. Phys.*, vol. 49, no. 43, p. 435101, 2016.

Authors’ photographs and biographies not available at the time of publication.