Two-Port-Network-Based Method to Measure Electrical Characteristics of MIS Devices With Ultrathin Barriers

René Berktold and Jochen Mannhart

***Abstract*— MISFETs with ultrathin gate insulator layers are often used as switches in highly integrated circuits. For such transistors, gate currents can be problematic. For devices with nonnegligible channel resistance, such as oxide FETs, gate leakage currents also cause difficulties in measuring the devices' capacitance–voltage (*CV*) characteristics. Here, we present a method to measure *CV* characteristics of MIS devices that is also applicable to devices with sizable channel resistances and large leakage currents.**

***Index Terms*— Capacitance measurement, capacitance–voltage (*CV*) characteristics, leakage currents, MIS devices, thin-film devices.**

I. Introduction

CAPACITANCE–VOLTAGE (CV) measurements are crucial for the characterization of MIS devices. Accurate CV measurements can be challenging for devices with gate currents, however. Measurements of the devices' impedance, for example, yield too little information to determine all parameters relevant for leaky devices. Data important for the modeling of MIS devices comprise the resistance of the electronic system R_s, the resistance of the barrier R_p, and its capacitance C_p (see Fig. 1). For traditional MIS devices, this problem is tackled by a specific selection of measurement frequencies, such that some circuit components are irrelevant for a given measurement [1]–[7]. To address these problems, in some cases, device characterization is done at multiple frequencies, using the assumption that the fundamental properties of the device materials are not frequency-dependent in the frequency range employed. Many common techniques utilize dual-frequency measurements or transmission-line measurements and contacts on the backside of the substrate [1]–[7]. For MIS devices, such as $LaAlO_3$–$SrTiO_3$ transistors that comprise conducting interfaces grown on insulators [8], these procedures are not applicable, however, because of the lack of back contacts. These devices can be equipped with side contacts only, and a transmission-line equivalent circuit [9], [10] has to be used to model the devices, as will be discussed in the following.

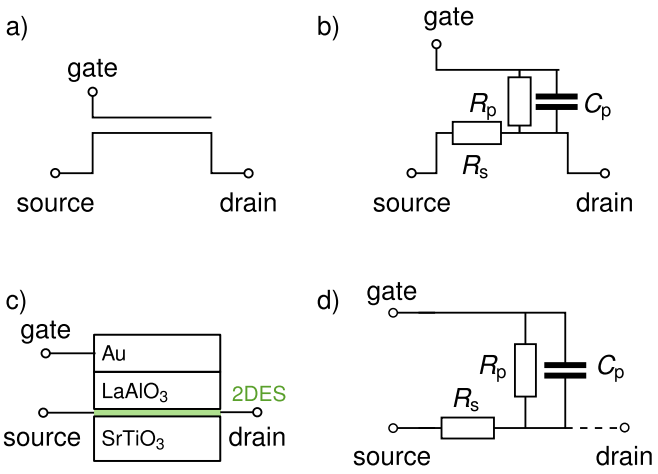

Fig. 1. Illustrations explaining the basic equivalent circuit model used. (a) Standard symbol for a MISFET. (b) MISFET symbol with added lumped circuit diagram indicating the gate capacitance (C_p) and its shunt resistor (R_p) caused by tunneling or leakage, as well as the resistance of the channel (R_s), which, while difficult to sketch, continuously connects as resistor source and drain. (c) Cross-sectional sketch of the $LaAlO_3$–$SrTiO_3$ devices investigated, illustrating the location of gate, source, and drain in the heterostructure. (d) Simple three-element equivalent circuit of a leaky device used to analyze CV measurements of MIS devices.

In the following, we describe a measurement procedure of CV characteristics that is applicable to devices with gate currents and large channel resistances. This method is based on a distributed equivalent circuit model, and it provides an exact analytical procedure to extract the device parameters from the measured data. The full device parameter set is obtained from a single-frequency measurement, such that the frequency dependence of the device parameters can also be measured.

II. Theory

For several reasons, the standard methods used to measure CV characteristics of MISFETs can be problematic. In case fundamental materials parameters of the devices are frequency-dependent, such as the dielectric constant of $SrTiO_3$ [12], measurements at multiple frequencies are difficult to interpret if their validity rests on the assumption of frequency-independent materials' properties. A second problem arises from the use of lateral contacts if the resis-

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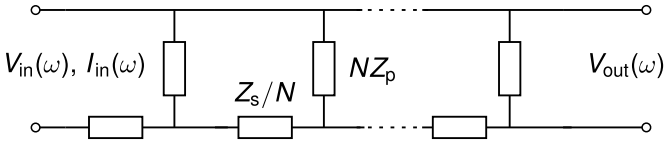

Fig. 2. Transmission-line equivalent circuit for a nonnegligible shunt impedance due to leakage currents (Z_p), nonnegligible interface conductivity (Z_s), and lateral interface contacts. The dashed line indicates a series of N similar loops. V_{in} denotes the input voltage and V_{out} denotes the output voltage as used for the frequency response.

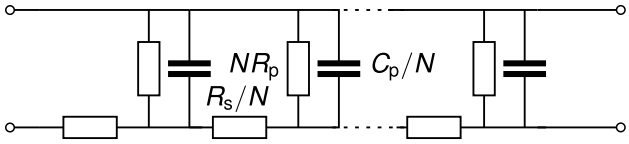

Fig. 3. Specific realization of the two-port network for a frequency-dependent impedance (C_p), leakage currents (R_p), nonnegligible interface conductivity (R_s), and lateral interface contacts. The dashed line indicates a series of N similar loops.

tance of the channel (R_s, Fig. 1) is not insignificant as compared with the gate resistance (R_p, Fig. 1). If these two resistivities are comparable, the potential gradient in the channel induced by the gate current is nonnegligible [11], [13]. Proper treatment of this gradient requires the use of a transmission-line type equivalent circuit, as shown in Fig. 2 [9], [10]. Also note that the method introduced in [9] is utilizing the advantages of the transmission-line modeling. In contrast to the method presented here, however, it uses the transmission-line equivalent circuit only to obtain a correction factor by another dc measurement to approximately calculate the device capacitance. With this, the capacitance obtained by an impedance measurement and application of a series-mode two-element equivalent circuit. As will be discussed in the following, in such a circuit, the simultaneous measurement of the transmission line's input current I_{in} and of the input and output voltages, V_{in} and V_{out}, respectively, provides the information required to analytically extract all basic device parameters, R_s, R_p, and C_p from single-frequency measurements. The frequency response of such a transmission-line circuit is given by

$$A(\omega) = \frac{V_{out}(\omega)}{V_{in}(\omega)} \tag{1}$$

and its impedance by

$$Z(\omega) = \frac{V_{in}(\omega)}{I_{in}(\omega)}. \tag{2}$$

For clarity, in the following, the dependence of the device parameters on the measurement frequency ω is noted only when specifically necessary. In the limit of an infinite number of loops ($N \to \infty$), the impedance of the equivalent circuit of the transmission line (Fig. 2) for the open-ended case is given by

$$Z = \sqrt{\zeta_s \zeta_p}\coth\sqrt{\frac{\zeta_s}{\zeta_p}}l \tag{3}$$

where $\zeta_s = (Z_s/l)$ is the impedance per unit length in the direction along the electronic system and $\zeta_p = Z_p l$ is the impedance per unit length perpendicular to it. The geometrical length of the transmission line is denoted by l [14]. The frequency response of this equivalent circuit is given by

$$A = \left(\cosh\sqrt{\frac{\zeta_s}{\zeta_p}}l\right)^{-1} \tag{4}$$

[14]. Solving (3) and (4) for the impedances per unit length ζ_s and ζ_p, we find

$$\zeta_s \zeta_p = Z^2(1 - A^2). \tag{5}$$

According to (4) and (5), the impeditivities ζ_s and ζ_p can be determined from the measured frequency response and impedance as

$$\zeta_s = Z\sqrt{(1 - A^2)}\,\text{arcosh}\left(\frac{1}{A}\right)\frac{1}{l} \tag{6}$$

and

$$\zeta_p = \frac{Z\sqrt{(1 - A^2)}}{\text{arcosh}\left(\frac{1}{A}\right)}l. \tag{7}$$

For a device described by a specific realization such as the equivalent circuit, as shown in Fig. 4, and impedances Z_s and Z_p that are determined by R_s, R_p, and C_p as

$$Z_s = R_s \tag{8}$$

and

$$\frac{1}{Z_p} = \frac{1}{R_p} + i\omega C_p. \tag{9}$$

We, therefore, find that

$$R_s = \text{Re}\left(Z\sqrt{1 - A^2}\,\text{arcosh}\left(\frac{1}{A}\right)\right) \tag{10}$$

$$R_p = \left(\text{Re}\left(\frac{\text{arcosh}\left(\frac{1}{A}\right)}{Z\sqrt{1 - A^2}}\right)\right)^{-1} \tag{11}$$

and

$$C_p = \text{Im}\left(\frac{\text{arcosh}\left(\frac{1}{A}\right)}{\omega Z\sqrt{1 - A^2}}\right) \tag{12}$$

where $\text{Re}\,(x)$ and $\text{Im}\,(x)$ are the real and imaginary parts of the quantity x. Using (10)–(12), the device parameters $R_s(\omega)$, $R_p(\omega)$, and $C_p(\omega)$ can, therefore, be analytically derived from simultaneous measurements of the frequency response $A(\omega)$ and of the impedance $Z(\omega)$.

III. Measurements

A. Experimental Methods

In the measurements, the impedance $Z(\omega, T)$ and frequency response $A(\omega, T)$ were obtained by simultaneously measuring V_{in}, V_{out}, and I_{in}. The voltages were amplified with high impedance, low-noise preamplifiers (Stanford Research SR 560), and measured with a lock-in amplifier (Zurich Instruments HF2LI). The current was obtained by measuring the

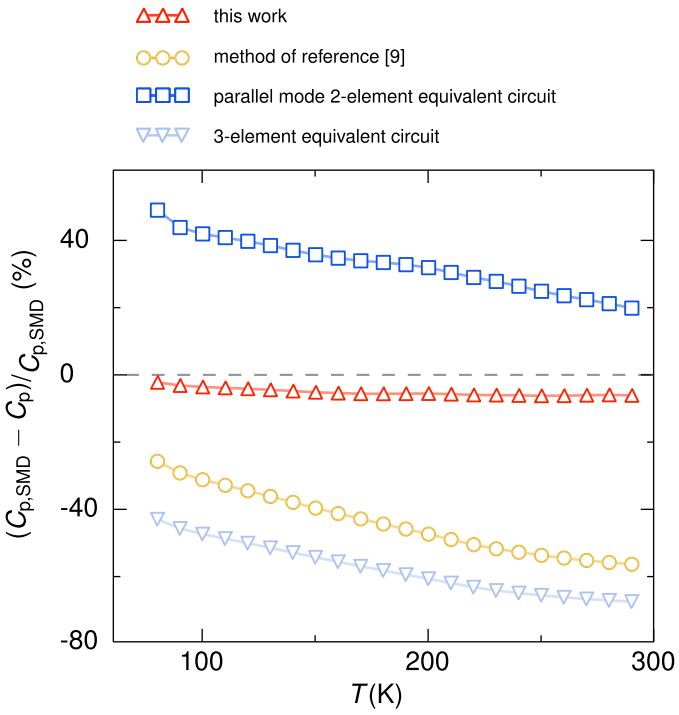

Fig. 4. Results of test measurements, analyzing a lumped circuit of ten discrete RC loops. The figure shows the temperature-dependent relative deviation of the extracted capacitance from the capacitance as used for the test circuit. The models refer to the three-element equivalent circuit shown in Fig. 1 as it is shown (squares) and a series mode two-element equivalent circuit (upside-down triangles). The yellow circles refer to the dc-correction method [9] and the red triangles refer to the presented method, thus the transmission-line equivalent circuit shown in Fig. 3 in the limit of infinitely many RC loops. The capacitance of the single capacitor was measured with an *LCR*-meter and is represented by the dashed line, as all other values are scaled relative to it.

voltage drop at a shunt resistor of a current preamplifier (1 kΩ, Zurich Instruments HF2CA) by a second lock-in amplifier (Zurich Instruments HF2LI). Both lock-in amplifiers shared one internal oscillator to ensure precise phase coherence of the measured signals.

B. Control Measurements

To explore the practical applicability of the presented method, we applied it to a test circuit of lumped linear devices and to $LaAlO_3$–$SrTiO_3$ FETs, the CV characteristics of which are notoriously difficult to measure. The test circuit was realized using ten nominally identical RC loops, each of which consisted of a ceramics capacitor $C_{p,i}$ (22 nF at 300 K) and two metal film resistors $R_{s,i}$ (33 kΩ at 300 K) and $R_{p,i}$ (3.3 MΩ at 300 K). The resistors were chosen, such that the total R_s of the circuit and the total R_p were approximately equal. The frequency for this measurement was 2 kHz. This frequency was chosen as it is so low that the conventional measurement procedures based on standard two-element circuit approximations would fail. The resistances R_s and R_p, and the capacitance C_p were simultaneously varied by cooling the test circuit to ∼50 K. The test circuit allowed to compare the values of $R_s(T)$, $R_p(T)$, and $C_p(T)$ derived from the measurements of $A(\omega, T)$ and $Z(\omega, T)$ as presented

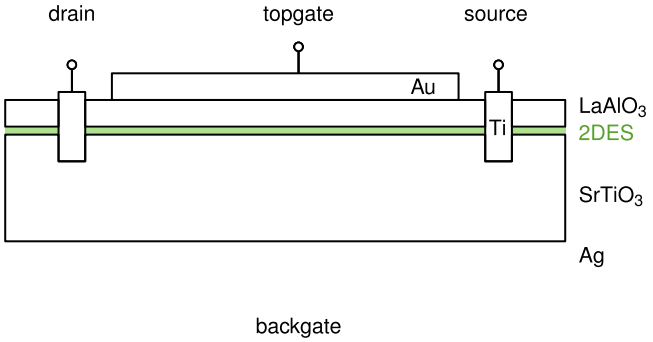

Fig. 5. Schematic representation of the $LaAlO_3$–$SrTiO_3$ sample used for the test measurements. The back-gate contact was used to modulate the charge carrier density at the interface 2-D electron system while the top-gate contact was used for the measurement of the impedance and the transfer function, respectively.

earlier to the values obtained by conventional measurements of the individual, separated components. During cooling, R_s and R_p varied by the factors of ∼5. The measured data of the test circuit were analyzed with the model shown in Fig. 2, and for reference also using the model presented in Fig. 1 and an up-to-date method for estimating the capacitance that also utilizes the transmission-line model [9]. Fig. 4 shows as a function of temperature the relative deviation of the measured capacitance of the test circuit as evaluated by using several different models from the temperature-dependent capacitance as determined for the individual capacitor. As is evident from Fig. 4, the transmission-line measurement method yields accurate values of C_p, whereas the capacitance determined using the three-element equivalent circuit (Fig. 1) or the advanced estimations method [9] deviates over a large parameter range almost as strongly as if the channel resistance was neglected at all (parallel mode two-element equivalent circuit).

In a second control experiment, a discrete $LaAlO_3$–$SrTiO_3$ FET [11], [15], [16] with five monolayers of $LaAlO_3$ grown on $SrTiO_3$(001), a gold top-gate contact, and interface contacts made of Ti were investigated (Fig. 5). The charge carrier density at the $LaAlO_3$–$SrTiO_3$ interface was modulated via a back-gate voltage (V_{bg}), and the interface resistance (R_s) was biased into the range of the $LaAlO_3$ leakage resistance (100 kΩ at −300 V and 0.3-mm^2 gate area). Using the transmission-line measurement method, the interface resistance R_s was measured as a function of V_{bg}, and then compared with the result of a direct dc measurement of R_s. These measurements were done at 4 K for the backgating to benefit from the large dielectric constant of $SrTiO_3$ at low temperatures. The measurement frequency was 29 Hz. This frequency was chosen as it is low and it enables the lock-in amplifier to use its internal sinc-filters. The results are shown in Fig. 6, together with $C_p(V_{bg})$, which varied by a factor of 3 over the bias regime. The transmission-line measurement method yields accurate results in this case as well; the values of R_s agree over the whole bias regime, as shown in Fig. 6. Finally, we note that the method presented offers a procedure to accurately measure the CV characteristics of devices for

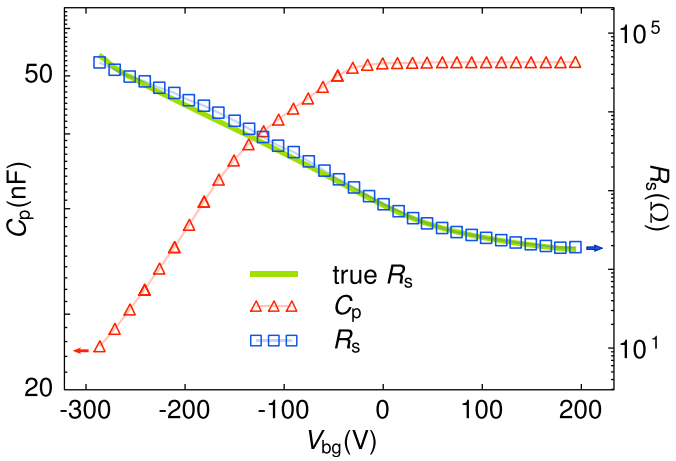

Fig. 6. Results of test measurements using a $LaAlO_3$–$SrTiO_3$ FET. The figure shows $C_p(V)$ and $R_s(V)$ measured with the method and $R_s(V)$ as obtained from a direct transport measurement.

all cases in which the output voltage $V_{out}(\omega)$ is large enough to be measured. Aside from this requirement, the method is applicable to devices of any area or leakage currents.

IV. Conclusion

A method has been developed to measure gate capacitances of leaky FETs with large channel resistances. This analytically derived method is based on a transmission-line equivalent circuit and uses measurements of the input and output voltages of the channel. It does not require back contacts for contacting the interface electron system. Experimental tests of the model using a test circuit and a state-of-the-art $LaAlO_3$–$SrTiO_3$ FET demonstrate the validity of the model and its applicability to oxide-electronic devices. Because this method does not require measurements at several frequencies or in restricted frequency regimes, it is appropriate for measurements of $CV(\omega)$ characteristics of leaky devices over extended frequency ranges.

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