

All Polymer FETs Direct-Written on Flexible Substrates Achieving MHz Operation Regime

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(Invited Paper)

Abstract—We report the successful combination of digital, direct-writing techniques, such as inkjet printing and femtosecond laser writing in order to fabricate megahertz operating, all-polymer FETs on flexible substrates without the use of any mask. By a control of the layout of the device, maximizing the ratio between the channel area with respect to the total gate overlap area through a simple interdigitated scheme, the frequency of transition f_T for an n-type polymer FET can be enhanced up to 4.9 MHz.

Index Terms—Flexible electronics, frequency of transition, high-frequency organic electronics, organic FETs, polymer semiconductors.

I. INTRODUCTION

ORGANIC semiconductors have been for long representing one of the most interesting options for the development of large-area and flexible electronics applications, spanning from lightweight, portable electronic devices to healthcare and wearable systems [1]–[5]. Such interest is determined by the wide library of materials available and in continuous development through chemical tuning, the low temperature processing, making them compatible with cheap plastic foils, and the mechanical robustness [6]–[8]. Ultimately, cost-effective manufacturing through scalable techniques, such as printing, is one of the most interesting perspectives for the successful deployment of such technology [9]–[12]. To this extent, solution-processable polymers offer the possibility to more easily tune the rheology properties of functional inks, thus simplifying to a certain extent the control of flows in printed patterns and uniformity with respect to small molecules. The drawback of a more demanding synthesis required for polymers is being faced by developing greener and shorter synthetic routes [13].

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Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

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While being more prone to intrinsic disorder, field-effect mobility μ in solution deposited solid-state polymer thin films is steadily increasing, consistently reaching the range between 1 and 10 $\text{cm}^2/(\text{V} \cdot \text{s})$ for both holes and electrons [14]–[16]. The latter progress is possible thanks to the recent development of high-performance co-polymers alternating donor and acceptor moieties along the backbone [17]–[19], by the fine control of the films self-assembling [20]–[25] and by the synthesis of planarized backbones with intrinsic barriers to conformational disorder [26], [27]. The typical figures of merit of polymer FETs, such as μ , are most of the time obtained from dc electrical characteristics, in device geometries characterized by a high level of capacitive parasitism [28], while limited attention is paid to the frequency behavior of organic FETs in general. Moreover, the patterning resolution of most state-of-the-art printing processes is of the order of tens of microns, posing a constraint on the critical features that can be realized. Therefore, poor maximum operating frequencies are typically associated with printed polymer devices for flexible electronics, introducing strong limitations to the possible applications [29].

To overcome such limitation several high resolution processes, characterized by the different levels of scalability, have been recently proposed for the patterning of organic FET electrodes, such as self-aligned inkjet printing [30], high-resolution gravure printing [31], and roll-to-roll compatible nanoimprinting [32]–[34]. Alternatively, the combination of digital, direct-writing techniques, such as inkjet printing and femtosecond (fs-laser) machining offers a versatile methodology for the improved patterning resolution of metallic lines for organic FETs [35], [36], compatibly with screen-to-screen and web-based processes [37], [38].

It is more rare to find in the literature examples of printed polymer FETs, which are totally based on organic materials, and which can thus benefit by additional features, such as semi-transparency [39], [40], and possibly by improved compatibility among materials. Moreover the maximum operating frequency obtained in a fully-organic device up to now is 25 kHz [39]. Such frequencies are not compatible with fast addressing electronics, required in all organic systems, such as high-resolution flexible displays [41], wireless communication devices [42], and Radio Frequency Identification (RFID)-based item-tracking systems [43]. It is therefore important to develop fast devices which maintain compatibility with plastic substrates and scalable processes.

In this paper, we demonstrate all polymer FETs fabricated by combining digital, direct writing techniques, such as inkjet and laser machining, which achieve a frequency of transition f_T , i.e., the frequency at which the current gain is equal to 1, of 4.9 MHz. This is the highest reported f_T to date for a printed all-polymer-based device, fabricated on a plastic substrate without the use of any mask. Such result can pave the way for the fabrication of flexible logic circuits with enhanced clock rate, for applications requiring fast addressing circuits, and for enhanced bandwidth amplifiers to enable integrated signal amplification in printed wearable and large-area sensors.

II. EXPERIMENT

A. Materials and Films Depositions

For the fabrication of devices, 125- μm -thick PEN Teonex Q65FA (DuPont TeijinFilms) was adopted and cleaned by simple rinsing with acetone and isopropanol before the deposition process. The entire printing process was performed through a Dimatix Materials Printer-2831 using 10-pl volume drops cartridges driven with a two voltage levels waveform. Poly(3, 4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS Clevios pjet700) was purchased from Heraeus and used for the deposition of the source, drain, and gate electrodes. The PEDOT:PSS printed bottom lines were baked at 110 $^\circ\text{C}$ for 30 min in air. Branched poly(ethyleneimine) (PEI) was purchased from Sigma Aldrich and dissolved in 2-methoxyethanol with a concentration of 0.1% in weight. The solution was spun on the PEDOT:PSS bottom lines before the fs-laser patterning, dripping 80 μl of solution at 5000 rpm for 1 min and then drying the film at 110 $^\circ\text{C}$ for 10 min in air. Poly{[N, N'-bis(2-octyldodecyl)naphthalene-1, 4, 5, 8-bis(dicarboximide)-2, 6-diyl]-alt-5, 5'-(2, 2'-dithiophene)} [P(NDI2OD-T2)] was purchased from Polyera Corporation and dissolved in mesitylene with a concentration of 5 g/l. After the deposition, the film was annealed at 120 $^\circ\text{C}$ for 12 h in nitrogen atmosphere. Poly(methyl methacrylate) (PMMA) was purchased from Sigma Aldrich (average Mw \approx 120000) and dissolved in *n*-butyl acetate with a concentration of 60 g/l. The solution was spun at 2000 rpm, acceleration 1000 rpm/s, for 1 min in air and then annealed at 80 $^\circ\text{C}$ for 30 min in nitrogen atmosphere. After the gate printing the device was annealed at 120 $^\circ\text{C}$ for 12 h in nitrogen atmosphere.

B. Fs-Laser System

The ablation process was carried out through a mode-locked Yb:KGW (ytterbium doped potassium gadolinium tungstate) laser at 1030 nm (Pharos). The laser produces a sequence of ultra-short pulses of 280 fs of width and a repetition rate of 500 kHz. Samples were fixed on a highly precise, programmable, 3-D moving stage (Aerotech ABL1000), with a resolution of 2.5 nm, a maximum travel speed of 300 mm/s, a maximum limit in vertical direction of 50 mm, and a maximum limit in horizontal directions (*x*- and *y*-axis) of 100 and 150 mm, respectively; 50 times magnification lens (Mitutoyo Plan Apo NIR) was used for the focusing of the laser beam.

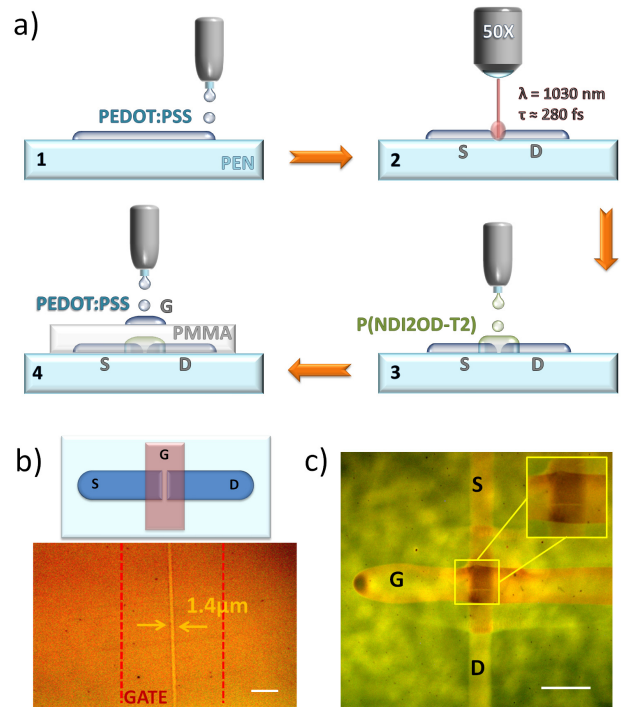


Fig. 1. (a) Sketch of the direct writing process adopted for the devices fabrication. First, PEDOT:PSS lines are inkjet printed on a PEN flexible substrate (1) and patterned through fs-laser ablation (2). For this step pulses with duration of 280 fs and a wavelength of 1030 nm are adopted. For the deposition of the semiconductor (3) and the gate electrode (4) inkjet printing is then subsequently used. (b) Sketch and optical microscopy picture of an ablated channel in a PEDOT:PSS printed line with $L \approx 1.4 \mu\text{m}$. Red square in the sketch and the red dashed lines in the microscopy picture indicate the gate occupancy of the complete device, defining the first geometry investigated, geometry 1. The scale bar is 10 μm . (c) Example of an all polymer FET with the downscaled ablated channel and, in the inset, zoom of the active area of the device. The scale bar is 200 μm .

C. Electrical Measurements

The electrical characterizations of the devices were performed in nitrogen atmosphere on a Wentworth Laboratories probe station. For the dc measurements an Agilent B1500A Semiconductor Parameter Analyzer was adopted. The linear and saturation mobility values were calculated using the gradual-channel approximation. For the calculation of the ON-OFF ratio, $I_{\text{DS-OFF}}$ was taken at $V_G = -5 \text{ V}$ and $I_{\text{DS-ON}}$ at maximum V_G value for both linear and saturation regime. For the ac measurements, a network analyzer (Agilent ENA series) with a signal modulation in the 100 to $3 \times 10^7 \text{ Hz}$ range and with a peak-to-peak amplitude of 632 mV was used, forcing the dc bias with a source meter (Agilent B2912A precision source/measure unit). For the f_T extraction, the devices were characterized in saturation regime ($V_G = V_D$). The dc bias was set at 30 V. A transimpedance amplifier, with a gain $G = 2 \times 10^3$, that returned an ac voltage v_{out} to the network analyzer, was used to read the ac currents produced. Further details are described in the supporting information (SI) of our previous work [24].

III. RESULTS AND DISCUSSION

In our approach, we exploit the combination of inkjet printing and fs-laser ablation, which we have previously shown to be effective in realizing metallic electrodes separated by

a high-resolution channel, with lengths from the micrometer down to sub-micrometer range [35]. Here we move to conducting and highly transparent PEDOT:PSS electrodes to demonstrate all polymer devices. We start by printing a highly conducting PEDOT:PSS ink onto a flexible PEN substrate [Fig. 1(a)], resulting upon drying in a sequence of parallel lines of approximately 60–80 μm of width and only 30 nm of maximum thickness, achieved in the middle of the line. Subsequently, a fs-laser beam with a wavelength of 1030 nm is focused through a 50X magnification lens directly on the sample surface. In these conditions, damages of the substrates are avoided up to 60 nJ of pulse energy. Uniform ablated channels in PEDOT:PSS, as shown in the optical microscopy illustration of Fig. 1(b), are realized setting a minimum pulse energy of 30 nJ and impinging on the surface with 1600 pulses/mm at a stage velocity of 10 mm/s. The length of the channel (L), obtained at 30 nJ, is approximately 1.4 μm , while longer channels can be fabricated by increasing the pulse energy [35]. For the fabrication of downscaled polymer FETs, we selected source and drain PEDOT:PSS electrodes separated by 1.8- μm long gap, produced with a pulse energy of 40 nJ, in order to reduce contact resistance effects owing to charge injection limitation in aggressively downscaled channels [44], [45], and to more easily benefit, as a consequence, from the downscaled features. As a semiconductor, we selected the very well-known P(NDI2OD-T2), a donor-acceptor co-polymer which shows good electron transporting properties and it has thus been largely studied for the realization of n -type FET devices. The latter are typically more challenging to be achieved than p -type devices due to a substantial lack of efficient and air-stable electron poor moieties until only a few years ago [46], [47]. P(NDI2OD-T2) was inkjet printed from a mesitylene-based solution in correspondence with the channel in a single printing pass, forming a very thin film of 10 nm. The solvent is chosen on the basis of the compatibility with the printing process owing to a relatively high boiling point and, as an effect of the presence of a substantial concentration of aggregates in the solution, to the good fibrillar microstructure induced in the dry solid film, which enhances charge transport properties [20], [24]. The devices are completed by spin-coating of ~ 300 -nm thick PMMA dielectric layer and by printing with PEDOT:PSS the top gate electrode with a width of 50–60 μm , thus finally completing a typical bottom-contacts, top-gate FET, an architecture which is adopted to favor charge injection and to provide optimal semiconductor-dielectric interfaces. A microscopy picture of a representative device with a single downscaled ablated channel (geometry 1) is reported in Fig. 1(c).

The transfer and output characteristics of the fabricated devices are reported in Fig. 2. The FET shows typical n -type behavior, with a modulation of the channel current I_{DS} of 10^4 in linear regime, with $I_{\text{DS-OFF}}$ down to 17.5 pA at $V_G = -5$ V. In the saturation regime the ON-OFF ratio is reduced to 10^2 as an effect of the parasitic p -type channel, which is accumulated at low-gate voltage ($V_G < 0$) and high source-drain voltage ($V_{\text{DS}} = 20$ V), owing to the intrinsic ambipolar nature of the semiconductor [48]. Remarkably, the gate leakage current is very low, at the level of the background of our setup.

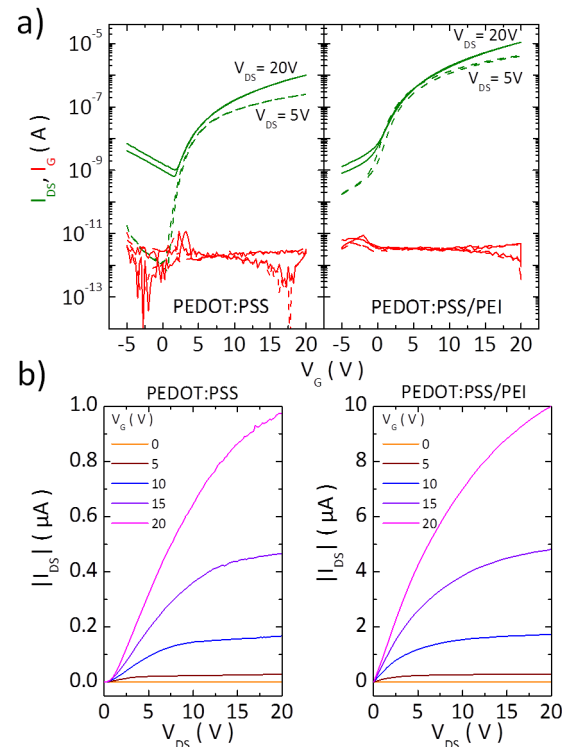


Fig. 2. (a) Transfer characteristics and (b) output of a device without PEI treatment (left), and of a device with PEI treatment (right). Red: gate leakage current. Green/black: source and drain current. The devices channel length and channel width are $L \approx 1.8$ μm and $W \approx 85$ μm .

Given that the thickness of the dielectric is 300 nm, lower than 500–900 nm of a typical top-gate solution processed FET [47], we attribute such low leakage to both the absence of sharp features at the electrodes edge, favored by the use of polymer electrodes, and to the patterning of the printed semiconductor close to the active area of the device.

From the transfer characteristic curves [Fig. 2(a) (left)] we extracted a saturation mobility μ_{sat} of ~ 0.02 $\text{cm}^2/(\text{V} \cdot \text{s})$ ($V_{\text{DS}} = V_G = 20$ V) and a linear mobility μ_{lin} of ~ 0.01 $\text{cm}^2/(\text{V} \cdot \text{s})$ ($V_{\text{DS}} = 5$ V, $V_G = 20$ V). Such FET mobilities are at least an order of magnitude lower than what can be routinely obtained with long channels defined only by inkjet printing the same PEDOT:PSS electrodes. In fact, all printed FETs, sharing a similar architecture as the devices here reported, but with longer channel length of 45 μm and thicker dielectric of 700 nm, were demonstrated to deliver average μ_{sat} of ~ 0.31 $\text{cm}^2/(\text{V} \cdot \text{s})$ ($V_{\text{DS}} = 60$ V, $V_G = 60$ V) and μ_{lin} of ~ 0.15 $\text{cm}^2/(\text{V} \cdot \text{s})$ ($V_{\text{DS}} = 5$ V, $V_G = 60$ V) [4], [39]. The strong limitation with short channels comes mainly from a correspondingly increased conductivity of the channel with respect to the long channel all printed devices and from an injection limitation, due to a Schottky barrier, of about 0.6 eV [39]. As a consequence a strong contact resistance effect is observed, as confirmed by an S-shape at low V_{DS} in the output curves [Fig. 2(b) (left)]. In order to reduce the limitation imposed by the poor injection, prior to ablation, the surface of the source and drain electrodes was treated with PEI, which is effective in reducing the PEDOT:PSS work function down to 3.88 ± 0.06 eV, as previously demonstrated by Zhou,

et al. [49]. The transfer [Fig. 2(a) (right)] and output [Fig. 2(b) (right)] characteristics of a typical laser-patterned device with the inclusion of the PEI electrode modification layer show an increase of I_{DS} of more than one order of magnitude in full accumulation, both in the linear and in the saturation regime as an effect of the improved injection. In particular, the output curves show now a clear linear regime at low V_{DS} . As a result, average μ_{sat} of $\sim 0.25 \pm 0.053 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 20 \text{ V}$, $V_G = 20 \text{ V}$) and average μ_{lin} of $\sim 0.12 \pm 0.021 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 5 \text{ V}$, $V_G = 20 \text{ V}$) are extracted. Given its positive effect, PEI is adopted in all device geometries here presented. A consequence of the contacts treatment is also the increase in the OFF currents. This can be due to two main phenomena: 1) a better matching of the Fermi energy of the PEDOT:PSS with the Lowest Unoccupied Molecular Orbital (LUMO) of the P(NDI2OD-T2) that causes a diffusion of electrons in the semiconductor [50] and 2) a doping of the semiconductor induced by the high density of electron donating amine side chains and the residual impurities identified as ethyleneimine dimers and trimers in the commercial PEI, which produces a neat increase in conductivity [51]. However, the ON-OFF ratio calculated from the transfer of Fig. 2(a) (right) in linear regime is still $\sim 10^4$, and it is slightly improved in the saturation regime, reaching 8×10^3 , because of the higher barrier for holes injection, suppressing the parasitic parallel p -channel at negative V_G s. The frequency operation of optimized short channel devices was then tested in order to extract the transition frequency f_T . f_T is a commonly adopted small signal figure of merit to estimate the maximum operative frequency of a transistor, and it corresponds to the current unity again, the frequency at which the small signal “input” gate current equals the small signal “output” channel current in short circuit condition. For frequencies above f_T the transistor behaves like a capacitor. The frequency of transition can be expressed as follows:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{g_m}{2\pi C_g}$$

where g_m represents the transconductance of the device, C_{gs} the gate to source capacitance, C_{gd} the gate to drain capacitance, and C_g the total gate capacitance [30].

We have measured an f_T up to 700 kHz (Fig. 4(a)), with a transconductance of $g_m = 2.1 \mu\text{A/V}$ and capacitances $C_{gs} = 0.25 \text{ pF}$ and $C_{gd} = 0.21 \text{ pF}$ ($C_g = 0.46 \text{ pF}$), on a device with an inkjet printed source/drain linewidth of $\sim 85 \mu\text{m}$, separated by an ablated channel of $L = 1.8 \mu\text{m}$, and with an inkjet printed gate linewidth of $\sim 50 \mu\text{m}$. Such structure features a total gate overlapping area $A_{ov} \approx 4250 \mu\text{m}^2$. The measured f_T is ~ 28 times higher than the all organic, all printed FETs previously reported [39], highlighting the positive effect in the shortening of the device channel length. Despite the improvement in f_T due to the shorter channel length, the device is limited by a wide overlap between the source/drain and gate electrodes, since their width is limited by the inkjet printing resolution. In fact, in order to control a $1.8\text{-}\mu\text{m}$ long channel, defining an active area $A_{ch} = L \times W$ of only $\sim 255 \mu\text{m}^2$, a total overlapping area A_{ov} of $\sim 4250 \mu\text{m}^2$ is present owing to the low resolution of the PEDOT:PSS lines,

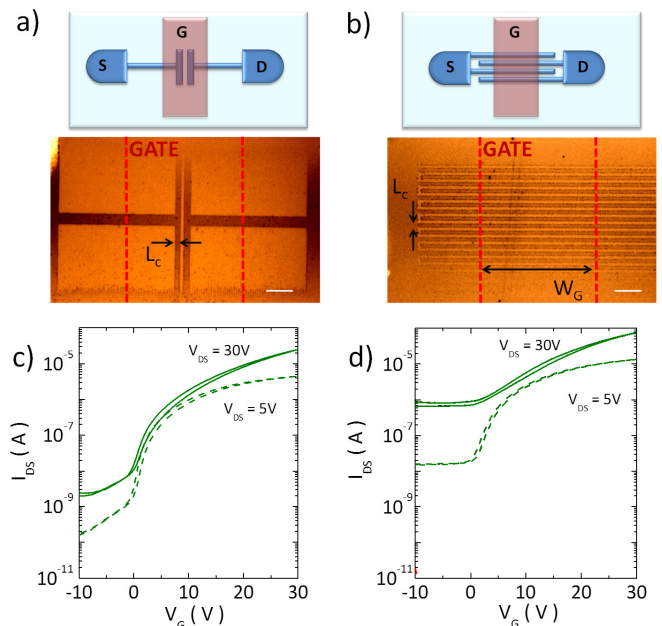


Fig. 3. (a) Sketch of the geometry 2 (top) and the microscopy picture of an $L_C \approx 3 \mu\text{m}$ patterned source drain electrodes (bottom). Dashed red line: gate occupancy. Purple square: total removed overlap area. (b) Sketch of the geometry 3 (top) and the microscopy picture of patterned source drain electrodes with 16 channels (bottom) with a minimum $L_C \approx 2 \mu\text{m}$. Red dashed line: gate occupancy. The scale bar is $10 \mu\text{m}$. (c) Transfer characteristic of a typical device with source and drain geometry (a) and $L_C \approx 3$. (d) Transfer characteristic of a typical device with source and drain geometry (b) and ten gaps.

thus resulting in high parasitic capacitive effects, drastically limiting the transition frequency. We have therefore exploited the ease of patterning allowed by fs-laser ablation in order to improve the ratio of active area with respect to the overall gate overlapping area according to two different geometries.

The first one named geometry 2 [Fig. 3(a)], consists in the removal of portions of the bottom electrodes, leading to a reduction of the parasitic capacitances. A multiple ablation line approach was used in order to remove the wide portions of lines, adopting pulse energy of 50 nJ and impinging with 1600 pulses/mm, ablating lines of $2.5 \mu\text{m}$ of width. By drawing one line per μm over $100 \mu\text{m}$ at a stage velocity of 10 mm/s, controlled and uniform rectangular areas were ablated. By adopting the same ablation parameters used to define the channel geometry in the previous case, a channel with $L = 1.8 \mu\text{m}$ separating two injection electrodes with a minimum width L_c down to $\sim 3 \mu\text{m}$, is obtained. As a result, with the same total channel area A_{ch} of $\sim 255 \mu\text{m}^2$, and a similar A_{ov} , the overlapping area affecting C_g is highly reduced down to $\sim 1064 \mu\text{m}^2$ (the full calculation is reported in the SI, Section I). The resulting FETs [Figs. 3(c) and S2.1(a) in SI], despite the strong reduction in the width of the PEDOT:PSS source and drain electrodes, show good n -type transfer and output characteristics, only slightly inferior to the device with large overlap, with $\mu_{sat} \approx 0.14 \pm 0.023 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 30 \text{ V}$, $V_G = 30 \text{ V}$) and $\mu_{lin} \approx 0.04 \pm 0.01 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 5 \text{ V}$, $V_G = 30 \text{ V}$) and I_{DS} ON-OFF ratio of $\sim 10^4$ both in linear and saturation regime. The gate leakage, as reported in the SI, is confirmed to be very low, at the level of the setup background. The lower mobility is likely due to enhanced

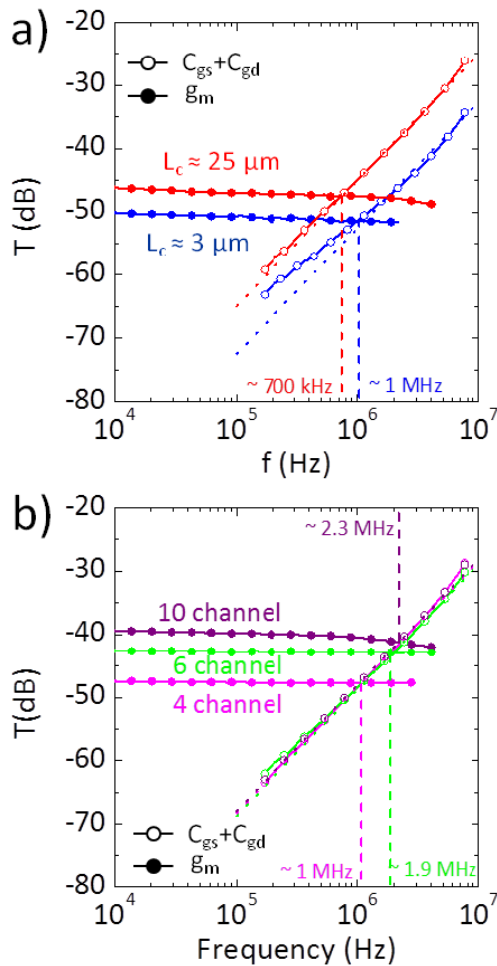


Fig. 4. (a) Frequency characterization of all-organic FETs. Blue line: geometry 2 reported in Fig. 3(a). Red line: geometry 1 reported in Fig. 1(b). (b) Frequency characterization of all-organic FETs characterized by the geometry 3, represented in Fig. 3(b), with increasing number of channel covered by the gate electrode. Pink: 4 channels. Green: 6 channels. Purple: 10 channels. The filled symbols stand for the channel signal, and the open symbols for the gate capacitance signal. For details on the f_T calculation, see experimental methods and SI of our previous work [24].

contact resistance effect, owing to the reduction in width of the electrodes, which manifest in a weak S-shape at low V_{DS} in the output curves [Fig. S2.1(a)]. By a simple estimation we can exclude the voltage drop along the source and drain contacts as the cause of the lower performance. We can also exclude that the effect is due to a reduction of L_c below the injection length of the contact that, in a current crowding model, is the fraction of the gate to contact overlap that is effectively involved in current injection [52], since we previously reported that this scales with the channel for P(NDI2OD-T2), being a fraction of it. Therefore, we tend to attribute the effect to an increased resistivity at the edge of the printed PEDOT:PSS electrode, which has a rounded shape and gets thinner and thinner toward the edge, where most of the injection takes place. Despite this limitation, the devices are characterized by a saturation mobility which is in the same order of magnitude of long-channel all printed devices [39], and produce a favorable increase in currents and transconductance. With respect to the device with larger overlap, g_m is slightly reduced, down to

$1.35 \mu\text{A/V}$ ($V_{DS} = V_G = 30 \text{ V}$), consistently with the mobility values calculated [Fig. 4(a)]. The reduction in overlap however is evident in the reduced capacitive component [Fig. 4(a)], with lower extracted $C_{gs} = 0.12 \text{ pF}$ and $C_{gd} = 0.09 \text{ pF}$ ($C_g = 0.21 \text{ pF}$), resulting overall in an improved f_T which is as high as 1 MHz , 1.5 times higher than in the large overlap FET.

Owing to the trade-off between parasitism and contact width, the improvement achieved with the second geometry is still limited. In order to further gain in operational speed we modified the contacts layout by adopting a further geometry, named geometry 3, based on an interdigitated layout [Fig. 3(b)]. The beam parameters are the same of the geometry 1 and the stage velocity is 1 mm/s . The adopted layout leaves unchanged the overlap area A_{ov} , $\sim 3600 \mu\text{m}^2$, but increases the width of the FET channel to $W = N_{\text{gap}} \times W_G$, where N_{gap} is the total number of ablated gaps and W_G is the inkjet printed gate width. This results in an increase of the total W/L ratio, and therefore to a proportional increase of A_{ch} and of the transconductance, at fixed A_{ov} . The transfer [Fig. 3(d)] and output [Fig. S2.1(b)] characteristics of a 10 channels device with $L = 1.8 \mu\text{m}$ and $W \approx 600 \mu\text{m}$, with a resulting $L_c = 3 \mu\text{m}$, show a corresponding improvement of I_{DS} of a factor of 2.6 with respect to the geometry 1 of Fig. 1(b), and of a factor of 4.4 with respect to the geometry 2 of Fig. 3(a) with $L_c = 3 \mu\text{m}$, while maintaining the same device footprint. The extracted average μ_{sat} of $\sim 0.11 \pm 0.04 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 30 \text{ V}$, $V_G = 30 \text{ V}$) and μ_{lin} of $\sim 0.025 \pm 0.005 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 5 \text{ V}$, $V_G = 30 \text{ V}$) are comparable with the average mobility of the geometry 2 with $L_c = 3 \mu\text{m}$. The I_{DS} ON-OFF ratio is lower than the other two geometries, particularly in saturation regime (10^2).

The positive effect of the interdigitation of the electrodes on f_T is evident in Fig. 4(b). The resulting C_g of 0.3 pF is lower than the value extracted from the device of the geometry 1. By varying the number of interdigitated channels, the total $C_{gs} + C_{gd}$ value is substantially constant, as demonstrated by the overlapping transfer function of the ac currents through the dielectric in Fig. 4(b) (empty circles), indicating that A_{ov} is sizing the total gate capacitance. The transconductance instead increases proportionally with the number of channels with extracted values of $g_{m-4ch} = 2.05 \mu\text{A/V}$, $g_{m-6ch} = 3.62 \mu\text{A/V}$, and $g_{m-10ch} = 4.31 \mu\text{A/V}$.

As a consequence, f_T scales with the number of interdigitated channels, being $\sim 1 \text{ MHz}$ with 4 channels, 1.9 MHz with 6 channels, and $\sim 2.3 \text{ MHz}$ with 10 channels. The interdigitated geometry is therefore demonstrated effective in improving f_T by improving the ratio between the channel area and the total overlap area. We therefore adopted this strategy to further increase f_T by interdigitating the maximum number of electrodes possible in the $80\text{-}\mu\text{m}$ wide inkjet printed PEDOTS:PSS line, so that L_c is not lower than $3 \mu\text{m}$, as in the case of the electrodes of the geometry 2.

We therefore fabricated an interdigitated source and drain pattern with 12 channels [Fig. 5(a)], which displayed $\mu_{\text{sat}} = 0.11 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 30 \text{ V}$, $V_G = 30 \text{ V}$) and $\mu_{\text{lin}} = 0.03 \text{ cm}^2/(\text{V} \cdot \text{s})$ ($V_{DS} = 5 \text{ V}$, $V_G = 30 \text{ V}$). As a result, a $g_{m-12ch} = 13.17 \mu\text{A/V}$ is obtained with an $A_{ov} \approx 4025 \mu\text{m}^2$,

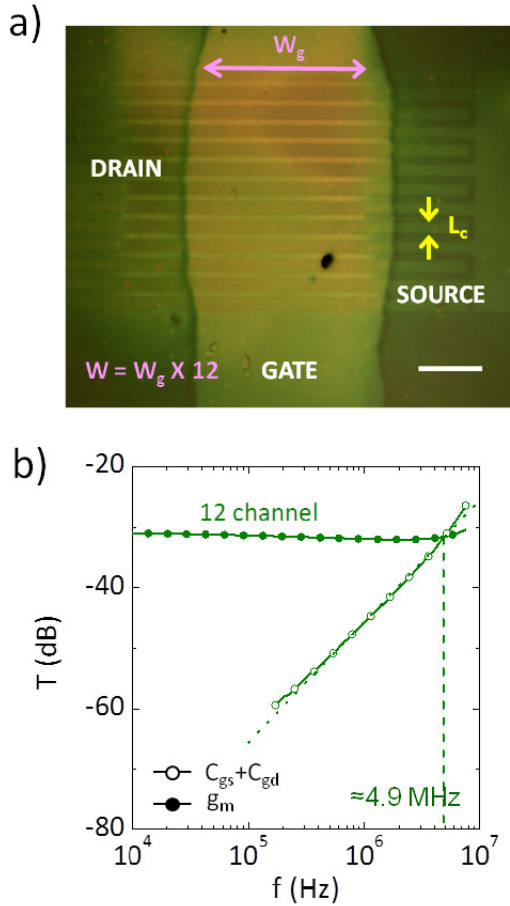


Fig. 5. (a) Optical microscopy picture of a device with interdigitated electrodes with $L_c \approx 3 \mu\text{m}$ and 12 channels and (b) its frequency characterization. Filled symbol: channel signal. Open symbol: gate capacitance signal. For details on the f_T calculation, see SI. The scale bar is $20 \mu\text{m}$.

TABLE I
SUMMARY OF THE MAIN FIGURES OF MERIT FOR THE
REALIZED DEVICES

	L (μm)	W (μm)	g_m ($\mu\text{A/V}$) ($V_{DS}=V_G=$ 30V) @ f_T	C_g (pF) @ f_T	f_T (MHz) ($V_{DS}=V_G=$ 30V)
Geometry 1	1.8	85	2.1	0.46	0.7
Geometry 2	1.8	85	1.35	0.21	1
Geometry 3	1.8	690	13.17	0.43	4.9
long channel geometry[39]	46	1180	0.96 ($V_{DS}=V_G=$ 40V)	6.16	0.025 ($V_{DS}=V_G=$ 40V)

which results in $C_{gs} = 0.24 \text{ pF}$ and $C_{gd} = 0.19 \text{ pF}$ giving a total $C_g = 0.43 \text{ pF}$, comparable to the $C_g = 0.46 \text{ pF}$ of the geometry 1, allowing to reach an f_T of $\sim 4.9 \text{ MHz}$ [Fig. 5(b)]. The results achieved with the different device geometries are summarized in Table I.

IV. CONCLUSION

We have reported a digital direct writing method for the fabrication of downscaled all-polymer FETs operating well into the MHz regime. In particular, the use of the inkjet printing process has allowed the deposition of conductive PEDOT:PSS and semiconducting P(NDI2OD-T2) for the realization of the devices electrodes and semiconductor layer, respectively. Thanks to the high resolution of the fs-ablation process, high-performance devices with source and drain electrodes separated by a single $1.8\text{-}\mu\text{m}$ long channel have been successfully realized on flexible substrates. The use of PEI functionalization of the source and drain electrodes has been proven essential for the overcoming of charge injection limitation from PEDOT:PSS electrodes. The low footprint of the device in combination with the adoption of soft, smooth, and thin polymeric electrodes have allowed the deposition of a thin dielectric layer, obtaining a good operation of the devices already at $V_G = 20 \text{ V}$, with extremely low leakage currents. Average saturation mobility of $0.25 \text{ cm}^2/(\text{V} \cdot \text{s})$ and average linear mobility of $0.12 \text{ cm}^2/(\text{V} \cdot \text{s})$ have been demonstrated, resulting in an f_T up to 0.7 MHz , limited by the low resolution of the inkjet printing process for the deposition of the gate electrodes.

In order to increase the devices f_T by reducing the parasitic effect due to the gate and source-drain overlap area, two different source and drain geometries have been investigated by exploiting the fs-laser versatility. The first one, consisting in the removal of portion of source and drain electrodes, has led to an increase of f_T up to 1 MHz as a consequence of the lowering of the gate and source-drain overlapping area and of the reduction of the parasitic overlap capacitance. The second one, consisting in the interdigitation of the source and drain electrodes, has resulted in a strong increase of f_T up to 4.9 MHz , owing to a larger W of the devices obtained with an unchanged gate and source-drain overlapping area. Such f_T is the highest reported to date for an all-polymer device fabricated on a flexible substrate and we have demonstrated that it can be reached already with an average apparent mobility of $0.11 \text{ cm}^2/(\text{V} \cdot \text{s})$. Improvement of injection properties and the use of higher mobility polymers will allow in perspective the achievement of tens of MHz operation in such polymer FETs, characterized by a simple device layout.

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