

# Reliable Time Exponents for Long Term Prediction of Negative Bias Temperature Instability by Extrapolation

Rui Gao, Azrif B. Manut, Zhigang Ji, *Member, IEEE*, Jigang Ma, Meng Duan, Jian Fu Zhang, Jacopo Franco, Sharifah Wan Muhamad Hatta, Wei Dong Zhang, Ben Kaczer, David Vigar, Dimitri Linten, *Senior Member, IEEE*, and Guido Groeseneken, *Fellow, IEEE*

**Abstract**—To predict the negative bias temperature instability (NBTI) toward the end of pMOSFETs’ ten years lifetime, power-law-based extrapolation is the industrial standard method. The prediction accuracy crucially depends on the accuracy of time exponents,  $n$ .  $n$  reported by early work spreads in a wide range and varies with measurement conditions, which can lead to unacceptable errors when extrapolated to ten years. The objective of this paper is to find how to make  $n$  extraction independent of measurement conditions. After removing the contribution from as-grown hole traps, a new method is proposed to capture the generated defects (GDs) in their entirety.  $n$  extracted by this method is around 0.2 and insensitive to measurement conditions for the four fabrication processes we tested. The model based on this method is verified by comparing its prediction with measurements. Under ac operation, the model predicts that the GD can contribute to  $\sim 90\%$  of NBTI at ten years.

**Index Terms**—Aging, bias temperature instability, interface states, lifetime, negative bias temperature instability (NBTI), oxide traps, positive charges.

## I. INTRODUCTION

Designing reliable circuits has become more difficult in recent years and one of the constraints is the negative bias temperature instability (NBTI) in pMOSFETs. The initial investigation of NBTI can be traced back to the 1960s [1]. The thick oxides ( $> 50$  nm) and low field ( $< 3$  MV/cm) used in early works [1], [2] prevent hole current flowing through the oxide. This “intrinsic” bias temperature instability follows a power

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R. Gao, A. B. Manut, Z. Ji, J. Ma, M. Duan, J. F. Zhang, and W. D. Zhang are with the School of Engineering, Liverpool John Moores University, Liverpool L3 3AF, U.K. (e-mail: z.ji@ljmu.ac.uk).

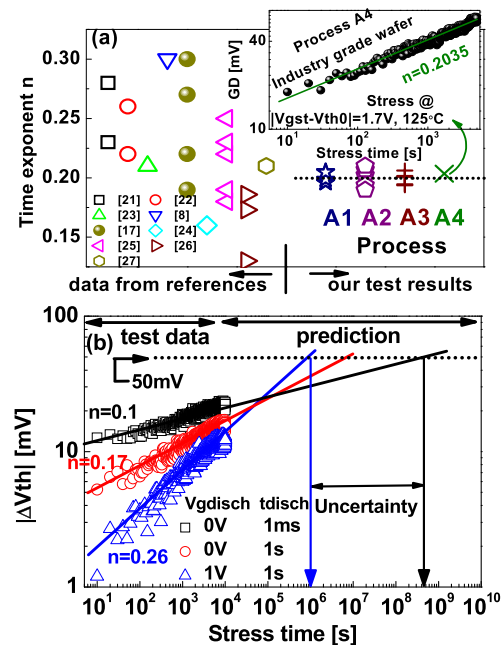
J. Franco, B. Kaczer, D. Linten, and G. Groeseneken are with imec, 3001 Leuven, Belgium.

S. W. M. Hatta is with the Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia.

D. Vigar is with Qualcomm Technologies International Ltd., Cambridge CB4 0WZ, U.K.

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**Fig. 1.** (a) Summary of time exponents reported by early works and extracted using the method proposed in this paper. Multiple points for each process (A1–A4 in Table I) represent the values from different stress voltage and temperature. The inset shows the kinetics for the industrial grade sample A4. (b) GD component measured by conventional method under different discharge voltage ( $V_{gdisch}$ ) and time ( $t_{disch}$ ). Different time exponents lead to substantial uncertainty in lifetime extraction when extrapolating to 50 mV. The stress was under  $|V_{gst}-V_{th}| = 1.2$  V.

law well, allowing its long term prediction by extrapolation, as recommended by JEDEC [3].

For thin oxides used in modern CMOS nodes, however, oxide field under typical NBTI stresses is high enough for hole current to flow through and charge the as-grown hole traps (AHT), in addition to interface state generation [4]–[12]. The AHT causes NBTI kinetics deviating from power law [9]–[12], making prediction by extrapolation problematic. To restore the power law, a common practice is to introduce a delay between the stress and measurement [13], [14], during which NBTI partially recovers [6], [14]–[19]. Even if the test data can be fitted well with a power law after such a delay, the time exponent  $n$  depends on measurement speed [14], [20]. Fig. 1(a) shows that the reported time exponent  $n$  has a wide

TABLE I  
TEST SAMPLES

	A1	A2	A3	A4
Gate	Metal	Metal	Poly-Si	Metal
Dielectric	HK stack	HK stack	SiON	HK stack
EoT(nm)	1.45	1	2.5	1.2
Nodes(nm)	45	22	45	28

spread [8], [17], [21]–[27], questioning the prediction accuracy when extrapolating based on these  $n$  values.

To extract the correct NBTI kinetics, the as-grown-generation (AG) model has been proposed [12], [28]. This model divides defects into two groups: AHTs and generated defects (GDs). AHTs are active in a fresh device, do not need an activation process, and remain the same after stress [9], [12], [28]. In contrast, the precursors responsible for GD are inactive in fresh devices, need stress-activation, and lead to an increase of defects after stress [9], [12], [28]. It has been proposed that these precursors can be hydrogen-related [2], [7], [29], [30].

AHTs and GDs can be well separated based on their different energy locations: AHTs are below the top edge of Si valance band  $E_v$ , whilst GDs are above  $E_v$  [12]. It is shown that filling AHT saturates typically within seconds [9], [12], [28] and, as a result, they should be removed from the aging kinetics. After removing the contamination by AHTs, Fig. 1(b) shows that the GD can be fitted well with a power law. After the same stress, however,  $n$  varies with the GD measurement conditions, resulting in unacceptable errors in prediction through extrapolation.

For the first time, this paper proposes a new test procedure that ensures capturing the total GDs and demonstrates that it allows the reliable extraction of the time exponent and makes the extraction insensitive to the measurement conditions. We observed that  $n$  is around 0.2 for all four fabrication processes used in this paper, as summarized in Fig. 1(a) for the processes A1–A4. We experimentally verify the prediction of the model based on this method and estimate that GD can contribute to  $\sim 90\%$  of NBTI at ten years under real use conditions.

## II. DEVICES AND TEST PROCEDURE

To investigate the process dependence of  $n$ , pMOSFETs fabricated by four different processes from two suppliers are used and summarized in Table I. They cover a wide range of samples: from processes under development to commercial processes, HKMG, and poly/SiON. Typical devices have a channel length and width of  $1 \mu\text{m} \times 1 \mu\text{m}$ . A1 was used unless otherwise specified.

The test procedure is shown in Fig. 2. After stressing under  $V_{\text{gst}}$ , an opposite polarity of gate bias ( $V_{\text{gdisch}}$ ) was applied to accelerate the discharge of as-grown traps, as used in early works [31], [32]. The low use-bias under real operation  $V_{\text{gch}}$  ( $|V_{\text{gch}}| < |V_{\text{gst}}|$ ) was then applied to refill all the traps that contribute under use condition. The pulse  $I_d \sim V_g$  curves are recorded during each step with a measurement time

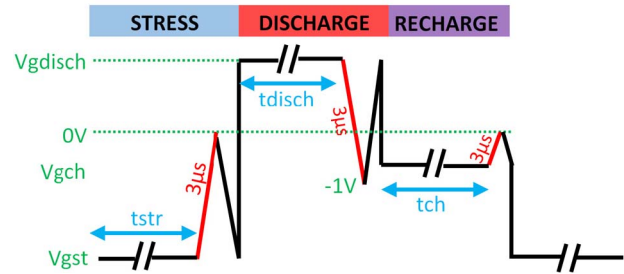


Fig. 2. Test follows a stress-discharge-recharge sequence. At the end of each step,  $\Delta V_{\text{th}}$  was monitored from a corresponding  $I_d \sim V_g$ , which was taken from the 3- $\mu\text{s}$  pulse edge with  $V_d = -0.1 \text{ V}$  applied.  $\Delta V_{\text{th}}$  was extracted at a constant current of  $500 \text{ nA} \cdot \text{W/L}$ .

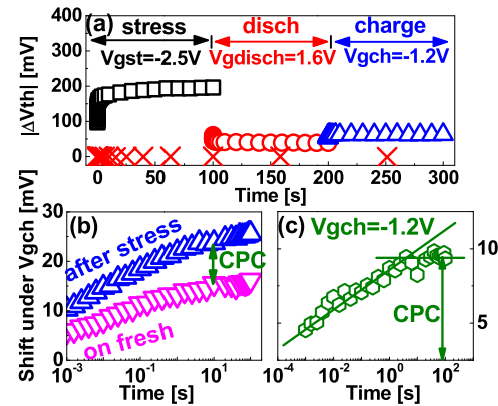


Fig. 3. (a) A typical result using a stress-discharge-recharge sequence. The symbol “x” is the result when  $V_{\text{gdisch}} = 1.6 \text{ V}$  was applied directly on a fresh device, showing that  $V_{\text{gdisch}}$  itself causes little aging. (b) Comparison of charging kinetics under  $V_{\text{gch}} = -1.2 \text{ V}$  before and after stress on the same device. The reference for the shift is  $V_{\text{th}}$  of fresh device for the “on fresh” data and  $V_{\text{th}}$  at the end of  $V_{\text{gdisch}}$  period for the “after stress” data. The difference in these two sets of data is caused by the stress-generated CPC as shown in (c). The saturation in (c) represents the completion of filling CPC. The EOT is  $1.45 \text{ nm}$  and the temperature is  $125^\circ \text{C}$ .

of  $3 \mu\text{s}$ . The threshold voltage degradation is monitored by sensing at a constant  $I_d$  of  $500 \text{ nA} \cdot \text{W/L}$  around threshold voltage. Unless specified, the temperature is  $125^\circ \text{C}$ .

## III. RESULTS AND DISCUSSION

### A. GD Component Extraction

A typical result with the procedure in Fig. 2 is shown in Fig. 3(a): the device was stressed under  $V_{\text{gst}} = -2.5 \text{ V}$  (“□”) and then discharged under  $V_{\text{gdisch}} = +1.6 \text{ V}$  for 100 s.  $V_{\text{gdisch}}$  is properly selected to make sure that there is no extrinsic degradation (“x”). The following  $V_{\text{gch}} = -1.2 \text{ V}$  recharged the defects that are chargeable under use condition (“Δ”). To measure the AHTs, the same  $V_{\text{gch}}$  was also applied on a fresh device (“∇”) in Fig. 3(b). Fig. 3(b) clearly shows that more traps were filled after stress. These extra traps can only come from the new traps generated by the preceding stress. In Fig. 3(c), subtracting the charging of fresh device from the stressed one shows that filling these generated traps saturates within 10 s under  $V_{\text{gch}} = -1.2 \text{ V}$ .

Fig. 4(a) shows the energy distribution of defects in a fresh and then stressed device by using the profiling technique

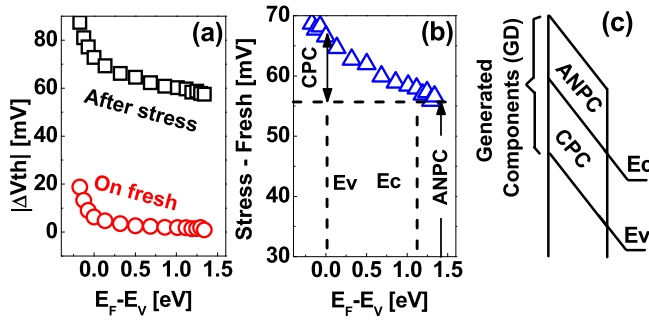


Fig. 4. (a) Comparison of the energy profiles before and after stress. (b) By subtracting the fresh profile from the stressed one, the profile for the GD was extracted. (c) Illustration of the energy range for the CPCs and the ANPCs.

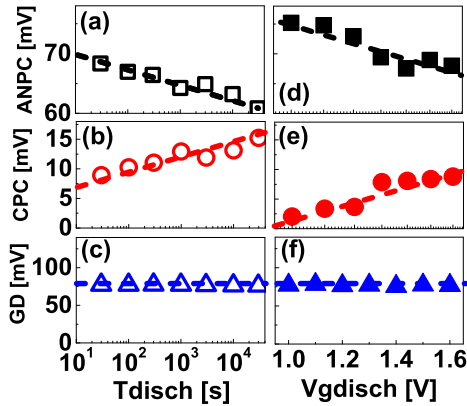


Fig. 5. Dependence on discharge conditions for (a) and (d) ANPC, (b) and (e) CPC, and (c) and (f) GD = ANPC + CPC. The discharging voltage is 1.6 V. Wherein, ANPC equals to  $V_{th}$  (end of discharge) -  $V_{th}$  (Fresh), CPC equals to  $V_{th}$  (end of recharge) -  $V_{th}$  (end of discharge), and GD is the sum of ANPC and CPC.

developed in [33]. Subtracting the fresh from the stressed one gives the distribution of GD component, as shown in Fig. 4(b). Clearly, GDs are located both within the Si bandgap and beyond Si conduction band. As observed in Fig. 3(a), charging-discharging can be cycled by alternating  $V_g$  polarity for the defects within the bandgap, so that they are referred to as cyclic positive charges (CPCs) [7]. On the other hand, the defects above Si  $E_c$  are more difficult to neutralize and they are called as antineutralization positive charges (ANPCs). What is worth noting is that the distribution in Fig. 4 originates from the oxide charge, rather than interface states. During the measurement, interface states remain constant, since  $\Delta V_{th}$  was always taken from the  $V_g$  shift corresponding to a constant  $I_d$  where the contribution of interface states to the charges change little during the measurement.

Early works often [8], [13], [14] extracted  $n$  after a delay during which NBTI partially recovered. If we measure  $\Delta V_{th}$  at the end of  $V_{gdisch}$  period, we obtain the ANPC. Fig. 5(a) shows that the ANPC reduces linearly against logarithmic discharge time [34]. This nonsaturated discharge makes the measured ANPC discharge-time-dependent and is the main challenge to the accuracy of  $n$  [8], as shown in Fig. 1(b). As a result,  $n$  should not be extracted from the  $\Delta V_{th}$  measured after an arbitrary delay and recovery.

To simplify the CPC and ANPC extraction, Fig. 2 can be used: by using the  $V_{th}$  at the end of  $t_{disch}$  as reference, the  $V_{th}$  shift during  $t_{ch}$  was measured with and without inserting a stress period. Without the stress phase, this shift only contains AHT. When the stress phase is inserted, it contains AHT + CPC. To minimize device-to-device variation, the test with stress can be performed after the test without stress. CPC can be extracted from their differences. By definition, ANPCs are the anti-neutralization positive charges, i.e., they are not neutralized at the end of discharge period, so that they equal to  $V_{th}(\text{end of discharge}) - V_{th}(\text{Fresh})$ .

When discharging time becomes longer, those traps with longer emission time lead to the linear increase of CPC against logarithmic time in Fig. 5(b). This is because, by definition, CPCs are the cyclic positive charges, i.e., they can be refilled in the recharged period, so that they equal to  $V_{th}(\text{end of recharge}) - V_{th}(\text{end of discharge})$ . The total GD component, i.e.,  $GD = CPC + ANPC$  in Fig. 5(c), is independent of discharging time. In addition, it is also independent of discharging voltage,  $V_{gdisch}$ , as shown in Fig. 5(d). Fig. 3(b) and (c) clearly show that CPC are the GDs, since they are taken from the increased  $\Delta V_{th}$  during recharge after stress when compared with that of fresh device. We cannot use this method to show that ANPC is also the GD, as the ANPC is not neutralized at the end of recovery period by definition and one cannot refill an already charged defect. To support that the ANPC is generated by the same process as CPC, Fig. 6 shows that they have the same thermal activation. Based on the common thermal activation of CPC and ANPC, on one hand, one may speculate that they have the same chemical structure and a variation of properties, such as bond length/angle, in amorphous oxides results in a distribution of energy levels. On the other hand, one may also speculate that they are different products of a common controlling aging process. Based on the past work, it is speculated that the AHT is most likely originating from oxygen vacancies [35] and it has been reported that they can react with hydrogen species [36]. For instance,  $H_2$  can be cracked by a trapped hole. Hydrogenous species are likely involved in the generation of both CPC and ANPC. For example, an increase in hydrogen exposure of the sample will significantly enhance the efficiency of the CPC generation [7].

An apparent activation energy  $E_a'$  can be extracted from Fig. 6.  $E_a'$  for both CPC and ANPC is 0.14 eV, much larger than  $E_a'$  of  $\sim 0.04$  eV reported for AHT [38], supporting the defect generation is a different process from filling as-grown traps. The extracted  $E_a'$  of 0.14 eV agrees well with the value reported by early works [37], [39]. What is worth noting is that since activation energy varies with different individual defect, the effective activation energy does not have intuitive physical meaning.

### B. Intrinsic Time Exponent for the GD Component

Once both CPC and ANPC are included in the GD, the GD becomes independent of the measurement conditions, i.e., the discharge time and voltage. This lays a solid foundation for investigating its generation kinetics. As shown in Fig. 7(a),

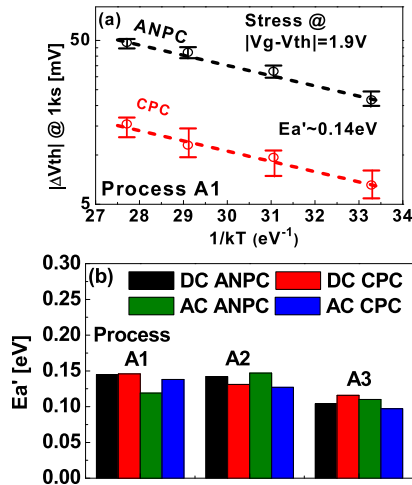


Fig. 6. (a) Effective activation energy extraction for CPC and ANPC for process A1 after stressed under dc  $|V_g - V_{th0}| = 1.9$  V for 1 ks. Wherein, CPC is taken from its saturated region in the recharge phased as illustrated in Fig. 3(c). Five devices are used for each temperature and the error bar is given. The corresponding activation energy,  $E_a$ , can be obtained by  $E_a/n = 0.7$  eV, where  $n$  is the time exponent obtained in Fig. 7(b). (b) Extracted  $E_a'$  from another two process: A2 and A3, under both dc and ac condition. Wherein, ac is with frequency of 10 kHz and duty factor of 0.5.

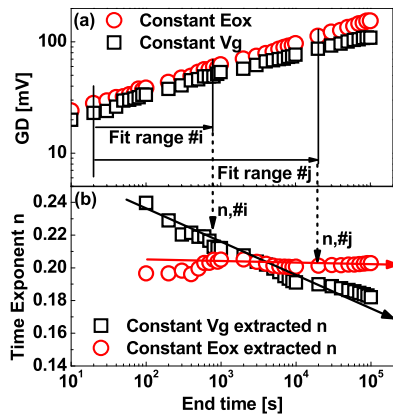


Fig. 7. (a) Kinetics for GD. (b) Extracted time exponent using data between 10 s and variable end time. The time exponent varies little after  $10^3$  s for constant Eox stress, in which the overdrive  $V_g - V_{th}$  is kept constant during the test. If the test is carried out under constant  $V_g$  stress, a gradual reduction can be observed.

the  $GD = (CPC + ANPC)$  follows power law relationship against time with  $n \sim 0.2$ . The impact of stress time range used for the extraction is further analyzed. Starting from 10 s, the end time varies between 100 s to 20 ks. Fig. 7(b) shows that, once the end-time exceeds 1 ks,  $n$  becomes independent of the range used. The total stress time is kept within 3 ks hereafter, therefore. What is worth noting is that if the test is performed under constant  $V_g$ , the widely-observed time-exponent decrease can be observed.

To study the dependence on stress conditions, GD are measured under different stress voltages and temperatures in Fig. 8(a) and (b). It is clear that  $n \sim 0.2$  is independent of stress conditions. Next, the time exponent,  $n$ , is extracted from four different processes given in Table I. The samples

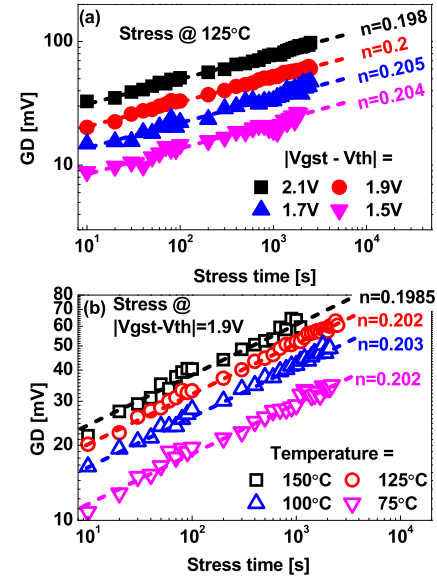


Fig. 8. Kinetics of GD component under different (a) stress voltages and (b) temperatures. The time exponent varies little around 0.2.

include both poly-Si/SiON and HKMG gate stacks, fabricated by different manufacturers, either during process development or used commercially. The result is summarized in Fig. 1(a), along with  $n$  reported by some early works [8], [17], [21]–[27]. The large spread of  $n$  between 0.13 and 0.3 reported by early works results from the dependence of  $\Delta V_{th}$  on measurement conditions, as shown in Fig. 1(b). Once the GD is independent of the measurement conditions, the spread of  $n$  is significantly reduced. For the four processes tested,  $n$  is around 0.2.

Early works [5], [40], [41] reported a reduction of  $n$  for longer stress under high temperature (up to 200 °C [5] and 400 °C [40], [41]). This could be caused by running out defect-precursors. The simultaneous annealing effect at the high temperature [42], [43] may also contribute to the reduction. Under the work temperature of 125 °C and within the typical lifetime criterion (e.g.,  $\leq 50$  mV), Fig. 8(a) shows that there are sufficient numbers of precursors that aging follows the power law well.

### C. Verify the Prediction Capability of the New Method

Although the GD can be significant under high stress bias, it is typically too small for establishing reliable NBTI kinetics under low use-bias (e.g.,  $V_g = -0.9$  V). The long term NBTI under low use-bias must be predicted by using the model established based on accelerated stresses, therefore. We now verify that the model extracted from the GD measured by the new method under high stresses can be used to predict the GD under low stresses.

The NBTI kinetics given by JEDEC [3] is

$$GD = g_0 * \exp(E_a'/kBT)(V_g - V_{th})^m t^n. \quad (1)$$

Figs. 6 and 8 already confirm GD following power law against time and Arrhenius relationship. Fig. 9 shows that the GD also follows a power law against overdrive voltage.

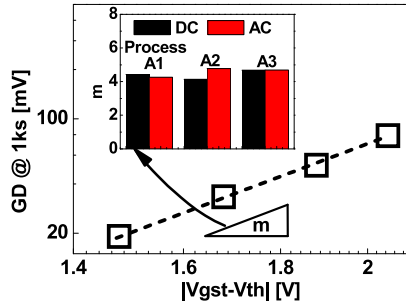


Fig. 9. GD follows a power law against  $V_g - V_{th0}$ . The data are taken from Fig. 8(a). The inset shows the extracted  $m$  value for dc and ac stress conditions for the processes A1, A2, and A3.

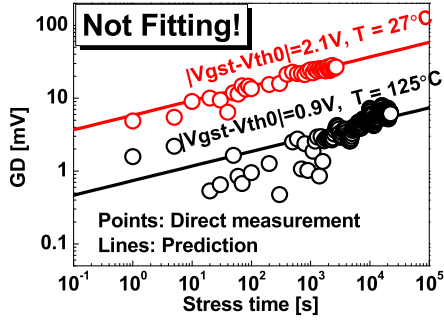


Fig. 10. Verification of the GD model. Prediction is by (1) and the measured data were not used for fitting the parameters in (1).

The GD measured by the new method under accelerated tests was used to extract  $g\theta$ ,  $Ea'$ ,  $m$ , and  $n$ . Equation (1) was then used to predict the GD under low stress conditions and Fig. 10 shows that the prediction agrees well with the directly measured GD. It should be pointed out that the measured data in Fig. 10 themselves were not used for extracting the parameters in (1).

Finally, we point out that, in addition to the GD, AHT also contribute to NBTI. The AG model of NBTI is [12], [28]

$$\Delta V_{th} = \text{AHT} + \text{GD}. \quad (2)$$

It is of interests to assess the relative importance of these two components under real use-conditions. From a practical perspective, CMOS circuits operate mostly under ac conditions with frequencies between several gigahertz for processor core, hundreds of kilohertz for L1 and scratchpad caches, and down to the kilohertz range for L2 and L3 caches [44], [45].

The similar  $Ea'$  and  $m$  from dc and ac stress condition shown in Fig. 6(b) and the inset of Fig. 9 indicate that the GD degradation is mainly driven by the effective stress time [28] (i.e., stress time  $\times$  duty factor). In Fig. 11(a), we measured the NBTI under ac (100 kHz) overdrive of  $-0.9$  V with a duty factor of 0.5. The GD component under ac stress is predicted using (1), as shown by the line in Fig. 11(a). The predicted GD is lower than the measured  $\Delta V_{th}$  and their difference comes from the contribution of preexisting traps. There are two supports for this claim. First, we measured the GD at the end of ac stress by using the new method and Fig. 11(b) conforms that they agree well with the prediction. Moreover,

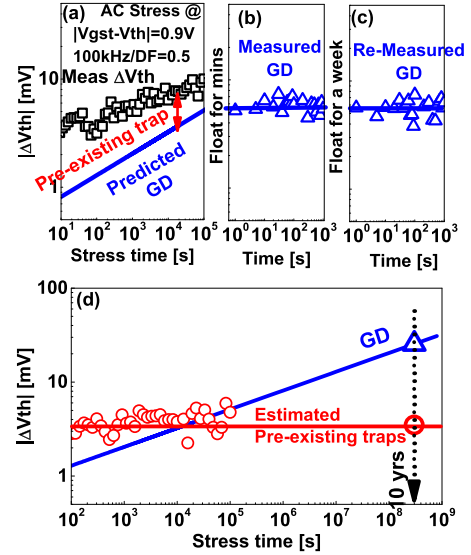


Fig. 11. (a) AC NBTI under low operation bias of  $(V_g - V_{th}) = -0.9$  V with 100 kHz and a duty factor of 0.5. (b) Predicted GD agrees well with the measurement after ac stress and (c) after floating under 125 °C for one week. (d) A comparison of AHT and GD at different time.

in Fig. 11(c), the GD was measured after one week and they remain the same, so that no defect losses [40] were observed under current test conditions. Second, subtracting the predicted GD from the measured  $\Delta V_{th}$  gives a flat line in Fig. 11(d), indicating most of the preexisting traps has been filled in seconds [9], [12], [28].

Although the rapid filling of preexisting traps makes them larger than GD initially in Fig. 11(d), at ten years, Fig. 11(d) shows that GD reaches 27 mV, while preexisting traps at  $\sim 4$  mV. As a result, the GD can contribute to almost 90% of the total NBTI toward the end of device lifetime under practical ac use-conditions.

#### IV. CONCLUSION

The time exponent  $n$  extracted by the conventional method varies with measurement conditions, leading to uncertainties in the long term prediction of NBTI through extrapolation. This paper proposes a new method for measuring the total GDs, including both CPCs in Si bandgap and ANPCs above the Si conduction band edge. By adding CPC and ANPC together, it is shown that the total GDs are independent of measurement conditions. It is found that GD can be well modeled with empirical power law relationship against time and voltage. The time exponent extracted from the GD measured by this new method is found to be around 0.2 for four processes from different suppliers. Under practical ac use-conditions, it is shown that the GD can contribute to nearly 90% of NBTI at ten years, although it is lower than AHTs initially.

#### REFERENCES

- [1] B. E. Deal, M. Sklar, A. Grove, and E. Snow, "Characteristics of the surface-state charge ( $Q_{ss}$ ) of thermally oxidized silicon," *J. Electrochem. Soc.*, vol. 114, no. 3, pp. 266–274, 1967.
- [2] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, 1977.

- [3] *Failure Mechanisms and Models for Semiconductor Devices JC-14.2*, Global Standards for the Microelectronics Industry (JEDEC), Alexandria, VA, USA, 2011.
- [4] D. S. Ang and K. L. Pey, "Evidence for two distinct positive trapped charge components in NBTI stressed p-MOSFETs employing ultrathin CVD silicon nitride gate dielectric," *IEEE Electron Device Lett.*, vol. 25, no. 9, pp. 637–639, Sep. 2004.
- [5] V. Huard, M. Denais, and C. Parthasarathy, "NBTI degradation: From physical mechanisms to modelling," *Microelectron. Rel.*, vol. 46, no. 1, pp. 1–23, 2006.
- [6] V. Huard *et al.*, "New characterization and modeling approach for NBTI degradation from transistor to product level," in *IEDM Tech. Dig.*, Dec. 2007, pp. 797–800.
- [7] J. F. Zhang, "Defects and instabilities in Hf-dielectric/SiON stacks," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1883–1887, 2009.
- [8] D. S. Ang, S. C. S. Lai, G. A. Du, Z. Q. Teo, T. J. J. Ho, and Y. Z. Hu, "Effect of hole-trap distribution on the power-law time exponent of NBTI," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 751–753, Jul. 2009.
- [9] Z. Ji, L. Lin, J. F. Zhang, B. Kaczer, and G. Groeseneken, "NBTI lifetime prediction and kinetics at operation bias based on ultrafast pulse measurement," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 228–237, Jan. 2010.
- [10] S. Deora, V. D. Maheta, and S. Mahapatra, "NBTI lifetime prediction in SiON p-MOSFETs by H/H<sub>2</sub> Reaction-Diffusion(RD) and dispersive hole trapping model," in *Proc. IRPS*, May 2010, pp. 1105–1114.
- [11] S. Mahapatra *et al.*, "A critical re-evaluation of the usefulness of R-D framework in predicting NBTI stress and recovery," in *Proc. IRPS*, Apr. 2011, pp. 614–623.
- [12] Z. Ji *et al.*, "Negative bias temperature instability lifetime prediction: Problems and solutions," in *IEDM Tech. Dig.*, Dec. 2013, pp. 15.6.1–15.6.4.
- [13] J. Hicks *et al.*, "45nm Transistor Reliability," *Intel Technol. J.*, vol. 12, no. 2, pp. 131–144, 2008.
- [14] S. Mukhopadhyay *et al.*, "Fundamental study of the apparent voltage-dependence of NBTI kinetics by constant electric field stress in Si and SiGe devices," in *Proc. IRPS*, Apr. 2016, pp. 5A-3-1–5A-3-7.
- [15] D. J. Breed, "A new model for the negative voltage instability in MOS devices," *Appl. Phys. Lett.*, vol. 26, no. 3, pp. 116–118, 1975.
- [16] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," in *IEDM Tech. Dig.*, Dec. 2003, pp. 14.3.1–14.3.4.
- [17] A. T. Krishnan *et al.*, "Material dependence of hydrogen diffusion: Implications for NBTI degradation," in *IEDM Tech. Dig.*, Dec. 2005, pp. 691–694.
- [18] T. Grasser *et al.*, "Simultaneous extraction of recoverable and permanent components contributing to bias-temperature instability," in *IEDM Tech. Dig.*, 2007, pp. 801–804.
- [19] Z. Ji, J. F. Zhang, M. H. Chang, B. Kaczer, and G. Groeseneken, "An analysis of the NBTI-induced threshold voltage shift evaluated by different techniques," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1086–1093, May 2009.
- [20] S. Mahapatra, V. Huard, A. Kerber, V. Reddy, S. Kalpat, and A. Haggag, "Universality of NBTI—From devices to circuits and products," in *Proc. IRPS*, Jun. 2014, pp. 3B.1.1–3B.1.4.
- [21] L. Jin, M. Xu, and C. Tan, "An investigation on the permanent component of NBTI degradation in a 90nm CMOS technology," in *Proc. ICSICT*, Oct. 2006, pp. 1147–1149.
- [22] A. Kerber, K. Maitra, A. Majumdar, M. Hargrove, R. J. Carter, and E. A. Cartier, "Characterization of fast relaxation during BTI stress in conventional and advanced CMOS devices with HfO<sub>2</sub>/TiN gate stacks," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3175–3183, Nov. 2008.
- [23] Z. Y. Liu *et al.*, "Comprehensive studies of BTI effects in CMOSFETs with SiON by new measurement techniques," in *Proc. IRPS*, Apr. 2008, pp. 733–734.
- [24] J.-J. Kim *et al.*, "PBTI/NBTI monitoring ring oscillator circuits with on-chip V<sub>t</sub> characterization and high frequency AC stress capability," in *Proc. Symp. VLSI Circuits*, Jun. 2011, pp. 224–225.
- [25] M. Jin *et al.*, "Impact of hydrogen in capping layers on BTI degradation and recovery in high-*k* replacement metal gate transistors," in *Proc. IRPS*, Apr. 2013, pp. PL3.1–PL3.5.
- [26] H. Kukner *et al.*, "Scaling of BTI reliability in presence of time-zero variability," in *Proc. IRPS*, Jun. 2014, pp. CA.5.1–CA.5.7.
- [27] C. Prasad *et al.*, "Bias temperature instability variation on SiON/Poly, HK/MG and trigate architectures," in *Proc. IRPS*, Jun. 2014, pp. 6A.5.1–6A.5.7.
- [28] Z. Ji *et al.*, "A test-proven As-grown-Generation (A-G) model for predicting NBTI under use-bias," in *VLSI Symp. Tech. Dig.*, Jun. 2015, pp. T36–T37.
- [29] A.-M. El-Sayed, M. B. Watkins, T. Grasser, V. V. Afanas ev, and A. L. Shluger, "Hydrogen-induced rupture of strained Si-O bonds in amorphous silicon dioxide," *Phys. Rev. Lett.*, vol. 114, no. 11, p. 115503, 2015.
- [30] C. Z. Zhao and J. F. Zhang, "Effects of hydrogen on positive charges in gate oxides," *J. Appl. Phys.*, vol. 97, no. 7, pp. 073703-1–073703-8, 2005.
- [31] V. Huard, F. Ivfonsieur, G. Ribes, and S. Brnyere, "Evidence for hydrogen-related defects during NBTI stress in p-MOSFETs," in *Proc. IRPS*, Mar. 2003, pp. 178–182.
- [32] D. Heh, P. D. Kirsch, C. D. Young, and G. Bersuker, "A new dielectric degradation phenomenon in nMOS high-*k* devices under positive bias stress," in *Proc. IRPS*, Apr. 2008, pp. 347–351.
- [33] S. W. M. Hatta *et al.*, "Energy distribution of positive charges in gate dielectric: Probing technique and impacts of different defects," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1745–1753, May 2013.
- [34] X. Wang, S.-H. Song, A. Paul, and C. H. Kim, "Fast characterization of PBTI and NBTI induced frequency shifts under a realistic recovery bias using a ring oscillator based circuit," in *Proc. IRPS*, Jun. 2014, pp. 6B.2.1–6B.2.6.
- [35] W. L. Warren and P. M. Lenahan, "Fundamental differences between thick and thin oxides subjected to high electric fields," *J. Appl. Phys.*, vol. 62, no. 10, pp. 4305–4308, 1987.
- [36] T. Grasser *et al.*, "The paradigm shift in understanding the bias temperature instability: From reaction-diffusion to switching oxide traps," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3652–3666, Nov. 2011.
- [37] S. Pae *et al.*, "BTI reliability of 45 nm high-*K*+ metal-gate process technology," in *Proc. IRPS*, Apr. 2008, pp. 352–357.
- [38] B. Djeddar, H. Tahi, A. Benabdelmoumene, A. Chenouf, M. Goudjil, and Y. Kribes, "On the permanent component profiling of the negative bias temperature instability in p-MOSFET devices," *Solid-State Electron.*, vol. 106, pp. 54–62, Apr. 2015.
- [39] J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, "NBTI: An atomic-scale defect perspective," in *Proc. IRPS*, Mar. 2006, pp. 442–447.
- [40] G. Pobegen and T. Grasser, "On the distribution of NBTI time constants on a long, temperature-accelerated time scale," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2148–2155, Jul. 2013.
- [41] T. Grasser *et al.*, "Gate-sided hydrogen release as the origin of 'permanent' NBTI degradation: From single defects to lifetimes," *IEDM Tech. Dig.*, Dec. 2015, pp. 535–538.
- [42] V. Huard, "Two independent components modeling for negative bias temperature instability," in *Proc. IRPS*, May 2010, pp. 33–42.
- [43] M. Duan *et al.*, "Defect loss: A new concept for reliability of MOSFETs," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 480–482, Apr. 2012.
- [44] R. Fernandez *et al.*, "AC NBTI studied in the 1 Hz–2 GHz range on dedicated on-chip CMOS circuits," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.
- [45] C. Liu, K. T. Lee, H. Lee, Y. Kim, S. Pae, and J. Park, "New observations on the random telegraph noise induced V<sub>th</sub> variation in nano-scale MOSFETs," in *Proc. IRPS*, Jun. 2014, pp. XT.17.1–XT.17.5.



**Rui Gao** received the B.Eng. and M. Eng. degrees from Xidian University, Xi'an, China, in 2011 and 2014, respectively. He is currently pursuing the Ph.D. degree in microelectronics with Liverpool John Moores University, Liverpool, U.K.



**Azrif B. Manut** received the B.Eng. and M.Sc. degrees from the National University of Malaysia, Malaysia, in 2001 and 2007, respectively. He is currently pursuing the Ph.D. degree with Liverpool John Moores University, Liverpool, U.K.



**Sharifah Wan Muhamad Hatta** received the M.Sc. degree from the University of Malaya, Kuala Lumpur, Malaysia, in 2009, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K.

She is currently a Senior Lecturer with the University of Malaya with a focus on reliability issues of nano-CMOS devices.



**Zhigang Ji** received the Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2010.

He is currently a Senior Lecturer with LJMU. His current research interests include characterisation and modelling on the reliability/variability related issues for CMOS and memory devices and their interactions with circuits.



**Wei Dong Zhang** received the Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2003.

He has been a Reader with Microelectronics, LJMU, since 2010. His current research interests include reliability assessment of CMOS and memory devices.



**Jigang Ma** received the Ph.D. degree in microelectronics from Liverpool John Moores University, Liverpool, U.K., in 2015.

He is currently a Post-Doctoral Research Associate and a Visiting Researcher at imec. His current research interests include modelling and characterization of emerging memory devices, CMOS devices, and GaN HEMT devices.



**Ben Kaczer** received the M.S. degree in physical electronics from Charles University, Prague, Czech Republic, in 1992, and the M.S. and Ph.D. degrees in physics from the Ohio State University, Columbus, OH, USA, in 1996 and 1998, respectively.

He joined the Reliability Group of imec, Leuven, Belgium, in 1998, where he is currently a Principal Scientist.

Dr. Kaczer is currently serving on the Editorial Board of the IEEE TRANSACTIONS ON

ELECTRON DEVICES.



**Meng Duan** received his Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K. in 2014.

He was the Research Fellow in LJMU up to 2016. He is currently with the University of Glasgow as Research Associate.



**David Vigar** received the B.Sc. degree in physics with physical electronics from the University of Bath, Bath, U.K., in 1983.

He was with several companies in the semiconductor industry. He was with Qualcomm, Cambridge, U.K. He is currently with Qualcomm Technologies International Ltd.



**Jian Fu Zhang** received the Ph.D. degree from the University of Liverpool, Liverpool, U.K., in 1982 and 1987, respectively.

He has been a Professor of Microelectronics with Liverpool John Moores University, Liverpool, since 2001. His current research interests include the aging, variability, characterization, and modelling of nanometer-size devices.



**Dimitri Linten** (SM'13) received the Ph.D. degrees in electrical engineering from the Vrije Universiteit Brussel, Brussel, Belgium, in 2006.

From 2012 to 2015, he was the ESD Team Leader with imec, Leuven, Belgium. In 2015, he became the Research and Development Manager of the Device Reliability and Electrical Characterization Group. His current research interests include device reliability including ESD for sub-10-nm CMOS and beyond Si technologies.



**Jacopo Franco** received the Ph.D. degree from Katholieke Universiteit, Leuven, Belgium, in 2013.

He is currently a Researcher with imec, Leuven. His current research interests include the reliability of high-mobility channel transistors for future CMOS nodes and on variability issues in nanoscale devices.



**Guido Groeseneken** (F'05) received the Ph.D. degree in applied sciences from Katholieke Universiteit Leuven (KU Leuven), Leuven, Belgium, in 1986.

He has been with imec, Leuven, since 1987. He has also been a Professor with KU Leuven since 2001.