The Trench Power MOSFET: Part I—History, Technology, and Prospects

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(Invited Paper)

***Abstract*— The historical and technological development of the ubiquitous trench power MOSFET (or vertical trench VDMOS) is described. Overcoming the deficiencies of VMOS and planar VDMOS, trench VDMOS innovations include pioneering efforts in reactive ion etching and oxidation of the silicon trench gate, polysilicon fill and recessed etchback, unit cell and distributed voltage clamping to protect the trench gate, and scaling active cells to high densities using deep submicron fabrication. Thereafter, gate–drain engineered trench VDMOS improved high-frequency switching capability with lower gate charge utilizing nonuniform gate oxides, field shaping, and charge balancing (superjunction, RSO) methods. The recent adaptation of trench gates in wide bandgap unipolar devices is also described.**

***Index Terms*— Avalanche breakdown, bipolar, bipolar junction transistor (BJT), cell density, charge balance, channel density A/W, deep p+, double diffusion, epitaxial layer, gate charge (Q_G, Q_{GD}), parasitic JFET, planar, power device packaging, power dissipation, power MOSFET, power transistor, punchthrough, reach-through, RSO, silicon, specific on-resistance ($R_{DS}A$), split trench gate, super junction, stepped gate, trench etch, trench thick bottom oxide (TBOX), trench VDMOS, $V_{(br)}$, VMOS, voltage clamping, wide bandgap (WBG).**

I. Introduction

AGAINST all expectations in its technological development and commercialization, the trench power MOSFET ultimately emerged as one of the world's most ubiquitous semiconductor devices. Facing daunting challenges in device design, fabrication, material issues, and device reliability, the trench gate MOSFET defied the fundamental premise that an MOSFET could only be reliably manufactured on the surface of a silicon wafer, and never along a vertically etched trench sidewall. Ultimately, its skeptics were proven wrong. Three decades later, the trench power MOSFET has grown into a 3 billion dollar annual market [1], [2] with well over 100 billion units shipped worldwide since inception.

Today, applications of the trench MOSFET are expansive, ranging from computers, televisions, and cell phones, to automobiles, motor drive, and critically preventing overheating of lithium ion batteries [3]. Trench fabrication technology has also been repurposed throughout the semiconductor industry into MEMs [4], and as trench gates and trench contacts used in trench IGBTs [5], [6], trench superjunction MOSFETs [7], in lateral trench MOSFETs and power integrated circuits [8], and more recently in wide-bandgap power semiconductor devices.

II. Background

Until the late 1970s, the bipolar junction transistor (BJT) was the only solid-state electron device capable of operating as a nonlatching power switch. Unlike thyristors, which lose gate control when triggered into a conducting state [9], the BJT can (subject to certain limitations) be turned ON and OFF "at will" by controlling its input base current. Despite its benefits, power bipolar transistors were limited in speed [10]–[12], required high base drive currents [13], [14], and were notoriously difficult to parallel [15], being subject to both thermal runaway [16] and second breakdown [17]–[20].

Motivation for the development of a power MOSFET alternative to the BJT included the promise of high speed switching [21], [22], high input impedance, and the ability to parallel or scale devices without the risk of current hogging or thermal runaway. Unfortunately, lateral (planar) MOSFET designs were not well suited for power applications, limited by punchthrough breakdown (drain induced barrier lowering) [23], snapback, and by field-plate-induced impact ionization producing localized avalanche in the vicinity of the gate to drain overlap [24]. Channel length and breakdown issues aside, because photolithography at the time was limited to large linewidths of several micrometers, integrating the transistor gate width needed to fabricate low ON-resistance devices was not practically achievable in any reasonable die size or cost.

A. V-Groove VDMOS

Somewhat ironically, the merger of an MOS insulated gate transistor with a vertical BJT device structure overcame

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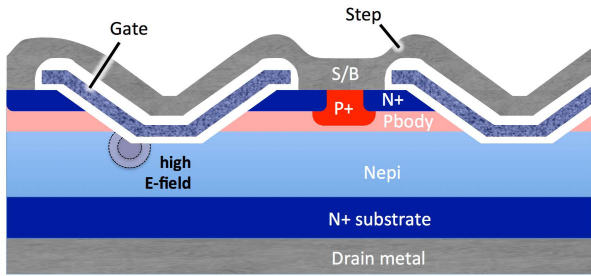

Fig. 1. Cross section of a v-groove VDMOS or VMOS. Unlike VMOS in logic ICs having a topside drain, the power device is inverted comprising a diffused source formed within an epitaxial drain.

the limitations of both progenitor devices. Originally created for realizing logic in digital ICs [25]–[27], the new and inventive device, the v-groove power vertical DMOSFET or VMOS [28]–[31] as shown in Fig. 1, comprised a vertical conduction majority carrier-based field effect device with a channel length determined not by photolithography, but by two diffusions.

Using a dopant profile borrowed from the BJT, the VMOS employs a double-diffused body with a negative concentration gradient comprising a deeper boron-doped diffused p-type body region and a shallower n^+ diffusion of arsenic or phosphorus as source formed within an n-type epitaxial drain. After double diffusion, a v-groove is chemically etched to transect the emitter–base and base–collector junctions of a diffused BJT, covering the entire BJT base with a thermally grown gate oxide and a metal or polysilicon gate electrode. To inhibit snapback breakdown, the VMOS is designed to intentionally and permanently disable bipolar conduction [32] using an integral source-to-body short (i.e., shorting the emitter-to-base of the parasitic BJT) located throughout the device, optionally by v-groove contact [33].

During MOS field effect operation, the gate is biased to a defined potential, either to inhibit or induce an inversion region across the diffused base or "body" region to control conduction. In its OFF state, the double diffused dopant profile's negative concentration gradient shifts most of the resulting depletion spreading out of the MOSFET's body into the lightly doped epitaxial drain, thereby eliminating the risk of punchthrough breakdown and short-channel effects. In its ON state, conduction is primarily vertical, where electrons flow from the n^+ source, across the p-type body under the v-groove gate and into the n-type epitaxial layer where they spread laterally before reaching the n^+ substrate and drain contact. The device's threshold is set by the peak concentration of the net body doping profile and accurately controlled by "double diffusion," i.e., two successive high-temperature diffusions.

V-groove n-channel double diffused MOSFETs may be operated as a power switch in a low ON-resistance state by applying a high positive gate bias [34]–[36], or as a current source, analog mux, or amplifier by applying a gate potential slightly above threshold [37], [38]. The term DMOSFET or simply DMOS was later adopted to generically describe any insulated gate field effect device, lateral or vertical, using sequential diffusions or nonuniform channel concentration. For its time, the VMOS was unique, utilizing the principle of double diffusion for MOS devices as well as representing one of the first submicrometer channel MOSFETs ever fabricated [25].

B. Vertical DMOS ON-State Resistance

When operated as a power switch in its linear region, the ON-state resistance of vertical current flow MOSFETs such as VMOS (and all related forms of VDMOS) can be modeled as the linear sum of series-connected lumped resistive elements (some of which may be zero resistance depending on a particular device's construction). Total die on resistance (excluding package resistance) includes varying degrees of contributions from the following elements: top metal resistance R_{metal}, metal-to-silicon contact resistance R_{contact}, source diffusion resistance R_{source}, the DMOS channel resistance R_{ch}, any accumulation layer resistance R_{acc} (formed from an overlap of the gate over portions of the epitaxial drain), JFET pinch resistance R_{jfet} (as applicable), epitaxial drain resistance R_{epi}, and substrate resistance R_{sub}.

Some of these components, such as accumulation layer resistance, JFET resistance, and portions of the epitaxial layer (where current is spreading), involve the interaction of 2-D phenomena. Top metal resistance may also exhibit 3-D effects interacting with packaging depending on the number and placement of bond wires. As such, the 1-D lumped element resistance model is only an approximation, requiring curve fitting of model parameters to match measured results. Full 2-D (and in some cases 3-D) device simulations are necessary to accurately account for all the phenomena.

Pragmatically, most vertical devices can be modeled by considering only two primary components—the epitaxial drain or "drift" resistance (which depends on epitaxial thickness and concentration) and the VDMOS channel resistance. Derived from the equation $I_D = (\mu\, C_{\text{ox}} W/L_{\text{ch}})(V_{\text{GS}}–V_t)V_{\text{DS}}$ for linear region operation of an MOSFET [39], it is insightful (and useful) to separate channel resistance R_{ch} into the product of a geometric factor [A/W] and an electrical channel resistivity term [R_{ch}W], i.e., where R_{ch} = [A/W] [$R_{\text{ch}}W$] /A and where brackets [ ] denote a defined figure of merit (FOM).

Channel density [W/A] (with units of cm^{-1}) describes how much MOS gate width W can be squeezed into a fixed active area, and A describes the portion of the die area A_{die} dedicated for fabricating active VDMOS devices (neglecting any die real estate lost to the device's high-voltage edge termination, gate bussing, and gate pad). In cellular VDMOS designs, an active transistor cell of area A_{cell} is repeated in multiple instances, i.e., n_{cells} times, to form a device having a total active area $A = \text{n}_{\text{cells}} A_{\text{cell}}$. Since the mid-1980s, cellular-based VDMOS devices are generated automatically using commonly available CAD tools.

As a convenient reexpression of channel transconductance [40], channel resistivity [$R_{\text{ch}}W$] (having units of Ωcm) as given by [$R_{\text{ch}}W$] = $L_{\text{ch}}/(\mu C_{\text{ox}}(V_{\text{GS}}–V_t))$ depends on gate bias V_{GS}, on gate oxide thickness (that sets C_{ox}), and on double-diffusion (the process which sets the VDMOS effective channel length L_{ch} and threshold voltage V_t). Moreover, because VDMOS channel length is determined by

diffusion, not by photolithography, its accurate extraction is not useful and somewhat academic. Instead, channel resistivity $[R_{ch}W]$, easily extracted electrically, is preferable for describing VDMOS conduction rather than using estimates of W/L_{ch} (a parameter frequently reported for uniformly doped channel MOSFETs used in logic ICs). Combining the foregoing, (1) describes the die ON-resistance of vertical conduction double-diffused devices

$$\begin{aligned} R_{DS(on)} &= R_{metal} + R_{contact} + R_{source} + R_{ch} + R_{acc} + R_{jfet} \\ &\quad + R_{epi} + R_{sub} \\ &\approx R_{ch} + R_{drift} = ([A/W][R_{ch}W] \\ &\qquad + R_{drift}A)/n_{cells}A_{cell}. \end{aligned} \tag{1}$$

Aside from channel resistance, the epitaxial drift resistance is a major component in VDMOS devices. Specifically, in well-designed vertical field effect devices, the epitaxial layer doping concentration and thickness (not the channel or edge termination) sets the device's breakdown voltage. For high voltage n-channel devices, Hu [41], [42] observed that the epitaxial resistance $R_{drift}A$ depends on the specified junction avalanche breakdown voltage $V_{(br)}$ raised to the power of n, or algebraically as $R_{epi} \propto V_{(br)}^{n}$ where n is approximately 2.5–2.6 a relation commonly referred to as the "silicon limit" for unipolar conduction. When combined with (1), the relation predicts for high blocking voltages the epitaxial drift resistance dominates overall device resistance and VDMOS cell density is a secondary design consideration. Conversely, it follows that for low voltage devices below 150 V (and especially at and below 60 V), the channel resistance R_{ch} becomes more significant. Low voltage device optimization therefore primarily involves minimizing channel length and gate oxide thickness to reduce channel resistivity $[R_{ch}W]$, and optimizing geometric cell design and photolithography to maximize the transistor's channel density [W/A].

Unfortunately, for low voltage device operation, both the VMOS and similarly planar vertical DMOS suffer fundamental limitations in channel density. In the case of the planar vertical DMOS, the presence of parasitic JFET resistance R_{jfet} located between facing body diffusions fundamentally limits beneficial dimensional scaling of the cell [43]. Specifically, as the polysilicon gate dimension is reduced below a certain width when shrinking the device cell pitch, an unavoidable increase in the JFET pinch resistance occurs (more than offsetting the decrease in channel resistance) and overall device resistance increases. As such, planar VDMOS is better suited for high voltage devices where channel density is less important.

In the case of VMOS, channel density is determined by the minimum width of the etched v-groove. Using KOH, etching a <100> oriented silicon wafer results in a v-groove terminating along the <111> crystalline plane and forming a 54.7° angle with the silicon surface [44]. To avoid high electric fields at the tip of a fully etched v-groove, the v-groove etch is terminated prematurely to produce a flat-bottomed or "truncated" groove of a predefined width. Combining the limitations imposed by the obtuse angle of the v-groove and the minimum width flat portion of the truncated groove, dimensional shrinking of the v-groove is fundamentally limited.

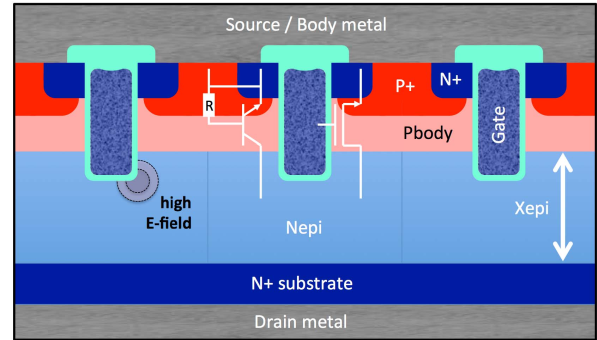

Fig. 2. Cross section of a trench gate vertical DMOSFET or trench VDMOS. Schematic elements illustrate the VDMOS active cell and parasitic n-p-n BJT.

Moreover, since the groove is too wide to refill and planarize, the deposited gate electrode must conformally coat the nonplanar topography. The resulting step height creates source metal step coverage problems rendering the device difficult to manufacture in volume. Other challenges including v-groove etch control, and issues in cleaning and growing stable gate oxides atop chemically etched surfaces. Despite its exuberant reception at the time of introduction, production of VMOS ended in the mid-1980s, one decade after its discovery.

In 1985 Ueda *et al.* [45] replaced the chemical v-groove etch with an anisotropic reactive ion etch to produce a steeper rectangular-shaped groove, demonstrating a functioning vertical MOSFET formed on a vertically etched sidewall. Like the VMOS, the device utilized a conformal polysilicon gate that in combination with a steep and wide rectangular groove profile resulted in an even larger step height than VMOS. Given its topological issues and a 14-μm unit-cell pitch, the 50 V device's 530-mΩmm^2 specific ON-resistance underperformed planar VDMOS of the time and was never commercialized.

III. Trench Vertical DMOSFET

In order to reproducibly fabricate a low-resistance trench gated DMOSFET with high reliability, several important innovations were required, including planarizing trench refill, trench field shielding, sacrificial gate oxidation, avalanche protection, and substrate engineering as described in the following.

A. Trench Refill and Etchback

To realize a manufacturable trench power MOSFET and to overcome the aforementioned step coverage issues of its predecessors, one indispensible trench process innovation proposed by Blanchard [46], [47] was the introduction of a fully planarized polysilicon gate. As shown in Fig. 2 after double diffusion forms the VDMOS's source and body regions, an etched trench of narrow width (e.g., 0.8 to 1.5 μm across) is oxidized to form a gate oxide lining the trench and subsequently filled with phosphorus *in situ* doped polysilicon. By design, the polysilicon CVD deposition completely fills the trench, overflowing the etched trench onto the silicon surface. Except for a (small) masked area needed for gate contact, the polysilicon is then "etched back" so that the top surface of the polysilicon gate is recessed, i.e., etched below, the silicon surface (but importantly still overlapping the n$^+$ source).

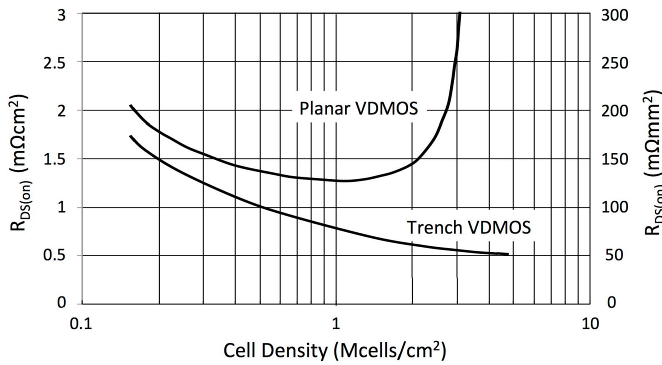

Fig. 3. Impact of cell density on specific on-resistance $R_{DS}A$. Planar VDMOS exhibits a minimum while trench VDMOS benefit from scaling.

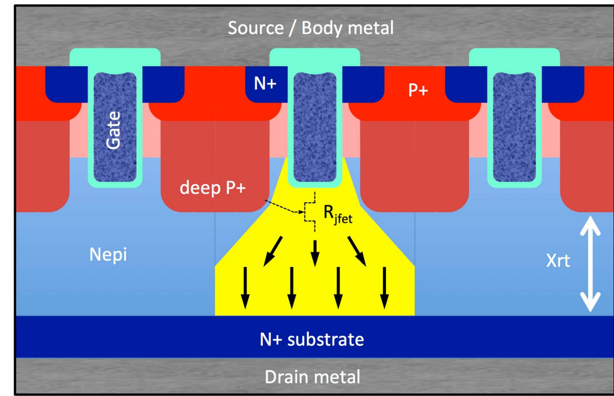

Fig. 4. Unit-cell clamped trench VDMOS. The deep p^+ shields the trench gate from high electric fields while clamping the avalanche voltage but constricts conduction current, increasing on-resistance at higher cell densities.

Subsequent thermal oxidation then caps and seals the recessed polysilicon with a protective layer of oxide. Alternatively, a thin conformal oxide may also be deposited after the polysilicon oxidation step. A contact mask then selectively exposes the transistor's surface gate and its numerous cellular source/body regions to an oxide etch (while protecting the oxide above the trench). The oxide etch may be performed by a wet chemical etch containing HF acid, by a plasma dry etch, or some combination thereof. After contact-etch, metal deposition and photolithographic patterning are performed interconnecting a sea of separate and distinct trench VDMOS cells into a single three-terminal trench power MOSFET. Except for the polysilicon gate contact, the resulting die's surface is nearly planar, so that problematic step coverage issues are completely eliminated. The resulting cell pitch was half that of any prior art vertical device, improving channel-resistance, epitaxial current uniformity, and total ON-resistance.

As represented in the graph of Fig. 3, increasing cell density of a trench vertical DMOSFET (also referred to as UMOS) decreases the device's ON-resistance hyperbolically. In contrast, devices with a fixed minimum gate dimension (such as planar vertical DMOS or VMOS) exhibit a U-shaped dependence, declining in ON-resistance with increasing density before reaching a minimum, then rising rapidly at higher densities as a result of a decrease in channel packing density [W/A] and poor current uniformity in the epitaxial layer.

In late 1987, a 30 V trench VDMOSFET prototype utilizing the trench refill and etchback method was reported [48]. Although the 2.4-kΩ test-device was limited to very low currents, its 100-mΩmm^2 specific ON-resistance confirmed the ON-state benefits of a high cell density enabled by poly etchback and a planarized trench structure. A few months later, a full-sized 60 V trench power MOSFET at 4 mΩ was fabricated and characterized [49]. While in hindsight the concept of the polysilicon trench fill and etchback process may appear obvious, at that time conformal coating (not overfill and etchback) was the predominant form of planarization.

B. Trench Gate Field Shielding (Unit Cell Clamp)

Given stochastic process variability in the depth of the diffused p-type body and of the etched trench, the location of avalanche can randomly shift from the body-to-epitaxial junction to a more-damaging localized avalanche near the trench gate. Avalanche juxtaposing the trench gate can catastrophically rupture the gate oxide by high electric fields or degrade the gate oxide through repeated hot carrier injection. Insightfully, Blanchard [50] proposed a thick bottom oxide (TBOX), i.e., using multiple gate oxide thicknesses to lower the field at the trench bottom, but limitations in process capability delayed the manufacture of TBOX trench devices for years.

As an alternative, Bulucea and Rossen [51], [52] proposed a method to protect the trench gate by introducing a deep p^+ diffusion within every source/body cell. The uniformly distributed *unit cell clamp* shown in Fig. 4 provides field shielding of every trench gate while clamping the maximum voltage by reach-through avalanche (set one-dimensionally by the deep $p^+/n_{epi}/n^+$ substrate sandwich). In trench VDMOS, the intent and primary benefit of deep p^+ to inhibit hot carrier generation in the vicinity of the gate dielectric is functionally distinct from the highly litigated matter of bipolar snapback suppression in high-voltage planar VDMOS [53], [54], especially below 200 V. Unfortunately, the use of deep p^+ in every cell adversely impacts conduction current spreading in the device's epitaxial drift drain region, its effect varying in degree with cell pitch.

C. Trench Etch and Manufacturability

The next critical step in trench VDMOS evolution focused on the monumental goal of making the device reliable and manufacturable in high volume, starting with the task of trench gate engineering—how to fabricate a silicon trench with rounded corners and grow a stable gate oxide free of surface states, not subject to hot carrier charging during operation.

To minimize surface state charge and achieve high channel mobility, the trench gates fabricated on <100> Czochralski grown silicon are etched parallel and perpendicular to the <110> crystal-plane [55] to avoid excessive surface roughness, high interfacial charge, and low mobility of the <111> plane [56]–[58]. Since automatic photomask aligners register wafers during the load operation relative to the wafer flat, and because standard silicon wafers used a flat ground on the <111> plane, to avoid rotating the wafers in the aligner (as

Ueda did) specially cut <100> wafers had to be developed by the monocrystalline wafer suppliers with a <110> oriented flat just to support the trench MOSFET business. Furthermore, to avoid etching across multiple crystal planes, rectangular and square shaped cell arrays, rather than hexagonal cells, were selected.

The next critical element in a production worthy trench MOSFET was silicon etch control. The trench etch is often performed using a temporary "hard mask" comprising a glass or nitride–oxide sandwich that is patterned and etched prior to commencing silicon etching. In this manner, photoresist is not present during the silicon etching process and organic residues cannot contaminate the trench and degrade gate oxide quality. To avoid sharp corners at the trench bottom, the trench etch commences using directional fields in the etch chamber to achieve (by momentum transfer) a high degree of anisotropy needed to form the vertical edge of the trench sidewall. At the end of the etch process, the accelerating field and the etch anisotropy are reduced resulting in a greater degree of chemical etching needed to round the bottom trench corners.

Another key element to trench formation is cleaning up etch damage from the etching process. Empirical data reveals that silicon etches alone are inadequate to remove dangling bonds and control surface state charge. Instead, a sacrificial oxide is required where the oxide in grown at a high temperature [57], typically over 1100 ° C followed by a complete removal of the "sac ox" before the gate oxide is grown. Although the temporary sac ox thickness is not significant, because of high temperature oxidation, the impact of the process's diffusivity-time constant (i.e., DT) on the p-type body profile and on updiffusion of the heavily doped substrate must be considered.

A final process optimization involves oxidation of the top of the recessed polysilicon and resultant shape and film stress at the surface trench corners. Depending on the formation and removal of the trench etch hard mask, care must be taken to avoid defects at the trench top or a high incidence of gate-to-source shorts (I_{GSS} failures) will be manifested. Top oxidation induced film stresses were also found to induce I_{DSS} channel leakage during high-temperature reverse bias (HTRB) burn-in observed randomly in a small but unacceptable fraction of the sample population. Studies revealed the leakage originated along the intersection of trenches (where crystalline planes meet), arising from film stress and defects, dopant depletion, and corner-specific short channel effects. By blocking the source implant from the trench corners to minimize corner conduction, burn-in leakage failures were eliminated [59]. Later, other process and design approaches addressing the acute corner issue were devised, including adjusting the layout [60] to avoid or at least minimize the density of active corners.

With the foregoing issues addressed, pilot line production of the device commenced [3]. Considering uncertainties in manufacturing yield and in long-term reliability of the new technology, the first commercial trench VDMOS [61] was deployed as components within power modules (where the operating conditions could be better controlled). At that time, the devices were not offered for sale as discrete components.

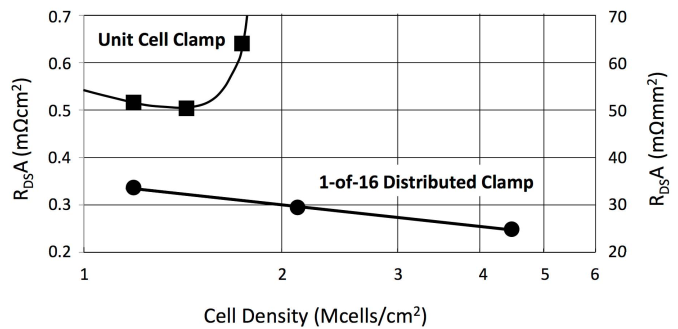

Fig. 5. Impact of trench VDMOS cell density on specific on-resistance (30 V, N-ch, circa 1997). The 1-of-*n* distributed voltage clamp avoids the increased in resistance of the unit cell clamped device while insuring rugged UIS capability.

Only after gaining several years of reliability statistics in real-world applications was the trench power MOSFET finally commercially introduced as discrete devices at the international electronics trade-show *Electronica* in Munich [62], including n-channel and p-channel trench power MOSFETs at 60 and 30 V manufactured with the cell densities of 1.3 and 1.9 Mcells/cm^2, respectively. With the advent of the Li–ion battery, the need for low threshold voltage power saving load switches quickly emerged. In order to serve the burgeoning Li-ion market, the first p-channel 30 V trench VDMOS with a specific ON-resistance of 90 mΩmm^2 at V_{GS} = 2.7 V (the Li–ion minimum voltage) was introduced [63].

D. Overcoming Unit-Cell Clamp Limitations (1-of-n Clamp)

One fundamental issue of integrating a deep p$^+$ clamp into every cell, i.e., unit cell clamp, is an inability to scale the cell to smaller dimensions without adversely impacting ON-resistance and device threshold (see Fig. 5). As shown, the observed increase in resistance at higher cell densities is primarily due to the deep p$^+$ constraining current spreading in the epitaxial drain. To overcome the JFET density limitation of the unit cell clamp, Williams [64] proposed distributing a deep p$^+$ voltage clamp in only one of every "n" cells, where avalanche is supporting by defined diodes not adjacent to active devices.

First confirmed by 2-D device simulation, analysis revealed that for $n = 16$, i.e., for a diode clamp in 1-of-16 cells, similar avalanche ruggedness to the unit cell clamp is achievable while enabling unlimited scaling of the active device cell dimensions. A cross section and top view of the 1-of-*n* distributed voltage clamped trench VDMOSFET is shown in Fig. 6. Numerous variations of the distributed clamp were devised and compared [65]–[67] including p$^+$ clamps under the gate bus.

Demonstrated in 30 V n-channel trench VDMOS, the distributed voltage clamp nearly tripled device cell densities to 5 Mcells/cm^2. Correspondingly, device ON-resistances were reduced by 50%—half that of predecessor trench VDMOS [68]. The benefits resulted principally from improved current spreading but also by an increase in [W/A] channel density. The 30 V SOP-8 package devices with a record setting specific on-resistance of 25 mΩmm^2 were used to establish

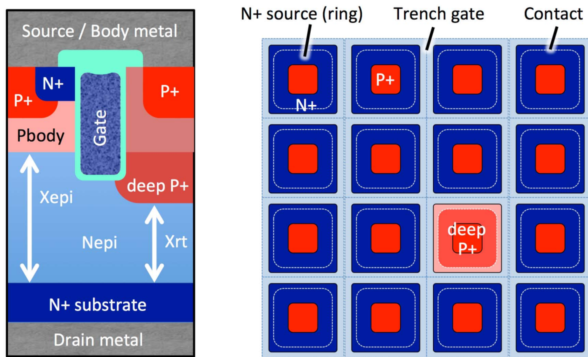

Fig. 6. Cross section and top view of a 1-of-n distributed clamp trench gated VDMOS with $n = 16$. In reach-through induced avalanche (having a net epitaxial thickness Xrt $<$ Xepi), the deep p^+ cell carries the most current.

the unclamped inductive switching (UIS) avalanche capability of the high-density device. Measured pulsed avalanche current *seven times* the device rating with no damage was confirmed.

For very low resistances, the same cell was employed to fabricate the first million-cell trench power MOSFET. With 2-mΩ die-resistance in DPAK sized die, such extremely low $R_{DS(on)}$ trench power MOSFETs were immediately recognized as problematic, because the package's bond-wire and lead resistance was comparable with the die's resistance. To capitalize on high cell-density silicon performance, large die designed for D^2PAK and DPAK packages required clip lead source contacts. Smaller die, such as those packaged in the SOP-8 and other SMPs, remained for the time being amenable to conventional bond wire assembly. With the expanded capabilities offered by high-density trench VDMOS, products in the range of SOT-23 to SOP-8 sized packages rapidly replaced DPAK sized planar VDMOS in space sensitive applications including hard disk drives, airbags, automatic braking system (ABS) antiskid brakes, and lithium–ion battery protection.

Four years later, trench VDMOS fabrication moved into former DRAM fabs with 0.35-μm linewidth [8]. Using million-electron-voltage high-energy ion (HEI) implantation [69] to replace diffusions, tighter threshold control and shorter channel lengths became manufacturable. Combined with self-aligned contacts, the trench power MOSFET achieved unprecedented densities of 44.5 Mcell/cm^2 and record low die resistances [8]. With such high cell densities, an SOP-8 sized 30 V trench VDMOS exhibits a die resistance of 2.7 mΩ, a performance only achievable previously by larger die sized to fill DPAK packages. Clip lead SOP-8 packages were soon introduced to capitalize on this newest generation of trench VDMOS.

As an alternative means to shrink the silicon mesa between trench gates, source/body trench contact processes were also successfully demonstrated [70]. Without self-alignment, however, silicon mesa widths must accommodate contact misalignment to the trench gate, and alone are unable to match the density or specific ON-resistance of self-aligned methods. Fabrication of superself-aligned devices—where the contact, trench gate, and p^+ body contact are all defined by a single mask [71], [72] were demonstrated up to densities of 100 Mcells/cm^2. For devices with such high channel densities, three challenges emerged. First, the channel resistance is so low that the substrate resistance becomes a significant contributor to total die ON-resistance. Second, gate and overlap capacitances C_{GS} and C_{GD} increase linearly with cell density while ON-resistances only decline hyperbolically, meaning the gate-charge ON-resistance $Q_G R_{DS(on)}$ FOM is degraded. Third, the ultralow specific ON-resistance $[R_{DS}A]$ limits the maximum usable die size, beyond which package resistance, not the die, becomes the dominant consideration.

So with the advent of deep submicron processing, the trench power MOSFET entered a new era where parasitic resistances, capacitance, and packaging, not cell density, represented the key design and process considerations in improving device performance (see Section IV).

E. Substrate Engineering

Because trench VDMOS conduction occurs *vertically* through its substrate, the starting wafer does more than provide mechanical support to active devices—it plays a crucial role in device fabrication and electrical performance. To minimize ON-state resistance, low-voltage trench VDMOS fabrication requires both post-fabrication wafer thinning and the need for degenerately doped substrates—wafers heavily doped with extremely low resistivity using boron or (rarely) gallium for p-channel devices, and either arsenic, phosphorus, or antimony for n-channel devices. Although arsenic doped wafers are available in the range $\rho_{sub} = 1.8$–3 mΩcm, phosphorus achieves a lower resistivity, e.g., 0.8–1.5 mΩcm, primarily a consequence of its reduced lattice mismatch. Phosphorus's advantage in conductance is, however, partly offset by its graded (less-abrupt) dopant profile. This unwanted dopant gradient occurring at the epitaxy-substrate interface is a consequence of updiffusion and vapor-phase "autodoping" during thermal processes, including epi-growth, VDMOS body diffusion, and from high-temperature sacrificial oxidation. The dopant gradient contributes to an increased ON-state resistance (without a commensurate improvement in breakdown). Various methods such as the "low-high" process temperature profile during epitaxy have been shown to steepen the transition step, especially for phosphorus [73]. Somewhat unexpectedly, p-type substrates are only slightly higher in resistivity than n-type, mainly because at extreme dopant concentrations, high carrier scattering causes hole and electron mobility values to converge [74].

Another unique feature of power device manufacturing is the use of epitaxial wafers supplied by the substrate vendor, i.e., substrate wafers already predeposited with specific epitaxial layers. Unlike high-voltage superjunction devices and epitaxial-based integrated circuits where epitaxial growth occurs *after* forming patterned buried layers, low-voltage trench VDMOS uses epitaxial layers grown atop unprocessed substrates. Substrate vendors routinely supply starting wafers with custom epitaxial layers grown to precise thickness and doping specifications unique to each client, device type, and voltage rating. In some cases, the epitaxial layer doping concentration may be graded, stepped, or contain multizone doping profiles. Because of the degenerately doped substrates,

care must also be taken in substrate polishing to prevent stacking faults and Frenkel defects in epitaxial layers. Epitaxial growth frequently commences with an *in situ* HCl etch or H_2 bake to remove surface defects prior to epitaxial deposition.

As described previously, trench manufacturing also requires special Czochralski wafers having a wafer flat ground parallel to the <110> plane to insure alignment between the trench mask and specific crystallographic planes. During trench etch the depth of the trench should not exceed the epilayer thickness or additional quality issues may occur. In particular, oxidation of trenches penetrating into degenerately doped substrates exhibit degraded dielectric strength, increased surface state charge, and excessive gate leakage.

Following fabrication, wafers are mechanically thinned and then coated with a sandwich layer back-metal such as titanium, nickel, and silver (TiNiAg) to provide ohmic contact to the wafer, to prevent diffusion of metals to the wafer contact interface, and to provide a solderable low-resistance layer to attach to silver-plated copper leadframes. Using a large grit for conventional mechanical grinding, rapid processing of wafers with good ohmic contact and adhesion to back metal can be achieved, reaching final wafer thicknesses of $x_{\text{sub}} = 150–200\ \mu$m. From the relation $R_{\text{sub}}A = \rho x_{\text{sub}}$, after conventional thinning the resulting substrate contributes approximately 5 mΩmm^2 to a device's specific ON-resistance.

For trench VDMOS below 20 V (or for cell densities over 50 Mcells/cm^2), conventional substrate grinding is inadequate with the mechanically thinned substrate still contributing significantly to the device's total ON-resistance. Extreme wafer thinning using conventional large-grit grinding is, however, problematic as it results in significant stress-induced wafer bowing and breakage. Fine-grit grinding (commonly used for smart card chip manufacturing) is not applicable, because back metal will not adhere to the fine texture surface, suffering metal peeling, and poor ohmic contact. Instead, a two-step process must be adopted, using a thick grit to grind the wafer to around 100 μm then using a chemical etch process to complete the thinning to 50 μm, to remove the stress and wafer bow, and finally to roughen the surface for good metal adhesion.

To avoid excessive wafer breakage during handling of ultra-thin wafers, the "Taiko" process [75] is frequently employed especially for sub-40 V trench VDMOS. Albeit more costly to manufacture, in the Taiko process, the center portion of the wafer is ground or etched to the target thickness, while a small outer ring of thicker silicon is retained to provide mechanical strength for handling and reduced breakage. Competing methods involve temporarily wafer bonding [76]–[78], attaching the product wafer frontside to a mechanical "handle" wafer with tape, glue, or wax to facilitate grinding and handling, then removing the handle wafer after thinning.

IV. Gate-Drain Engineering

Aside from increasing cell density, another important design consideration in trench VDMOS is minimizing unfavorable electrical interactions between a device's epitaxial drain and its trench gate, including effects impacting breakdown and specific ON-resistance, leakage, feedback capacitance, gate charge, switching speed, gate drive loss, and reliability.

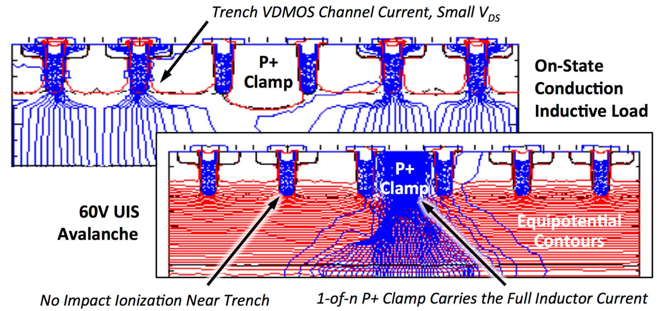

Fig. 7. Avalanche current in a uniform TBOX trench VDMOS. TBOX shifts the avalanche location away from the trench gate to a local deep p^+ clamp.

A. Electric-Field Shaping

One method to improve trench VDMOS performance and reliability is to employ thick oxides at the bottom and optionally on the trench sidewalls (but not overlapping the channel region) to facilitate field shaping, i.e., controlling the location of peak electric fields and preventing avalanche or significant hot carrier generation in the vicinity of the trench gate oxide [79]–[83]. As shown in the example of Fig. 7 properly optimized, a uniform TBOX layer has the ability to shift avalanche current away from the trench gate, forcing avalanche near the unit center of active cells or at higher currents, diverting breakdown to the regions of deep p^+ avalanche clamps [84], [85]. Other field shaping options include using graded thick sidewall oxides [86].

Aside from using multiple oxide thickness, field shaping also benefits from employing graded on nonuniform epitaxial dopant concentration profiles, especially to lower the net donor concentration in the drain adjacent to the trench gate. Dopant gradients can be achieved by numerous means including: 1) depositing epitaxial layers of varying doping concentration, i.e., graded epi; 2) using HEI implantation to locally increase drain concentrations spaced vertically below the trench; 3) ion implanting the bottom of the trench to counterdope body diffusions [87], [88] locally increasing drain concentration slightly below (but not touching) the TBOX trench bottom; or 4) using a 3-D design, laterally alternating conducting portions of a trench gate with segments where the trench bottom is surrounded by a p-type counter doped region [89]. Other methods to control the electric fields near the trench gate include field plate and split gate structures (see Section IV-B), using charge balancing (see Section IV-C), and combinations thereof.

Aside from the active device cells, electric field shaping is also required along the die periphery in the high-voltage edge termination. Although most trench VDMOS utilize thick field oxide with field plates or at higher voltages floating field rings, novel terminations utilizing the trench have also been proposed to reduce termination dimensions [90]. Care should be observed to consider the photolithographic and etching challenges of concurrently defining and dry-etching trenches of varying widths.

B. Reducing Feedback Capacitance and Gate Charge

Historically, each generation of trench power MOSFET has achieved a lower specific ON-resistance by device scaling, i.e., shrinking its cell dimensions and increasing its cell density, thereby reducing both channel resistivity and improving epitaxial drain current uniformity. In higher switching speed applications, a fundamental challenge to increasing cell density arises from the adverse impact of capacitances intrinsic to the trench VDMOS, primarily the effect of gate-to-drain feedback capacitance C_{GD} but also including the gate-to-source capacitance C_{GS}. While in early generation trench VDMOS, gate and feedback capacitance were dominant, as these parameters have improved the role of drain-to-source junction capacitance C_{DS} has also become increasingly important, especially in methods that reduce C_{GD} by sacrificing low C_{DS}.

In low-voltage power circuitry, the gate-to-drain capacitance C_{GD} is especially important, because it represents a nonlinear feedback connection between the transistor's output and input terminals—an unwanted parasitic adversely impacting both a device's power efficiency and switching performance. In the hybrid-π representation of an MOSFET, this feedback element is referred to by the term C_{rss}. Miller [91] and Gray *et al.* [92] observed that in (vacuum tube) amplifiers with voltage gain, the magnitude of this feedback capacitance appears larger on the input terminal of the device than its physical value. This circuit related phenomena now commonly referred to as the Miller effect applies to any device exhibiting voltage gain including BJTs and power MOSFETs. Specifically, on the gate-to-source input terminals of the power MOSFET, the feedback capacitance C_{rss} has an apparent magnitude $A_{\mathrm{V}}C_{\mathrm{rss}}$, where A_V is the voltage gain of the circuit under a specific bias condition.

In switching operation, the MOSFET traverses between ON and OFF states by operating momentarily in its saturation region where voltage gain occurs and the Miller effect is manifested. Because both the feedback capacitance C_{rss} and the voltage gain A_V vary with voltage and because the bias conditions are constantly changing during a switching transient, it is impractical to use the small signal capacitance values to model the device's switching behavior or accurately predict switching power losses. In fact, many device models used in the circuit simulation software SPICE rely on voltage variable capacitances that do not conserve charge [93]–[96], meaning the simulation cannot be used to accurately predict power loss. Instead, power MOSFET switching losses are best analyzed using charge rather than capacitance. With charge based equations, gate drive losses of a power MOSFET switching at a frequency f can be expressed in a more convenient form as $(Q_G V_G)f$ shown in (2) where

$$\mathrm{P_{gate}} = ½ f(C_{\mathrm{iss}}V_{\mathrm{GS}}^2 + \smallint(A_{\mathrm{V}}C_{\mathrm{rss}})V_{\mathrm{GD}}dV) = (Q_{\mathrm{G}}V_{\mathrm{G}})f. \quad (2)$$

Since charge Q_G is conserved, power loss calculations using charge depend only on the starting and ending voltage states and not on the myriad of bias conditions in between. Unlike tedious and less precise capacitance characterization, the total gate charge $Q_G = Q_{\mathrm{GS}} + Q_{\mathrm{GD}}$ can easily be measured by injecting a constant current I_G into the MOSFET's gate and plotting the gate voltage versus time, while the MOSFETs drain is biased by an electrical load. Since the gate current is constant during testing, then $Q_G = I_G \bullet t$ and the time axis can be replaced by charge, resulting in a graph precisely describing how much charge is required to switch a power MOSFET with a specific gate bias. In a gate charge measurement, the gate charge curve of a power MOSFET exhibits a "Miller plateau" region (see graph of Fig. 9) where gate voltage temporarily remains unchanged (even though the gate is being driven by a constant current). The plateau region represents the charge Q_{GD} supplied to the gate-to-drain capacitor C_{GD} during a turn-ON drain transient dV_D/dt. In essence, rather than charging C_{GS}, gate current is temporarily diverted into charging C_{GD}, at least so long that the condition $I_G = C_{\mathrm{DG}}\ dV_D/dt$ persists.

Once the MOSFET enters its linear operating region and is no longer in saturation (i.e., $V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_{t0}$), the drain voltage approaches $I_D R_{\mathrm{DS(on)}}$ as the gate voltage resumes its climb to its final V_{GS} value. The resulting width of the plateau resulting from the drain voltage transition is therefore proportional to C_{GD} and a direct measure of Q_{GD}. In the conventional trench gate charge curve example shown, the gate charge at $V_{\mathrm{GS}} = 10$ V is $Q_G = 93$ nC of which approximately $Q_{\mathrm{GD}} = 27$ nC or 30% was consumed charging C_{GD}. The charge required to drive a device from its OFF state with $V_{\mathrm{GS}} = 0$ to a fully on state, e.g., with gate bias $V_{\mathrm{GS}} = 10$ V is independent of the gate driver itself. In an actual application circuit using constant voltage gate drive, the plateau region is virtually unnoticeable in the gate voltage waveform. Nonetheless, the gate charge and associated drive loss required to turn the device on is identical to the Q_G measured by the gate charge curve (even though the voltage plateau is not observable).

The values of Q_{GD} and of Q_G (at a particular gate voltage) for trench VDMOS depend on the device and cell design, as well as the fabrication process employed. Analogous to specific on-resistance, *specific gate charge* $[Q_G/A]$is the gate charge divided by its active area A. The total gate charge Q_G of a device comprising n_{cells} each of area A_{cell} with specific gate charge $[Q_G/A]$ is given by

$$Q_{\mathrm{G}} = [(Q_{\mathrm{GS}} + Q_{\mathrm{GD}})/A] \bullet n_{\mathrm{cells}} A_{\mathrm{cell}} = [Q_{\mathrm{G}}/A] \bullet n_{\mathrm{cells}} A_{\mathrm{cell.}} \quad (3)$$

In high-frequency switching applications, especially for switchers operating over 1 MHz, trench VDMOS having large gate charge requirements suffer numerous issues including the following:

1) large power loss from gate drive (drive losses);
2) reduced power efficiency;
3) requires high gate drive currents;
4) requires large gate driver buffers;
5) poor transient response;
6) limitation of minimum or maximum duty cycle.

Another potential adverse impact of high gate-to-drain capacitance is the problem of shoot-through or *dV/dt* effects [97], [98]. In trench VDMOS with large C_{GD} capacitance, the gate driver is unable to hold the MOSFETs internal gate potential at ground during turn-OFF. As the drain voltage

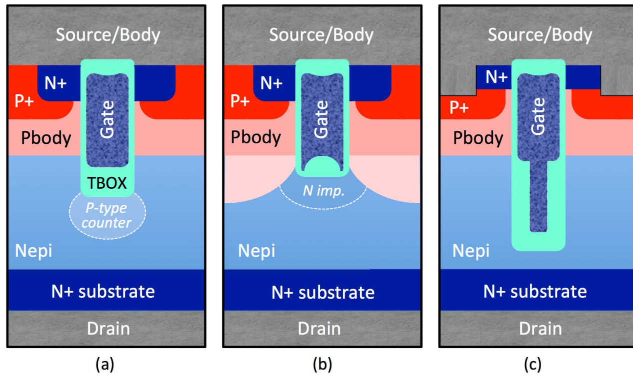

Fig. 8. Cross sections of various TBOX trench VDMOS. (a) Uniform TBOX with optional p-type counterdope implant. (b) W-gated with optional n-type implant. (c) Terraced oxide field plate.

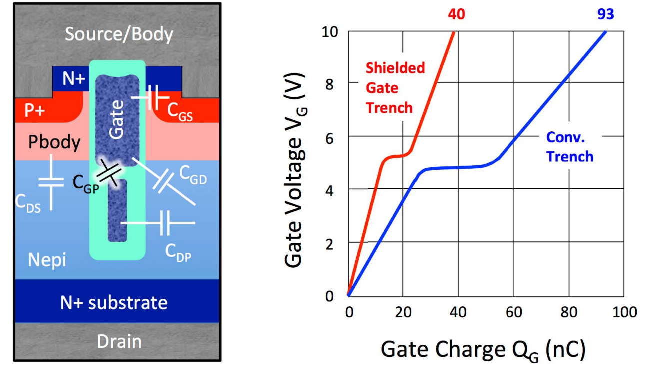

Fig. 9. Cross section and gate charge benefit of split-gate trench VDMOS.

rises during turn-OFF, the C_{GD} capacitor forms a transient voltage divider with the transistor's gate resistance. The net effect is the MOSFET's internal gate voltage momentarily rises, temporarily turning the device on again, and increasing switching losses even though the gate terminal is grounded.

To combat the forgoing issues, significant efforts have been made in minimizing trench VDMOS gate charge and reducing gate-to-drain capacitance but without adversely impacting device ON-resistance, thereby minimizing the adverse effects of increasing the cell density on switching performance. Using a thicker oxide at the trench bottom such as those shown in the examples of Fig. 8 offers an attractive solution.

In the case of Fig. 8(a), the TBOX is formed by directional deposition of oxide using low pressure CVD [7]. The presence of the TBOX reduces the value of C_{GD} by eliminating the vertical component of capacitance. The challenge of improving trench VDMOS switching performance using uniform TBOX is one of process control.

Specifically because of stochastic variability in trench depth, penetration of the gate electrode into the epitaxial drain (and hence the degree of overlap) is not consistent, changing from one manufacturing lot to the next. As such, the magnitude of gate-to-drain overlap capacitance C_{GD} is difficult to insure. Using a self-aligned process technique, Darwish *et al.* [99] demonstrated one means to mitigate trench depth process variability and its impact on feedback capacitance. In this method, a local oxidation is performed on the trench bottom to shape the polysilicon gate and form thick oxide to minimize C_{GD}. The resulting bottom oxide exhibits a gradual transition from its full thickness in the center to its thin gate oxide along the trench walls and at the trench corners, resulting in the device's characteristic "W" shaped gate topography shown in Fig. 8(b). Prior to oxidation, the trench bottom is HEI implanted with phosphorus to self-align to the p_{body} to n_{epi} junction to the trench.

To minimize the sidewall component of C_{GD}, the device employs a slightly deeper p_{body} region, shielding the embedded trench gate from the epitaxial drain. This method further benefits device reliability by moving the location of avalanche laterally apart from the thin gate oxide. Care must be taken, however, not to diffuse this body region too deep, or (in a manner similar to Bulucea's unit cell clamp) current spreading in the epitaxial drain will be limited and adversely impact epitaxial drift resistance, increasing the device's overall ON-resistance from a parasitic JFET similar to planar VDMOS.

A third variant of trench VDMOS with TBOX is shown in Fig. 8(c). In this implementation, the lower portions of the trench (including its sidewalls and trench bottom) utilize a thick oxide, while only the upper portion of the trench employs a thin gate oxide. The resulting terraced or stepped gate electrode forms a gate with an extended field plate, reducing the electric field near the trench and lowering feedback capacitance [50], [100], [101]. Although the field plate facilitates field shielding of the thin gate portion of the device, because it is electrically connected to the gate, it still represents an added component of feedback capacitance.

A widely adopted improvement to the field plate trench VDMOS first proposed by Baliga [102], [103] is the split-gate or shielded-gate trench VDMOS and its variants [104]–[108]. The split gate structure shown in Fig. 9 comprises two *in sit*u doped polysilicon regions—an upper "gate" portion comprising the transistor's gate electrode, and a lower "buried field plate."

While the split-gate trench VDMOS uses thick and thin oxides structurally similar to the field plate trench VDMOS, the buried field plate is not connected to the transistor's gate, but instead is grounded (the ground connection is not shown in the illustrated cross section). Since the buried field plate is grounded and not connected to the gate, it does not contribute to an increase in C_{DG} feedback capacitance. In its OFF state, the depletion spreading induced by the presence of the grounded buried field plate electrostatically shields the upper gate electrode from the full drain potential. Electrically, this 2-D depletion region effect behaves like a phantom capacitance in series with C_{GD}. Since connecting two capacitors in series lowers total capacitance, the split gate structure dramatically reduces the gate-to-drain capacitance C_{GD} and correspondingly significantly reduces Q_{GD} [109] and Q_G. As shown in the accompanying graph, using the split gate structure, trench VDMOS gate charge at $V_{GS} = 10$ V is reduced by 57% from 93 to 40 nC and Q_{GD} is significantly reduced by 75% from 27 to 7 nC. The gate charge values cited are included for illustrative purposes to exemplify the benefit of the split gate structure, not to compare each device to prior

generations. The performance benefit of the split gate varies by design and device rating.

Although the split-gate trench structure of Fig. 9 significantly reduces gate-drain charge Q_{GD}, it introduces two new parasitic capacitances associated with the buried field plate, specifically a drain-to-plate capacitor C_{DP} and a gate-to-plate capacitor C_{GP}. In operation, gate-to-plate capacitance C_{GP} is electrically in parallel with gate capacitance C_{GS}, increasing input capacitance $C_{iss} = C_{GS} + C_{GP}$ and contributing to a higher gate charge Q_{GS} and Q_G. This increase partly offsets the split-gate device benefits of lowering Q_{GD} and explains why the aforementioned 57% improvement in Q_G is not as significant as the observed 75% reduction in Q_{GD}.

As mentioned previously, the buried field plate also introduces a drain-to-plate capacitor C_{DP} into the split gate trench VDMOS. Since the plate is grounded, C_{DP} appears electrically in parallel with the p_{body} to n_{epi} junction capacitance C_{DS}, thereby increasing the output capacitance $C_{oss} = C_{DP} + C_{DS} + C_{GD}$. This higher output capacitance adversely impacts efficiency in high-frequency dc/dc converters [110], especially at higher voltages [111], e.g., over 100 V and although less significant at lower voltages, it is becomingly increasingly important with the reduction of Q_G in each new device generation.

Like TBOX, capacitance reduction methods such as the field plate and split gate also reduce electric fields adjacent to the trench gate allowing a higher doping concentration to be employed for the same breakdown voltage device rating, i.e., the specific ON-resistance is reduced for a given breakdown. When combined with charge balancing (discussed in section IV-C), field-plate and split-gate trench VDMOS are particularly effective in reducing electric fields, improving breakdown, and in reducing C_{GD} gate-to-drain feedback capacitance. Combining these field plate methods with nonuniform drain doping offers the opportunity to significantly impact epitaxial drift resistance component in ON-resistance, especially in trench VDMOS over 40 V where its contribution is more important.

C. Charge Balancing (Superjunction)

Another method to optimize breakdown, improve specific ON-resistance, and minimize feedback capacitance in vertical DMOS utilizes the principle of "charge balancing" or "charge compensation". First reported on a *lateral* p-n junction (JFET) as a means to reduce surface electric fields [112], the RESURF effect exhibits the beneficial 2-D property that the doping concentration of the more lightly doped side of a p-n junction can be increased without lowering breakdown with the proviso that the total "charge" of the layer is limited. Specifically, the RESURF criteria stipulate that so long that a doped layer (drift region) in a reversed biased p-n junction becomes fully depleted before reaching the semiconductor's avalanche critical electric field E_{crit} then the *doping concentration* of the depleted layer does not determine the avalanche voltage. Immediately after its publication, a variety of vertical unipolar and bipolar conduction devices based on the RESURF principle of charge balancing were proposed [113] but being overly

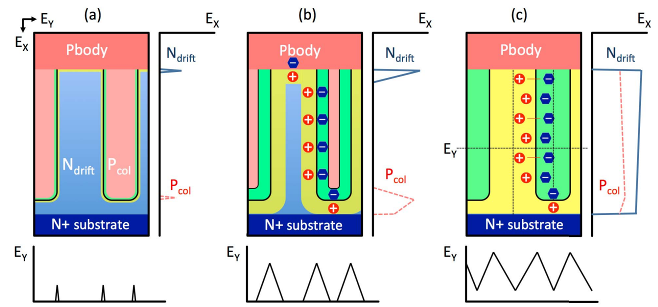

Fig. 10. Cross sections of a superjunction under increasing reverse bias. In the highest bias condition the n_{drift} and P_{col} become completely depleted and the vertical electric field in the n_{drift} becomes constant increasing breakdown.

complex and costly to fabricate, which were never reduced to practice.

Later, Chen [114] more pragmatically adapted the charge balance concept to vertical conduction in bulk silicon (rather than surface layers) by forming alternating columns of p-type and n-type materials of limited charge where *both sides* of the junction become fully depleted under reverse bias. Able to conduct vertically through multiple parallel highly doped n-drift regions, planar VDMOS based on this new "superjunction" or SJ concept achieved record low ON-resistances not only far outperforming its lateral RESURF predecessor but breaking the 1-D "silicon limit" identified a decade earlier. Commercial production of 600 V planar VDMOS commenced in 1998 [115].

The behavior of a superjunction diode under reverse bias is shown in Fig. 10. In the leftmost illustration [Fig. 10(a)], the junctions are only slightly reversed biased whereby the n_{drift} and p_{col} columns are not depleted. In the center drawing [Fig. 10(b)], an applied reverse biased causes ionization of donor atoms in the n_{drift} resulting in fixed positive depletion charge. By charge conservation, an equal number of acceptor atoms become ionized in the p-type column depletion region. Both vertical and lateral electric fields present across the depletion regions that have a characteristic triangular shape.

Upon an additional reverse bias, rightmost drawing [Fig. 10(c)] shows that the entire n_{drift} and p_{col} regions become completely depleted with immobile ionized donor and acceptor charges balanced laterally (along the y-axis) at every depth cross section. Because the charges are balanced laterally, the vertical junction between the p_{body} and n^+ substrate behaves as if it were undoped, i.e., intrinsic—similar to a p-i-n diode. As such the electric field along the vertical (x-axis) orientation of the n_{drift} column (and similarly in the p_{col} column) charges from a triangular profile to a nearly constant field value. Integrating the area under the electric field curve results in a much higher breakdown voltage than the voltage supported by the triangular electric field characteristic of a conventional 1-D p-n junction. Because the breakdown voltage is higher for the same epilayer thickness, a thinner epi-drift layer can be used to support a targeted voltage rating. In its ON state, a thinner drift layer exhibits a lower resistance, thereby improving the tradeoff between avalanche voltage and specific ON-resistance.

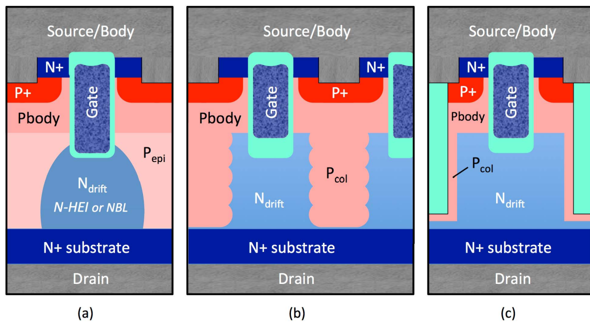

Fig. 11. Low voltage superjunction trench VDMOS cross sections. Devices include (a) trench bottom implanted n_{drift}, (b) p-column HE implanted, and (c) dielectrically filled deep trench with sidewall implanted p-type column.

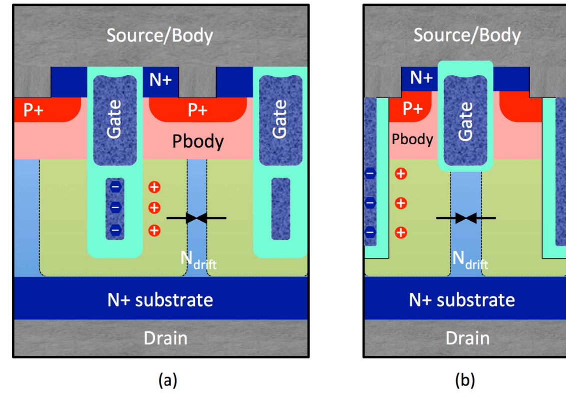

Fig. 12. MOS superjunction trench VDMOS cross sections. (a) Split gate. (b) Dual trench. n-drift must meet SJ charge criteria to completely deplete.

In short, a vertical superjunction can achieve a higher breakdown voltage using higher doping concentration and thinner layer provided the total charge is limited in accordance with the charge control principle of total depletion. In this context, the term "charge" refers to the multiplicative product of column concentration n_{col} and column width Y_{col}. For silicon, this the total charge of both n-type and p-type columns should meet the charge balance criteria $Q_{CB} = n_{col} Y_{col} \leq [m \bullet 10^{12}]$ cm^{2,} where m may vary from 1 to 4 depending on 2-D and 3-D considerations. While in high voltage devices requiring thick epitaxial layers, the columns are formed either using multiple epitaxial depositions or deep trench etching, in low voltage trench SJ VDMOS where the epitaxial layer is thinner, and other fabrication options involving deep diffusions or HEI implantation are also possible.

Fig. 11 shows three examples of trench SJ VDMOS implementations. In Fig. 11(a), the n_{drift} region is implanted with high energy through the trench bottom to form an n-column, counterdoping a p-type epitaxial layer or a deep p-type tub [116], [117]. The uncompensated p_{epi} layer or tub therefore forms the p-type column $p_{col,}$ while the trench width and the phosphorus implant dose determine the n-column charge n_{drift}. In center illustration [Fig. 11(b)], the p-type column is implanted into a n-type mesa region i.e., between the trenches, using multiple high-energy implants to compensate the n_{epi} [111], [118], where the implant width and dose defines the p-column charge. In Fig. 11(c), a deep trench with a p-type implant forms the p_{col} region. Adapted from 600 V superjunction devices, the trench may be filled with selectively deposited epitaxy [119], or may comprise a dielectric either oxide or a sealed air gap [120].

Using charge balance methods in a trench SJ VDMOS allows an increase in the average concentration of the n_{drift} drain region carrying conduction currents. Despite preventing current spreading and reducing the cross-sectional conducting area by half, the higher doping concentration is still able to achieve a significant reduction in drift resistance compared with conventional trench VDMOS. Combining charge balancing with TBOX or field plate trench gates have been shown to match the split-gate trench VDMOS in reducing Q_{GD} but without introducing the parasitic C_{GP} and C_{DP} capacitances, the superjunction device outperforms the split-gate device in achieving lower Q_{GS} and Q_G values.

Another type of change-balanced trench VDMOS can be realized using a MOS capacitor (rather than a p-type column) to balance the charge in the n_{drift} region. Like a p-n junction, an MOS capacitor induces a silicon depletion region under negative bias, i.e., where the polysilicon plate is biased at a more negative potential than the n_{drift} region. The immobile fixed positive charges of ionized donor atoms in the n_{drift} depletion region precisely counterbalance the negative charge (electrons) on the conductive field plate [121]–[129]. Unlike in the case of p-n junction charge balancing, in the SJ-like field plate trench VDMOS also known as RSO for RESURF stepped oxide, a polysilicon electrode capacitor is used to induce depletion of the n_{drift}. The electrode, mirroring the drift charge, may comprise a buried field plate in a split gate trench VDMOS shown in Fig. 12(a), or utilize a dedicated field plate in dual trench design [see Fig. 12(b)].

In either implementation, the n_{drift} total charge must meet the charge balance criteria, i.e., the n_{drift} must fully deplete before the 1-D vertical $p_{body}/n_{drift}/\ n^+$ substrate junction reaches its critical electric field and avalanche commences. Since the transistor's breakdown voltage and reverse blocking capability must be maintained in low frequency applications as well as during high speed pulse width modulation (PWM) operation, nonequilibrium MOS deep depletion cannot be used to satisfy the charge balance condition and the mesa between trenches must be designed accordingly using the mesa width and concentration to control the total drift charge.

Unlike in the case of the p-n junction superjunction where the p-type must meet the charge balance criteria, in the MOS-induced superjunction, the only requirement is that the field plate's isolation has to withstand the device's full blocking voltage across the dielectric at the trench bottom, a criteria mandating oxide thicknesses in the micron range. Accordingly, special care is required to avoiding thinning at the trench's bottom corners and to prevent formation of stress-induced defects along the trench's bottom edges and corners. The MOS field plate-based charge balanced trench VDMOS was first introduced commercially for –20 and –30 V p-channel devices in 2001 and at comparable voltages for n-channel trench devices a year later [121]. Later, charge

balancing in RSO-type trench VDMOS was extended to higher voltages [123], [130].

Both superjunction and RSO type charge-balanced trench devices exhibit low gate-charge characteristics and high switching speeds while maintaining good avalanche ruggedness providing an excellent alternative to conventional trench VDMOS [131]. Unlike conventional trench VDMOS, however, trench charge balanced devices manifest a nonlinear voltage dependence of drain-to-source capacitance C_{DS}. At low voltages, drain-to-body p-n junction capacitance C_{DS} varies according to a linear relationship $V_{DS} \propto 1/C_{DS}^2$ for step junctions, declining smoothly with reverse bias V_{DS} consistent with 1-D expansion of the junction's depletion region. At the onset of the 2-D charge balancing (RESURF) effect, the n-type drift region becomes completely depleted (shielding the p_{body} junction). Once depleted, the space charge distance between the body and the undepleted portion of the drain, i.e., the capacitor's dielectric thickness, greatly increases invoking a commensurate drop in junction capacitance, and behaving *as if* the surface area of the junction suddenly decreased. Left uncompensated, this rapid C_{DS} decline can, in high frequency switching applications, produce switching noise, oscillations, and other circuit instabilities. Methods to compensate the effect include introducing additional linear capacitance across the device or employing integrated snubber (filter) circuits [132]–[134].

Because of differing advantages of various trench technologies, trench VDMOS optimized for minimum ON-resistance, minimum switching losses, avalanche operation, and for other conditions (such as diode conduction in synchronous rectification) likely employ different processes and design concepts. As such, the trench power MOSFET market is expected to remain fragmented technologically for the foreseeable future, with a trend toward diversity and *application specificity* (detailed in The Trench Power MOSFET, Part II) rather than technological homogeneity.

D. Trends in $Q_G R_{DS}$ and $R_{DS}A$ FOM

As described herein, in trench VDMOS numerous process and design tradeoffs exist between achieving the lowest specific ON-resistance $[R_{DS}A]$ (mΩmm^2) and minimizing specific gate charge $[Q_G/A]$ (nC/mm^2). In switching applications such as high-frequency dc/dc converters, both factors are important. As such an FOM describing the tradeoff between $R_{DS(on)}$and Q_G is required. By combining (1)–(3), a switching FOM (4) for power devices $[Q_G R_{DS}]$ can be expressed as

$$[Q_G R_{DS}] = [R_{DS}A][Q_G/A] = ([\text{A/W}][R_{ch}W] + R_{drift}A)[(Q_{GS} + Q_{GD})/A]. \quad (4)$$

Fig. 13 shows the trend in the $R_{DS(on)}$ and $[Q_G R_{DS}]$ FOM of various voltage power MOSFETs below 200 V [135], [136]. This FOM considers geometric packing density, channel resistivity, drift resistivity, gate-to source charge, and gate-to-drain charge to measure a device's switching performance. ON-resistance and gate charge data are based on published data sheet comprising typical values

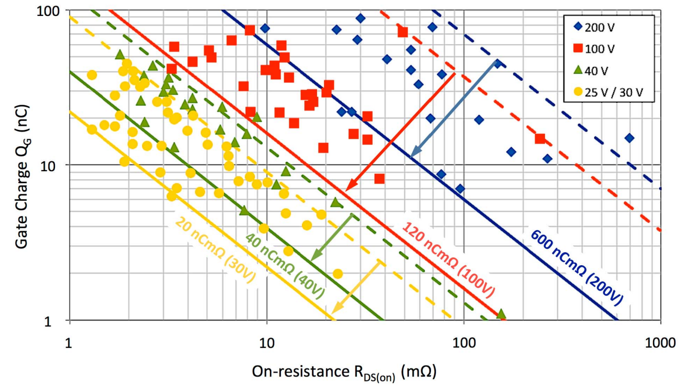

Fig. 13. Trend in power MOSFET on-resistance and gate charge. Constant $Q_G R_{DS}$ lines show 200 V (blue), 100 V (red), 40 V (green) and 30 V (yellow).

(not max ratings) with 10 V gate drive for 100 and 200 V devices and 4.5 V gate biases for 20–40 V devices.

Compared with previously reported results (dashed lines), present day state-of-the-art devices (solid lines) exhibit 20 nCmΩ (or pC•Ω) at 30 V, 40 nCmΩ for 40 V devices, 120 nCmΩ for 100 V devices, and 600 nCmΩ for 200 V devices. With each new generation, the $[Q_G R_{DS}]$ product improves further. Because of application specificity, the industry's lowest ON-resistance devices often do not represent the best switching devices, i.e., trench VDMOS having best-in-class $[Q_G R_{DS}]$ FOMs. For example, one 40 V trench VDMOS [137] has a typical $R_{DS(on)}$ of 0.54 mΩ at V_{GS} = 10 V and 0.8 mΩ at V_{GS} = 4.5 V, notably low resistances (especially considering package resistance is major factor in this range). With 81 nC of gate charge at 4.5 V, the resulting $[R_{DS}Q_G]$ = 65 mΩnC is, however, far from the state of the art in switching performance. As such, the device offers superior performance in conduction loss dominated applications, e.g., motor control, but is not optimum for switching-loss dominated apps, such as multimegahertz dc/dc conversion. Fig. 14 shows a sampling of published specific ON-resistance data [138] for conventional and TBOX trench VDMOS with comparisons to superjunction and field-plate superjunction (RSO) versions.

While trends in $[Q_G R_{DS}]$ can be data-mined from published data sheets, the reported values of specific ON-resistance $R_{DS}A$ are more difficult to obtain or substantiate, in part because no single standard exists on how to measure and whether to include or exclude various resistive components such as metal spreading resistance, active versus total die area, substrate resistance, contact resistance, and lead resistance.

V. TRENCH VDMOS RELIABILITY

Trench VDMOS reliability must consider two major sets of criteria. The first criteria relate to its manufacturing, i.e., insuring the device is fabricated in a well-controlled manner consistent with statistical process control methods. Critical unit processes relate primarily to the trench etch, the gate oxidation, the trench top oxidation and planarization, and the contact etch process. Trench fabrication related defects include I_{GSS} and I_{DSS} failures at final test or life failures after HTRB and

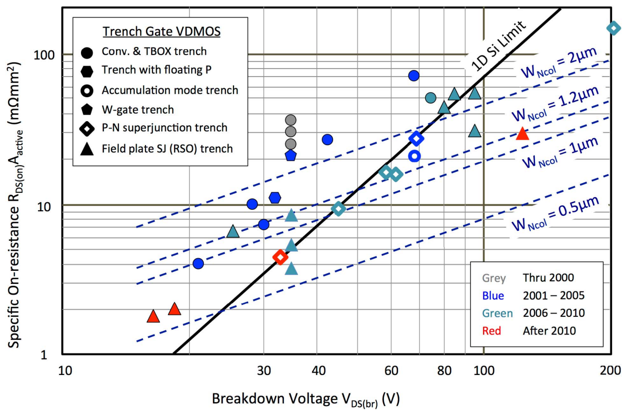

Fig. 14. Trench VDMOS specific on-resistance versus breakdown voltage.

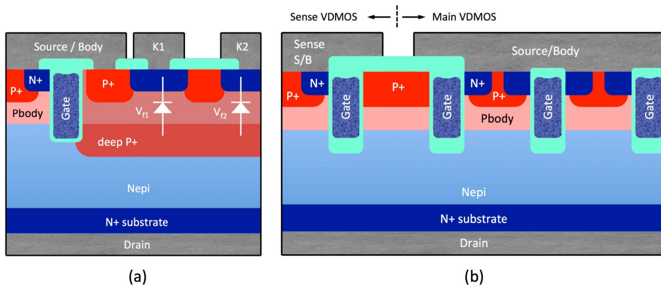

Fig. 15. Trench VDMOS with integrated sensors. (a) Differential p-n junction temperature sensing. (b) Current-mirror current sensing.

high-temperature gate-bias testing. Another important manufacturing consideration concerns the time duration after trench etching until the trench is oxidized and filled (i.e., sealed). After etching, the trench should not be exposed to organic compounds (photoresist byproducts), which can contaminate the etched surface. Studies also show that leaving the etched trench exposed and unfilled for extended durations of time can lead to I_{GSS} gate failures or threshold instability in life testing.

A second set of trench VDMOS reliability considerations relate to its application, i.e., the electrical conditions imposed on the device in various classes of applications including UIS, repetitive avalanche, safe operating area, hard commutation (diode reverse recovery), and hot-carrier generation in saturation (current source operation). Application related reliability issues are considered in greater detail in The Trench Power MOSFET (Part II). Aside from application specificity, overtemperature and overcurrent represent two generic reliability concerns that may arise in any application. Because of thermal resistances in the die and package and heat propagation delays introduced from thermal mass, monitoring a trench VDMOS's junction temperature remotely from the PCB or even on its leadframe is too slow and inaccurate to be used to protect the device.

Instead, thermal protection can be achieved by employing a "temp-sense" trench VDMOS, realized as shown in Fig. 15(a) by introducing an *in situ* thermal monitor within the trench VDMOS itself comprising one or two forward biased p-n junctions [139].

Since the forward biased voltage of a diode shifts at approximately 2.2 mV/° C (depending on current), the diode voltage can be used to calculate the device's junction temperature. To avoid unwanted bipolar transistor conduction, the n+ junction sensor diode should be formed within the deep p+ region so the parasitic n-p-n beta (current gain) is well below unity, i.e., $\beta_{n-p-n} << 1$. In an improved version, two diodes biased at different currents are used to monitor the temperature as a changing *difference* in forward biased voltage with temperature. The analog circuit advantage of this differential technique is that a differential signal does not require calibration and is immune to common-mode noise (such as displacement currents arising from rapid dV_{DS}/dt transitions during switching). In operation, if an overtemperature condition is detected by external driver circuitry monitoring the temp sensor, the device can be turned OFF or its duty factor reduced to limit heating. Temperature protection is, however, not applicable for UIS. If an overtemperature arises during UIS, nothing can be done to reduce the heating while the inductor delivers its energy into the avalanching power device.

Another reliability related operating risk is an overcurrent condition arising from a short circuit or in motor drive from a stuck rotor. While an external current sense resistor may be connected in series with the trench VDMOS, introducing additional series resistance requires a larger lower resistance power MOSFET to be used to compensate for the added resistance. The sense resistor also adds unwanted stray inductance. The alternative for ultralow resistance switches is to employ a current-sensing trench VDMOS shown in Fig. 15(b), integrating a current mirror into the device by separating a small group of source cells to measure a fraction of the current flowing through the main device [140], [141]. For example, using a 10 000:1 sense cell ratio, when the main power device is conducting 100 A, the sense cells carry only 10 mA, producing a 10-mV sense signal in a 1-Ω sense resistor. By monitoring the sense resistor voltage, an over current condition can be detected and the transistor's gate shut OFF or circuit bias conditions changed [142], [143].

VI. Future Prospects

The future of adopting trench MOSFET technology to new semiconductor materials is very encouraging. In a manner similar to silicon trench device design, wide-bandgap (WBG) semiconductors such as SiC and GaN can be adapted to fabricate trench gate devices with vertical conduction, outperforming their lateral and planar VDMOS counterparts [144]–[147]. Notably, because of their intrinsically high avalanche critical electric fields, device designs and material thickness producing a 40 V device in silicon results in high voltage breakdown devices, e.g., over 600 V (depending on the material) when fabricated in WBG semiconductors.

Trench SiC VDMOS offer better specific ON-resistance than planar SiC MOSFET structures due to the elimination of the JFET region. SiC trench MOSFETs shown in Fig. 16(a) with high blocking voltage and high speed switching capability have been demonstrated. A double-trench SiC DMOS structure that has both source trenches and gate trenches as shown in Fig. 16(b) was also reported. The SiC devices achieved the reported breakdown voltages of 630 and 1260 V with the

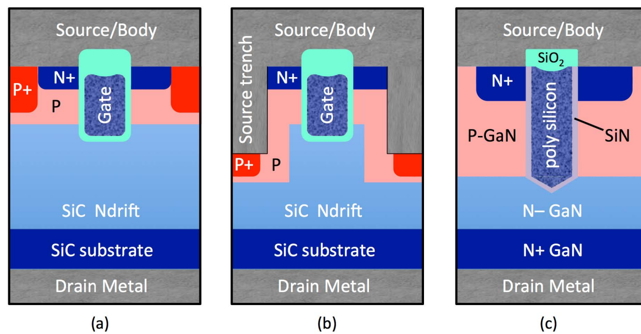

Fig. 16. Cross section of WBG trench VDMOS including (a) trench-gate SiC, (b) dual-trench SiC, and (c) trench gate GaN.

specific ON-resistances of 79 and 141 mΩmm^2, respectively. Lower voltage targeted SiC devices have not yet been demonstrated. Fig. 16(c) shows a trench MOSFET structure using GaN material that achieved a breakdown voltage of 180 V. Although promising, the use of WBG materials in trench VDMOS is not without challenges. First, the semiconductor–insulator interfaces formed using WBG materials are significantly worse than that of Si–SiO_2, exhibiting degraded channel mobility, interfacial charge states, and frequency-dependent charge trapping.

Another challenge involves the stability and field strength of the gate dielectric, especially when operating over extended durations. While further optimization of the gate dielectric formation may improve its reliability, an alternate approach is to shield the gate from high fields using a series JFET such as shown in the dual trench device of Fig. 16(b) or alternatively to select a more favorable lower charge crystal plane for the trench surface. As with any series connected element, the JFET adversely impacts specific ON-resistance.

Aside from WBG devices, other ongoing developments in trench VDMOS devices include efforts in enhanced channel mobility devices [148], [149], in ultrathin substrate fabrication [150], in thin silicon bonded to copper [151], in the integration of trench lateral DMOS (trench LDMOS) into integrated circuits, in the development of application specific trench DMOS, in the use of ultralow parasitic resistance and inductance packages, and in improving trench VDMOS reliability in particular applications. Application specific trench VDMOS have, thus far, been developed and commercialized for dc/dc converters and synchronous rectification, for the Li–ion battery disconnect switch, for solenoid valve drivers used in vehicle ABS, for motor drive, and in airbag squib drivers for controlling airbag inflation rates. The discussion of packaging, reliability, application specific trench VDMOS, and trench LDMOS are described in detail in The Trench Power MOSFET (Part II).

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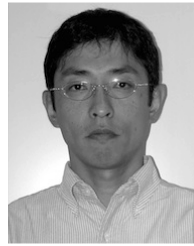

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