The Trench Power MOSFET—Part II: Application Specific VDMOS, LDMOS, Packaging, and Reliability

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(Invited Paper)

***Abstract*— The technological development of application specific VDMOS and lateral trench power MOSFETs is described. Unlike general-purpose trench vertical DMOS, application specific trench DMOS comprise devices merged or optimized for a specific function or characteristic. Examples include the bidirectional lithium ion battery disconnect switch, the airbag squib driver with safety redundancy, the antilock breaking systems solenoid driver with repeated avalanche operation, and various forms of synchronous rectifiers (including integrated Schottky and pseudo-Schottky operation). Trench lateral DMOS include all implant quasi-vertical, lateral trench, and lateral trench charge balanced devices. Trench power MOSFET packaging addresses multichip surface mount, DrMOS, low inductance, and clip lead packages.**

***Index Terms*— Airbag, antilock breaking systems (ABS), avalanche breakdown, avalanche energy, barrier-lowering, bidirectional lithium ion battery disconnect switch (BDS), boost, break-before-make (BBM), Buck, clip lead, drift region, ESD protection, gate charge, gate drive loss, heat tab, high-side switch (HSS), lateral DMOS (LDMOS), lightly doped drain, low-side switch (LSS), motor drive, polysilicon diode, power device packaging, power dissipation, power MOSFET, power transistor, pseudo-Schottky effect, pulsewidth modulation (PWM), Q_G, Q_{GD}, Q_{rr}, RESURF, RESURF stepped oxide (RSO), reverse recovery, Schottky, silicide gate, silicon, solenoid driver, specific ON-resistance ($R_{DS}A$), superjunction, switching voltage regulator, thermal resistance, trench gate, trench lateral DMOS (LDMOS), unclamped inductive switching (UIS), VDMOS.**

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I. Introduction

THE widespread commercialization of the vertical trench power MOSFET in the 1990s was driven by its unparalleled adoption of the device in motor drive, in battery protection, and in switching power converters. Capitalizing on record low ON-resistances, early trench power MOSFET users focused on applications where high efficiency and low power dissipation were tantamount, especially in the emerging markets of notebook computers, cellphones, and hard drives.

Rather than compete on a cost basis against conventional planar VDMOS packaged in large heat spreader packages (such as the DPAK), marketing of trench discrete power devices in the early 1990s primarily targeted space-constrained applications unable to dissipate power or accommodate large power packages [1]. Using small footprint surface mount packages considered *at that time* unsuitable for power applications (e.g., the SOP-8 and TSSOP-8), early trench VDMOS was promoted for efficiency with a philosophy that "the best way to eliminate heat is not to dissipate it in the first place," [2] filling each package cavity with the largest lowest resistance die possible. This thermal strategy was immediately embraced by automotive applications where, due to high ambient temperatures in the engine compartment, dissipating excess power and removing heat is perpetually problematic [3].

Later in 1997, the commercial-launch of high-density trench power MOSFETs (nearly triple the density of the prior generation) [4] extended power performance levels into the TSSOP-8 and to the ubiquitous small footprint SOT-23 package [5]. The smaller packages enabled yet another cycle of miniaturization in portable consumer, (portable) computers, and communication products. For desktop-computer switching regulators, where size or excess power dissipation was considered less important than cost, widespread adoption of the trench power MOSFET did not occur till the turn of the century [6] when devices finally became competitive to planar devices on a cost-performance basis [i.e., having comparable $\$ \cdot R_{DS}$ figure of merits (FOMs)]. Enabled by trench VDMOS, switching regulators and energy-saving "tiered" power architectures [7] have recently begun to displace "always on" linear regulators even in cost sensitive ac powered consumer products (such as TVs, set top boxes, and appliances), inspired in part by green initiatives (such as Energy Star) and by legislative pressure.

In retrospect, the trench power MOSFET was, from its very inception, *application specific*, first addressing compact low-power-loss applications not served by planar VDMOS, then migrating into high frequency dc/dc conversion where gate-charge became an important parameter in device and circuit optimization. Over time, the basic trench power MOSFET spawned a large family of derivative devices specifically created for select applications, such as antilock breaking system (ABS) brakes, airbags, lithium ion battery protection, motor drives (e.g., hard disk drives), and high-frequency synchronous Buck converters. Each application likewise demanded its own unique packaging solution. Later, lateral versions of trench power devices capable of integration with analog and digital circuitry in application-specific BCD power ICs also emerged [8].

II. Packaging Considerations

As a general-purpose discrete device used in applications switching at subMHz frequencies, the key electrical parameter of the trench vertical double-diffused MOSFET (or trench VDMOS) of primary concern is its specific ON-resistance $R_{DS}A$ or R_{sp}. Representing a FOM in its conductive state, specific ON-resistance (having units of $m\Omega mm^2$ or $m\Omega cm^2$) is used to describe how large of a semiconductor die is needed to realize a device with a specific target resistance. Ostensibly, the concept is simple–the ON-resistance of any power MOSFET of a given OFF-state breakdown voltage is defined by the specific ON-resistance of the device divided by its active area, i.e., $R_{DS(ON)} = [R_{DS}A]/A$, where area and ON-resistance exhibit a simple inverse relationship and where specific ON-resistance increases with breakdown voltage [9], [10]. That said, scaling trench VDMOS devices to higher densities and lower specific ON-resistances is not without its challenges.

A. Managing Package-Related Resistance

To better understand overall device performance, we must consider not only the active trench VDMOS but the parasitic resistance contributed by the package and wire bonds, the die's top metallization, and at higher cell densities, even the silicon substrate itself. According to (1), numerous resistance components such as top metal 2-D-spreading resistance R_{metal}, bond wire resistance R_{wire}, and package resistance R_{pkg} do not scale with the die's active area A

$$R_{DS(ON)} = [R_{DS}A]/A + (R_{metal} + R_{wire} + R_{pkg}). \quad (1)$$

Even using a large number of bond wires, these parasitic resistances comprise several milliohms of total resistance. In a 100-mΩ device, the parasitics are negligible, but in a 5-mΩ device, their contribution may represent 25%–40% of the product's total resistance, requiring a larger silicon die and higher cost to offset. The impact of package and wire resistance is further exaggerated as cell densities are increased and specific ON-resistance is lowered. Fig. 1(a) shows a direct comparison of device ON-resistance and gate voltage dependence of two successive generations of trench DMOS packaged in a bond-wired SOP-8 package [6].

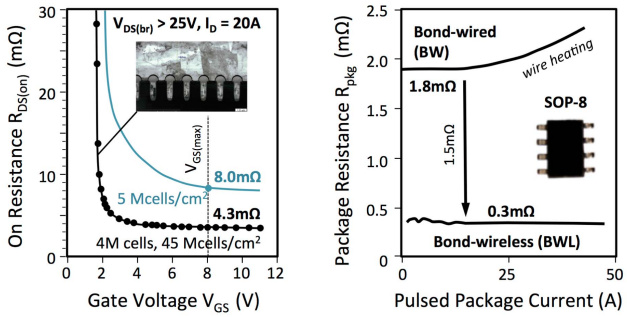

Fig. 1. SOP-8 trench VDMOS resistance. (a) V_{GS} dependence of 5 and 45 Mcell/cm^2 devices. (b) Package resistance of bond wire versus clip lead (BWL).

TABLE I
Comparison of Components of Resistance for Bond-Wired and Bond-Wireless (BWL) SOP-8 Assembles as a Function of Trench Cell Density

SOP-8 Package Assembly Type	Bond-wired (BW)		Clip-lead (BWL)	
Package Resistance (mΩ)	1.8		0.3	
Device Cell Density (Mcell/cm^2)	5	45	5	45
Die Resistance (mΩ)	6.2	2.5	6.5	2.5
Total Resistance (mΩ)	8.0	4.3	6.8	2.8
% Parasitic Resistance	23%	42%	4%	11%

The devices are rated for 25 V breakdown and 20-A pulsed current applications where package and PCB thermal impedances set the maximum usable duty factor. As shown, the lower cell density device (5 Mcells/cm^2) exhibits a classic hyperbolic gate bias dependence with a minimum ON-resistance at $V_{GS} \geq 8$ V of 8 mΩ including die, bond wire, and package resistance. At 45 Mcells/cm^2, the higher cell density technology results in an SOP-8 sized device containing four million active trench VDMOS cells. Because of its enormous transconductance, the device's gate bias turn-ON dependence exhibits a steep "L-shaped" curve, approaching its minimum value of 4.3 mΩ with only 3 V of applied gate bias. This extremely flat resistance characteristic independent of gate bias indicates the majority of total device resistance is not from the channel and die resistance, but from parasitics.

Fig. 1(b) shows the measured characteristics of the SOP-8 package and bond wire resistance as a function of current, revealing parasitics contributes 1.8 mΩ, or as described in Table I, 23%–42% of the total product resistance. Interestingly, even in pulsed power testing, bond wire heating contributes an added increase in overall package resistance.

Whenever the resistance of a packaged product is significantly impacted by parasitics, the benefit of scaling cell densities becomes compromised. The only viable alternative to further enable trench VDMOS device evolution is to concurrently address the underlying package problem, using clip lead or sandwich package assembly methods to eliminate bond wires while maximizing the ratio of die area to package footprint [11]–[14]. As shown in Fig. 1(b), bond wireless assembly lowers package-related resistance by more than 85% to 0.3 mΩ and is not subject to current dependent wire heating. As described in Table I, parasitic resistances can be reduced from a 42% contribution to only 11%. Fig. 2 shows a variety

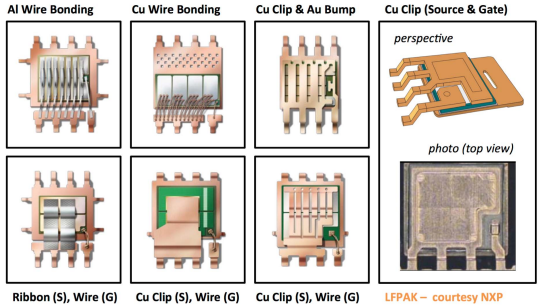

Fig. 2. Example of bond-wire and clip-lead power SOP-8 leaded packages.

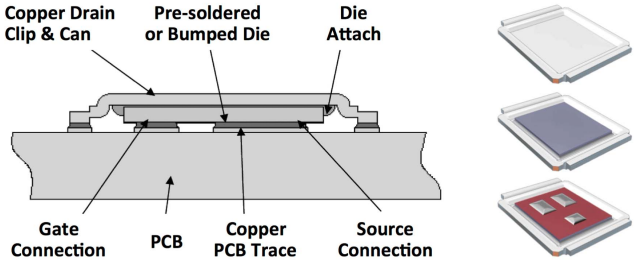

Fig. 3. Cross section of sandwich package power device die assembly.

of high-current SOP-8 power packages contrasting bond wires to various clip lead assemblies [15].

Still another method involves sandwiching the die between two conductors, either two lead frames or a leadframe and the PCB copper traces [16], [17]. One such design shown in Fig. 3 utilizes a direct contact between the device's source and gate with the underlying PCB traces using a bumped or pre-soldered layer. The backside of the die, i.e., the drain connection, is die attached to a copper clip or "can," which covers the die and carries current to the PCB as well as serving as a heat sink and convective surface. Aside from its thermal resistance benefit, the assembly greatly reduces package inductance and parasitic resistance. Other methods sandwich the die between two copper leadframes, providing cooling from both package sides.

Albeit more expensive to assemble, eliminating bond wires using a clip lead or sandwich package not only improves ON-resistance but also improves switching performance and efficiency. In particular, by eliminating bond wire and top metal resistance, a smaller die with lower input capacitance and gate charge may be used to achieve the same product resistance specification, in applications manifesting lower gate drive losses than its bond-wired counterpart. Eliminating bond wires also reduces parasitic package inductance. Fig. 4 graphically shows a comparison of the resistance and inductance of various power packages [13], [14], [18] highlighting the benefit of bond-wireless and clip lead packages. Precise values vary by supplier and manufacturing method.

B. Multidie Packaging

To address space sensitive portable applications, dual isolated trench power MOSFETs can be integrated into a single surface mount package by utilizing separate die pads with exposed backsides [19]. Because, however, of the requirement to maintain coplanarity among the package leads and the

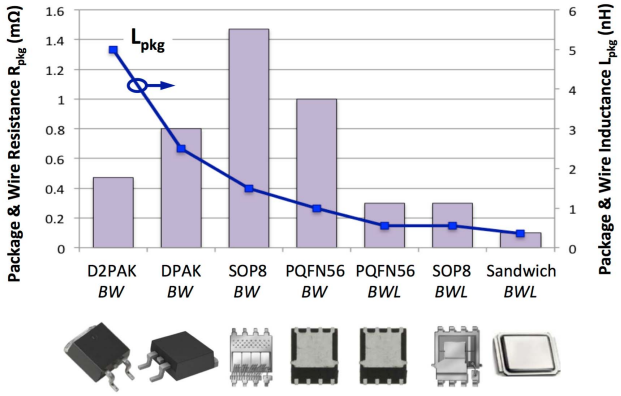

Fig. 4. Power package parasitic resistance (bars) and inductance (line).

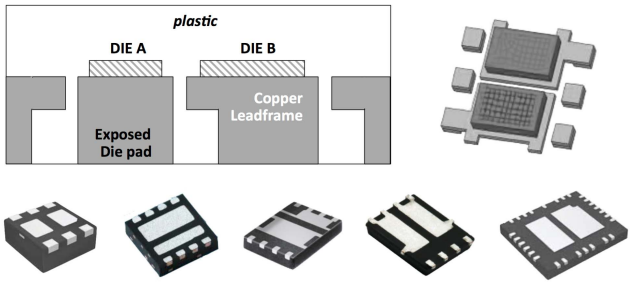

Fig. 5. DFN packages used for trench power MOSFETs.

two die pads, gulls-wing surface mount packages are ill suited and difficult to manufacture. Instead, adapting dual die leadless (DFN) leadless packages where the leads and heat slugs are formed from a common copper leadframe as shown in Fig. 5 is preferable. In package design, care must be taken to insure adequate intrapad spacing to avoid PCB solder shorts. Moreover, older PCB factories using wave solder assembly cannot assemble leadless packages such as the PQFN, PDFN, or chip scale packages, because the solder cannot be applied beneath the die.

While most system architectures involve packaging the MOSFETs separately from their control and drive circuitry, in high frequency dc/dc conversion requiring precise regulation during rapid transients, it is beneficial to combine the gate driver with the trench power MOSFETs. As shown in Fig. 6, the integrated driver-MOSFET combination, or DrMOS [20], [21], comprises a three-die half bridge with a small high-side switch (HSS) and a larger low-side switch (LSS) synchronous rectifier (both comprising n-channel trench VDMOS) along with a controller and buffer IC for driving the power devices. The controller performs the important task of shoot-through protection with "break-before-make" (BBM) circuitry. The driver also includes the bootstrap diode function for charging the flying capacitor (not part of the driver), and various safety functions such as overtemperature and overcurrent protection.

Other multidie package solutions combining trench VDMOS with control ICs also exist, applicable for automotive applications, for valve or solenoid drivers, speaker drivers, high-capacity battery packs, and more. In the case of motor drive, H-bridge, voice-coil, or three-phase bridge driver implementations require a module assembly comprising a control IC

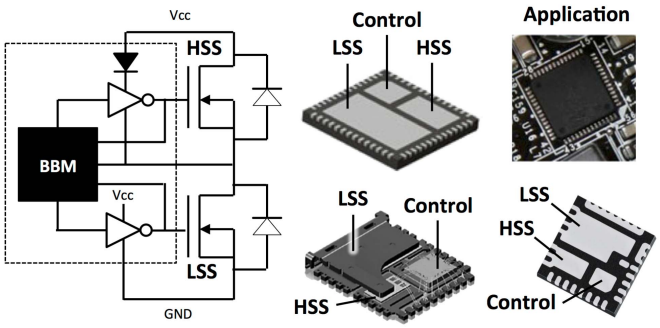

Fig. 6. DrMOS comprising driver IC copackaged with trench VDMOS.

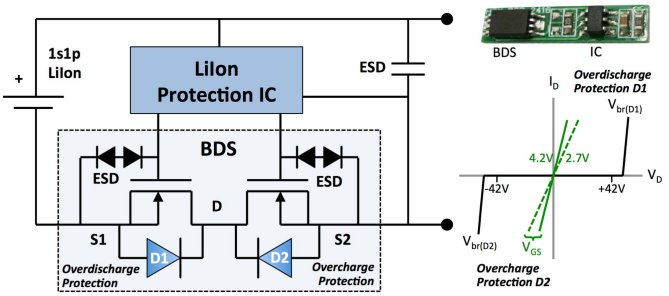

Fig. 7. Simplified Li–ion protection schematic and BDS operation (1s1p).

with four to six separate trench VDMOS die packaged into a single power module [22].

III. Application Specific Trench VDMOS

Aside from achieving record low ON-resistances and offering high-frequency switching capability, trench VDMOS can be optimized for an application's needs by targeting specific electrical loads (resistive, capacitive, inductive, and battery) and by designing the device to operate in concert with the application by adapting to changes in control, input, or load conditions.

A. Lithium Ion Battery Disconnect Switch

One important development in application specific trench power MOSFETs is the development of the battery disconnect switch for lithium ion batteries, the indispensible energy source of the mobile device revolution [23]–[25]. Because lithium is a highly reactive group-I element (atomic number 3) with a single outer shell electron, the atom easily ionizes participating in highly energetic reactions. Its reactivity is the reason for lithium ion and lithium polymer batteries' high energy densities but also responsible for a corresponding safety risk [26], [27] specifically its propensity to overheat and catch fire if improperly operated.

Multiple layers of safeguards are employed to minimize Li–ion fire risks, including overvoltage protected intelligent battery chargers, the exclusive use of only CE certified ac power adapters, strict quality control in cell manufacture (by reputable International Standard Organization certified suppliers), and unique protection circuitry–specifically a battery disconnect switch or BDS, embedded within the Li–ion battery pack itself. As a last line of defense in case the BDS fails, high-quality lithium ion cells incorporate a *bilayer separator* [28]–[30], a thin film having two layers with different temperature coefficients of expansion that in the case of overheating prevents mixing of electrolytes by halting the electrochemical reaction.

Operation of the Li–ion battery disconnect switch is uniquely matched to the specific battery chemistry to prevent both overcharging, i.e., overcharging protection (OCP), and to provide overdischarge protection (ODP) [31]. Failure to reliably perform these functions can have catastrophic consequences [32], [33]. In normal operation, the BDS must allow current to flow in both directions—supplying energy from a charger into the Li–ion cell during charging, and allowing current to flow in the opposite direction during discharging, i.e., during use. As such, the BDS must be capable of high-current bidirectional conduction at a low resistance and bidirectional blocking.

A simplified schematic of the BDS function for a single-series cell, single cell Li–ion battery pack is shown in Fig. 7. Pack protection includes a TSOP-6 sized Li–ion protection IC controller and a TSSOP-8 packaged battery disconnect switch (BDS) comprising two trench VDMOS sharing a common drain D, where source S1 of the ODP switch connects to the cathode of the Li–ion cell and where source S2 of the overcharge protection device connects to the pin of the battery pack. The circuit also includes a capacitor and/or transient voltage suppressor to protect the entire pack from ESD damage. Because the gates connect to external pins subject to static discharge, BDS trench VDMOS includes a bidirectional ESD protection diode across its gate to source connections, an uncommon feature in trench VDMOS [34].

Charging a Li–ion even slightly beyond 4.28 V creates a potentially dangerous condition that can cause the cell to overheat and catch fire. The critical function of the OCP device during charging is to cut off current flow whenever the protection IC detects an overcharge, overcurrent, or overtemperature condition. During discharging (when the battery is acting as a power source), current flows in the opposite direction. If the cell becomes deeply discharged, conductive filaments will grow within the electrochemical cell creating permanent damage and the risk of a cell short. The minimum safe voltage varies by cell chemistry and by the anode material, but most controllers cut off discharge at 2.7 V or if an overcurrent or overtemperature condition is detected.

In operation, total BDS series-sum resistance of both devices depends on the current rating of the pack, varying from 100 mΩ for consumer devices to 25 mΩ for higher current smartphones and tablets. The lower resistance specs are especially challenging because of the small available PCB area (see photo inset) and because the specified resistance must be achieved with a minimum gate drive of only $V_{GS} =$ 2.7 V. By merging two trench VDMOS into a single die sharing a common drain, a bidirectional BDS [35], [36] can be monolithically integrated as shown in the cross section of Fig. 8. The integrated trench VDMOS BDS is application specific, offering improved specific ON-resistance over discrete and multichip implementations.

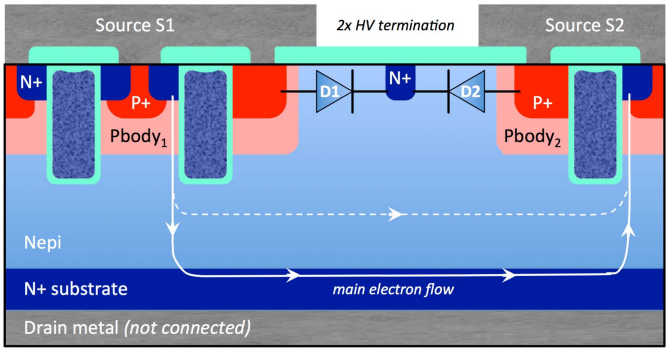

Fig. 8. Dual common-drain trench VDMOS BDS cross section.

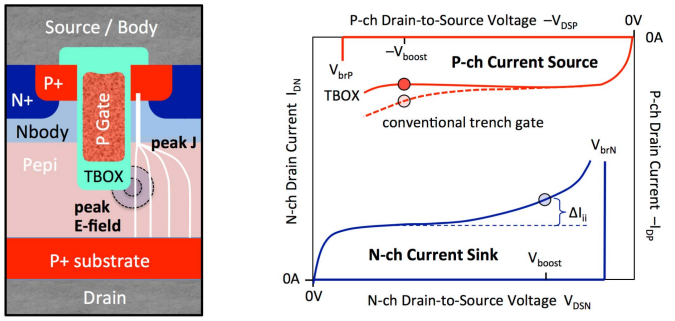

Fig. 9. Impact ionization in n-ch and p-ch trench VDMOS current sources. p-ch exhibits less preavalanche impact ionization offering a more ideal saturated current curve (greater small-signal impedance in saturation).

Operationally, during charging electrons flow from source S1 through the channel formed in $Pbody_1$ and into the common drain, where the currents flows laterally beneath the high voltage terminations separating the two devices and back up to source terminal S2 through the channel formed across $Pbody_2$. Although some of the lateral current flow occurs within the n_{epi} region, because of its heavy doping the majority of lateral conduction occurs in the n+ substrate. As shown, the drain metal does not connect to any external connection, yet the presence of the backside metal acts as a shunt to the substrate, further reducing total BDS resistance.

In the event of an overcharge condition the channel across $Pbody_2$ is shut OFF by gate G2 and diode D2 comprising the $Pbody_2$ to nepi junction blocks any further charging current. During discharging the device works similarly except the polarity and direction of electron flow reverses. Because the BDS must block in either direction, the region between the two devices comprises two back-to-back high voltage terminations with an intervening n+ channel stop to prevent surface leakage between the opposing Pbody regions. For devices in the range of 27–45 V commonly used in Li–ion packs comprising only cell (referred to by the cell configuration 1s1p meaning one-series, one parallel cell), a field plate termination method normally suffices to meet a stable breakdown voltage.

For multicell Li–ion packs such as two-cell 2s1p and 1s2p dual-cell configurations used in professional video camcorders; 3s1p, 3s2p, and 4s1p used in notebooks, and high voltage Li–ion packs used in electric vehicles (e.g., 50s2p), additional functions are required for cell balancing (to maintain uniform cell aging) and failsafe protection [37]–[39], requiring higher voltage trench power MOSFETs used throughout the system. Lithium ion (and lithium ion polymer) battery protection represents one of the highest annual volume uses of the trench power MOSFET. Driven by mobile devices, the emergence of hybrid and electric vehicles, and new cell chemistries [40], battery protection demand is expected to grow unabated for the foreseeable future. Future developments in solid-state Li–ion batteries with reduced fire risk are now also in development.

B. Airbag Redundant Squib Driver System

Another important application for trench VDMOS is the squib driver for airbag supplemental restraint systems (SRS) used in automobiles. The pyrotechnic squib is a gas generating explosive device that inflates an air bag at a rate proportional to the current (total energy) delivered to the inflator during a collision. To insure the airbag does not accidentally inflate or deploy too quickly (potentially injuring the occupant), the driver circuit employs not one, but two trench VDMOS in series with the squib [41]—one operating as a constant current source, the other operating as a switch using pulsewidth modulation (PWM). By controlling current and PWM duty factor, the inflation rate [42] is matched to an occupant's size and weight.

The constant current source may be realized using either a p-channel or an n-channel trench VDMOS, typically rated at 60–80 V. A comparison of the operating characteristics of the p-channel and n-channel trench devices shown in the I–V characteristics can be used to determine which device makes a more ideal constant current source [3]. Fig. 9 illustrates that the magnitude of any deviation in drain current ΔI_D resulting from impact ionization is less in the case of the p-channel trench VDMOS, primarily because holes exhibit a greater effective mass and a lower ionization coefficient than electrons. Although circuit techniques can be used to compensate for sub-avalanche generation currents, the risk of hot carrier damage from electrons is greater than holes.

By incorporating thick bottom oxide (TBOX) into a p-channel trench VDMOS shown by cross section, the location of the peak current density J_D in the epitaxial drain of a saturated device can be misaligned from the peak field location, significantly reducing impact ionization rates. As such, a p-channel trench VDMOS with TBOX is an attractive candidate for a reliable high-voltage current source and preferable over n-channel alternatives, especially since $R_{DS}A$ is not critical for operating in saturation, i.e., at large V_{DS}.

Utilizing an unusual electrical network topology shown in Fig. 10, in an airbag squib driver circuit, the squib is connected *in series* with two devices, not as a half-bridge, but as a *redundant* power switch to avoid an accidental deployment of the airbag.

When a collision is detected, the n-channel LSS trench VDMOS is pulsed as a switch using PWM with its duty factor D adjusted to control the air bag's inflation rate. Concurrently, the p-channel high-side trench VDMOS is turned on

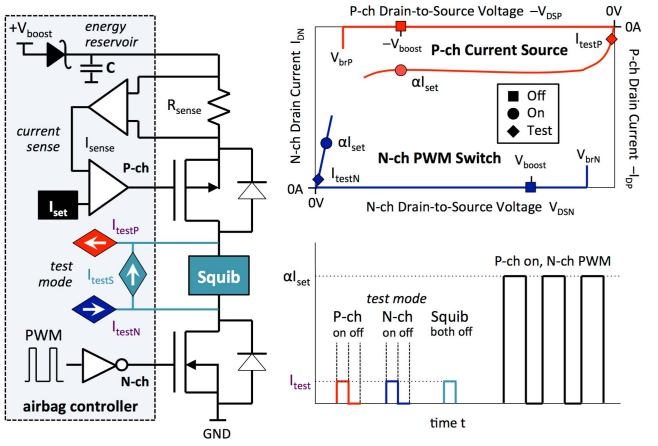

Fig. 10. Redundant trench VDMOS switch and control circuit for airbag SRS squib driver. Small test currents check switch and squib status. In a collision, energy in capacitor C is pulsed through squib to control airbag inflation.

in its saturation region of operation to a fixed current αI_{ref} using feedback from current sense resistor R_{sense} to provide closed loop control. Together the constant current p-ch sets the airbag's *maximum* inflation rate and n-ch duty factor D provides PWM control.

The power used to drive each airbag is created by a boost converter (not shown) and stored on capacitor C at 40–60 V individually for each squib. The Schottky diode isolates that this reservoir capacitor from the battery in case the battery is damaged (or shorted) during a front-end vehicle collision. Because accidental airbag inflation can cause a fatal malfunction, dual-switch redundancy prevents a short of either VDMOS from completing the circuit and accidentally igniting the squib. Similarly, because the squib is not directly connected to either supply rail, a single point failure, i.e., a malfunction, connector short, or wire short on either side of the squib, will not fire the squib so long that the two VDMOS remain off.

For maximum safety, the two switches are implemented as discrete trench VDMOS devices, and not integrated into a power IC. The devices are typically similar in size, the n-channel to achieve a low resistance, and the p-channel to be sufficiently large not to overheat operating as a constant current source, i.e., in saturation during pulsed operation. Moreover, to guarantee the switches and the squib are all operating correctly, a small test current is applied successively to each switch and to the squib checking for opens and shorts. If an SRS system failure is detected, the driver is immediately informed and (for legal and liability reasons), the data and time recorded inside the SRS system microcontroller.

C. Synchronous Rectification and DC/DC Conversion

Another major application for the trench power MOSFET is in dc/dc conversion. Pioneered in the late 1970s and early 1980s [43]–[45], power MOSFET-based PWM dc/dc converters employ a variety of converter *topologies* designed for stepping voltages up or down, regulating the output voltage against changes in load current and input voltage, and optionally galvanically isolating a load from incoming power. In operation, switching regulators comprise a main or "control switch" used to regulate energy flow from the converter's power input into an inductor, coupled inductor, or transformer, and an output "rectifier" used to convert the chopped voltage waveform back into dc and to provide a recirculation path for inductor current whenever the main switch is OFF. After rectification, the output is conditioned by a (*RC* or *RLC*) low-pass filter to remove ripple, enhance converter stability, and improve load transient response. Feedback continuously adjusts the switch on-times to perform PWM, regulating the output voltage to a target value using analog or digital control methods.

While at lower power levels the converter can be monolithically integrated, higher output power and isolated converters require discrete application specific power MOSFETs driven by a PWM control IC. In such a partitioning, trench VDMOS devices are often used both as the main "control" switch (especially from 20 to 200 V inputs) and for synchronous rectification, although designs differ substantially. As the main switch, the trench VDMOS is tailored not for the lowest specific ON-resistance, but for fast switching, low gate charge, low gate resistance, low feedback capacitance, and the lowest possible $R_{\text{DS}}Q_G$ FOM. As a synchronous rectifier, the trench VDMOS is customized for the lowest specific ON-resistance $R_{\text{DS}}A$ and sized to minimize conduction losses. Used as a replacement for Schottky rectifiers, trench VDMOS improves overall converter efficiency [46], [48], provided the device is designed to manage stored charge in quadrant III operation, minimize reverse recovery losses, and survive hard commutation (described later).

Converter topologies and control methods vary with voltage and power levels. Commercially, synchronous Buck and boost converters dominate nonisolated topologies, while isolated converters generally comprise forward, flyback, or full-bridge topologies depending on the power level required [49]. Lower voltage converters are typically hard switching, i.e., where the current in a PWM switch is interrupted at any time and where reverse recovery of the trench VDMOS intrinsic antiparallel diode is an important synchronous rectifier device design consideration. At higher voltages, soft-switching converters, such as resonant or quasi-resonant control methodologies, are also employed, synchronizing switching transitions according to time constants of the reactive components in the output filter. In such converters, trench VDMOS is used as the main control switch up to approximately 200 V (beyond which planar superjunction VDMOS predominate), but remain the preferred device technology for synchronous rectification.

The importance of various trench VDMOS design parameters is best exemplified in the context of dc/dc converter operation. The synchronous Buck converter shown in Fig. 11 comprises a half-bridge constituting an n-channel (or optionally a p-channel) trench VDMOS high-side switch (HSS) and a trench VDMOS n-channel low-side switch (LSS) operating as a synchronous rectifier (SR).

Aside from regulating voltage, the PWM control circuit also prevents shoot-through current in the two devices by insuring a BBM interval exists where both switches are biased OFF. During the BBM interval diode, recirculation current flows through the intrinsic antiparallel drain-to-body diode within the LSS trench VDMOS. During diode conduction,

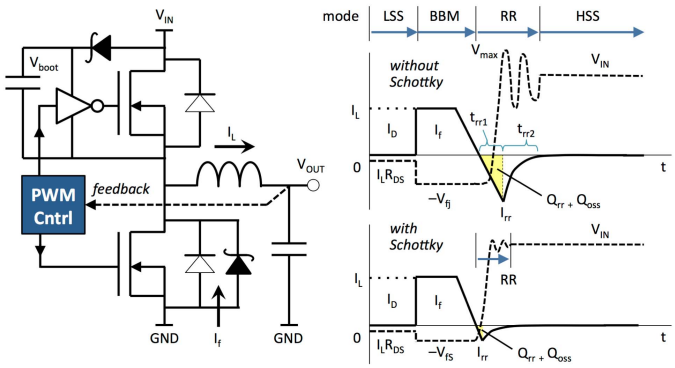

Fig. 11. Synchronous Buck converter circuit and operating waveforms shown with and without Schottky diode integrated into the synchronous rectifier.

TABLE II
SWITCH-MODE TRENCH VDMOS COMPONENTS OF POWER LOSS

Device	Conduction Loss P_{cond}	Gate Drive Loss P_G	C_{oss} Output Loss P_{Qoss}	Cross Over Loss P_{xo}	Diode RR Loss P_{rr}
General	$I_D^2 R_{DS(on)} D + P_{BBM}$	$Q_G V_G f$ $Q_G = Q_{GS} + Q_{GD}$	$\frac{1}{2} Q_{oss} V_{DS}$	$\frac{1}{2} I_D V_{DS} (t_r + t_f) f$ $t_r \approx t_f = Q_G / I_G$	$Q_{rr} V_{DS} f$
Buck HSS	$I_L^2 R_{DS(HSS)} \left(\frac{V_{out}}{V_{in}}\right)$	$(Q_{GS} + Q_{GD}) V_G f$	$\frac{1}{2} Q_{oss} V_{in}$	$I_D V_{in} Q_G / I_G$	0
Buck SR LSS	$I_L^2 R_{DS(LSS)} \left(1 - \frac{V_{out}}{V_{in}}\right) + I_L V_f t_{BBM} f$	$\approx Q_{GS} V_G f$	0*	0*	$Q_{rr} V_{in} f$

** total power loss may be shared between HSS and LSS* Row 1 describes any converter, Rows 2 & 3 are Buck specific

charge is stored in the trench device as injected minority carriers (diffusion capacitance) that must be removed during diode *reverse recovery* before the half-bridge is able to change states. As illustrated by the switching waveforms in Fig. 11, shunting the p-n diode current by a Schottky diode represents one method used to minimize the adverse impact of diode reverse recovery on power loss, switching speed, and EMI (discussed further in the next section).

Gate drive and gate resistance can also impact high-speed operation of a trench VDMOS. Low gate charge is important to reduce gate charging time needed to maximize the converter's duty factor range D_{max} to D_{min} especially in "low dropout" converters where $\Delta V = (V_{IN} - V_{OUT})$ is small. Moreover, trench VDMOS must be designed with adequate gate bussing or silicide to insure rapid state transitions. A low internal gate resistance guarantees all active cells turn on concurrently, otherwise additional "crossover" power loss P_{xo} (where high drain current and voltage temporarily coexist) will occur [50].

For reliable operation, it is necessary to balance the power losses in the control switch and in the synchronous rectifier so that the HSS and LSS trench VDMOS exhibit comparable power dissipation and heating. Power dissipation within a given device comprises conduction losses and switching losses. The relative magnitude of the $I^2 R_{DS}$ conduction losses for each switch depends on its resistance and its on-time t_{ON} as a percentage of the total period $T_{sw} = (t_{ON} + t_{OFF})$. For the HSS trench VDMOS in a Buck converter, the term $D = [t_{ON}/(t_{ON} + t_{OFF})]$ is referred to as the device's duty factor D and depends on the output to input voltage ratio, i.e., where $D = V_{OUT}/V_{IN}$. Since the LSS synchronous rectifier trench VDMOS is on when the HSS is OFF, then the LSS duty factor is equal to $(1 - D)$. In cases of large Buck voltage conversion ratios, i.e., where $D = V_{OUT}/V_{IN} \ll 100\%$, then to balance the losses across the high side and low side devices, the synchronous rectifier trench VDMOS should be bigger and ideally employ a lower specific on resistance technology. Using conduction loss as a first-order design parameter, the target area ratio of the LSS to HSS trench VDMOS given by (2) is approximately

$$A_{LSS}/A_{HSS} = ((V_{IN} - V_{OUT})/V_{OUT}) \times ([R_{DS}A]_{LSS}/[R_{DS}A]_{HSS}). \quad (2)$$

For example in a 5-to-1 V synchronous Buck converter using similar specific ON-resistance technology for both switches, the LSS should be approximately four times bigger than the high-side connected main switch. Packaging of totem pole n-channel trench DMOS into a single duel-die package for synchronous Buck converters therefore generally employs an asymmetric leadframe with the die pad for the low-side device three to six times larger than the high side device. If the HSS and LSS incorporate different process trench VDMOS technologies with dissimilar specific ON-resistances (e.g., if the HSS is a p-channel), the relative size ratio of the devices should be adjusted by (2) accordingly. Multifactor optimization of HSS and LSS device sizes must consider both conduction and switching losses, as well the full range of input and output voltages, not just the typical application condition [50], [51]–[54].

Power loss in a trench power MOSFET depends both on how it is constructed and how it is used. While power loss models vary, in general semiconductor power loss is given by

$$P = (P_{cond} + P_{BBM}) + (P_{gate} + P_{Qoss} + P_{xo} + P_{rr}) \quad (3)$$

where the first parenthetical term comprises current-dependent conduction losses and the second describes frequency dependent switching losses. The generic loss components summarized in the first row of Table II (in terms of V_{DS}, D, and so on) are restated specifically for the synchronous Buck converter's HSS and LSS devices (in terms of V_{IN}, V_{OUT}, and so on). The table highlights that the magnitude of various loss components is application specific. For example, device ON-resistance is a key design parameter for the synchronous rectifier trench VDMOS because in most Buck converters the synchronous rectifier (SR) conducts for the majority of the switching period T_{sw}, i.e., the duty factor of the control switch $D_{HSS} < 50\%$. Because the HSS changes states with the converter's full input voltage present across the device, i.e., $V_{DS(HSS)} = V_{IN}$, then minimizing its gate-to-drain overlap capacitance C_{GD} and Q_{GD} is critical.

In contrast, since the synchronous rectifier trench VDMOS switches with virtually no voltage across it, low feedback capacitance is not important for the synchronous rectifier. In a similar manner, the crossover switching loss term $\frac{1}{2} I_D V_{DS} t_{sw} f$ occurs primarily only on the HSS

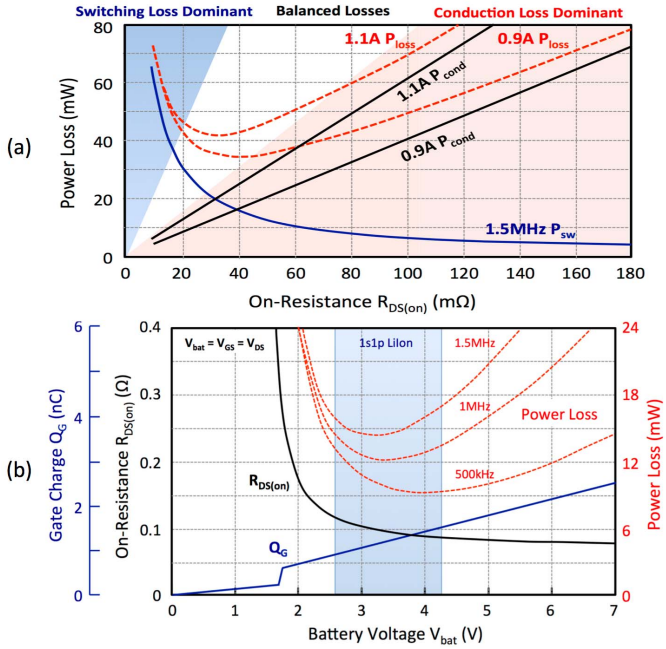

Fig. 12. Optimizing trench VDMOS for synchronous Buck converters efficiency. (a) ON-resistance dependence. (b) Input voltage dependence.

trench VDMOS. Diode recovery is also application specific. While the synchronous rectifier operates in quadrant III, the HSS does not. Diode reverse recovery is therefore important in the Buck synchronous-rectifier LSS trench VDMOS but not in the HSS.

Although losses associated with C_{DS} and Q_{oss} are ever present, their relative contribution increases in proportion to the input voltage. In the case of switch-mode operation of charge-balance [RESURF stepped oxide (RSO) or superjunction] trench VDMOS additional consideration of the nonlinear effects of C_{DS} is required [55]–[58]. Invariably, then, device selection and circuit optimization involves numerous application specific tradeoffs and compromises as illustrated in Fig. 12 for two completely different dc/dc converter designs.

As shown, the I^2R_{DS} conduction loss varies with the rms load current I and by per cycle *on-time* t_{ON} (as set by the converter's output to input voltage ratio). Switching losses are constant for a given operating condition (set by input and output voltages and switching frequency $f = 1/T_{sw}$). Fig. 12(a) illustrates lowering ON-resistance (using a larger trench VDMOS die) reduces conduction losses but increases capacitive switching losses, thereby improving high current efficiency by sacrificing switching losses. Conversely, small devices with high resistance suffer poor efficiency at high load currents but because of low capacitance exhibit reduced switching losses [50], [59].

Given a $[R_{DS}Q_G]$ FOM, equation(4) exemplifies the tradeoff between conduction and switching losses with ON-resistance $R_{DS(ON)}$

$$\begin{aligned} P_{loss} &= I^2 R_{DS(ON)} D + Q_G V_G f + Q_{oss} V_{DS} f \\ &= I^2 R_{DS(ON)} D + ([Q_G R_{DS}]/R_{DS(ON)}) V_G f + P_{other}. \end{aligned} \tag{4}$$

Since a converter operates over a range of voltages and currents, there is no one perfect size trench VDMOS for the entire range. To optimize average efficiency, assumptions must be made as to the user-profile as to what voltage and currents occur most frequently and matched to the technology that performs best under those conditions [60]–[64].

As shown in Fig. 12(b), another tradeoff occurs in Li–ion powered portable applications when the time varying battery voltage serves as both the converter's input voltage, i.e., $V_{bat} = V_{DS}$ and as its gate drive supply $V_{bat} = V_{GS}$. By swapping the ordinate and abscissa of the gate charge curve, the conduction and gate drive losses can be overlaid in the same graph as a function of the battery voltage V_{bat} [65], [66]. During each discharge cycle, the battery voltage declines from 4.2 to 2.7 V, whereby for a freshly charged battery, switching and gate drive losses predominate and conduction losses are low. Conversely, for a discharged battery, conduction losses dominate. To maximize battery life, device design should align the converter's minimum power loss condition to the nominal Li–ion battery voltage of 3.6 V to maximize per-charge use life.

D. Quadrant III Operation and Diode Reverse Recovery

Referring again to the switching waveforms of Fig. 11, during the interval that the low-side trench VDMOS is conducting, the inductor current recirculates through the LSS channel and the half-bridge output is driven below ground to a voltage $(-I_L R_{DS})$ as determined by the resistance of the ON-state synchronous rectifier. The LSS trench VDMOS operates in quadrant III, i.e., with $V_{DS} < 0$ and $I_D < 0$, in the same polarity as to forward bias the device's drain-to-body p-n junction. Before, however, the HSS can be turned back on, the LSS synchronous rectifier device must be momentarily turned off by the BBM circuit function, interrupting channel current and temporarily forcing diode conduction.

Without utilizing a Schottky rectifier, the voltage present across the OFF-state LSS during the BBM interval increases to approximately a voltage of -0.7 V, i.e., the forward biased drain-to-body junction voltage V_{fj}. p-n junction diode conduction during BBM causes two problems, namely: 1) it increases power dissipation in the device and 2) more significantly, it stores charge Q_{rr}, i.e., minority carriers, in the device's epitaxial drain that must be removed during the next HSS turn ON. When the high-side device turns ON, it must remove this charge before the voltage across the low-side trench VDMOS can change. This process, called diode *reverse recovery* shown in the upper waveform of Fig. 11, actually causes current to momentarily flow through the p-n diode in the wrong direction, i.e., negative current $(-I_{rr})$ with a peak negative value related to the overall inductance of the commutation loop.

The higher the reverse current peak, the higher the rate of voltage rise *dV/dt*, and thus the greater the turn-OFF voltage spike, will be. During this time, the reverse conducting diode behaves like a transient "dead short" across the input lowering converter efficiency. Ironically, even though the BBM interval is intended to prevent shoot-through in the two VDMOS from shorting out the input supply rail V_{IN}, because of diode

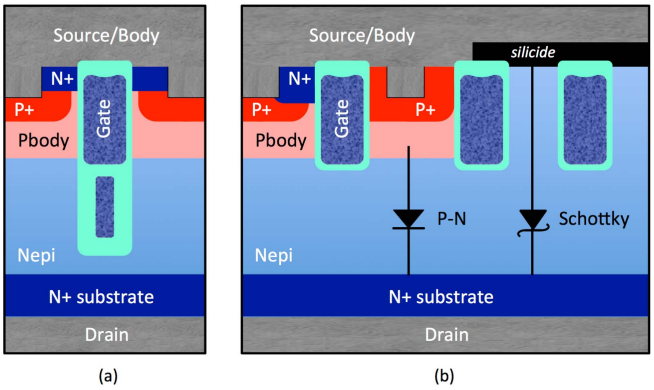

Fig. 13. Trench VDMOS for synchronous Buck converter. (a) HSS with low gate charge. (b) LSS synchronous rectifier with integrated Schottky diode. Anode connected trench gates shield the Schottky interface from electric fields.

recovery, the effect happens anyway in the HSS VDMOS's channel and the reverse conducting LSS diode.

Moreover, with a long reverse recovery time t_{rr}, the LSS voltage transient is undesirably delayed until well after the HSS is fully ON. As the stored holes are finally removed or recombine, the LSS suddenly experiences a high slew rate in its drain voltage leading to voltage overshoot to a voltage V_{max} greater than V_{IN} [67]. In addition to creating noise and electromagnetic interference, should V_{max} exceed the avalanche breakdown voltage $V_{(br)LSS}$ of the low-side trench VDMOS, the device may avalanche temporarily, conducting current from V_{IN} to ground and lowering converter efficiency. High *dV/dt* slew rates during diode recovery can also inadvertently trigger dynamic re-turn-ON of the synchronous rectifier channel by momentarily pulling the gate voltage above the threshold voltage due to the capacitive voltage divider of C_{GD} and C_{GS}.

In extreme cases, especially in poorly designed devices with inadequate source-body shorts, the displacement current from a rapid positive drain transient in the drain-to-body capacitor C_{DB} can induce a voltage drop in the p_{body} pinch resistance leading to forward biasing of the n+ to p_{body} junction, turn ON of the n-p-n parasitic BJT, and the potential for snapback breakdown. First categorized by Severns into four modes of *dV/dt* turn-ON [68], spurious turn-ON of trench VDMOS remains an important design consideration [69].

One means to avoid diode recovery induced high *dV/dt* is to limit the injected charge in quadrant III operation. Ideally, if an antiparallel Schottky diode is included in the circuit, the LSS drain voltage is clamped to the forward biased voltage V_{fS} of the Schottky diode (approximately −0.2 V) and as confirmed by switching waveforms, the problem with stored reverse recovery charge is largely ameliorated. In high-speed dc/dc conversion, however, using a *discrete* Schottky assembled in a separate package offers little performance benefit, because package lead inductance of the Schottky delays its conduction for an interval longer than the BBM period. As such, discrete Schottky clamps offer little or no improvement in the reverse recovery performance of high frequency dc/dc converters.

The solution to this problem as depicted in Fig. 13(b) is to utilize an application specific trench VDMOS with an integral

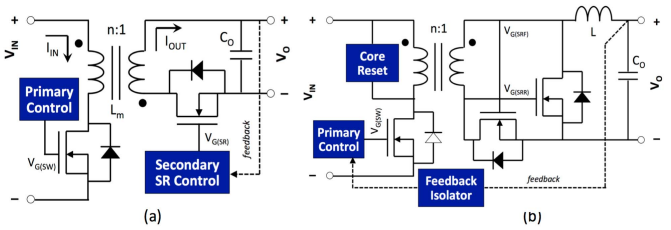

Fig. 14. Synchronous rectification in isolated dc/dc converters. (a) SR flyback converter. (b) SR forward converter. SR gate drive may comprise secondary side SR driver IC or direct drive with isolated feedback to primary.

Schottky diode formed within the device itself. Schottky integration is achieved using a refractory metal connected to the trench VDMOS source metal in contact with the n-type epitaxial drain material. Since the Schottky only carries current for a small fraction of the switching period, it does not require the same large area as a Schottky rated for continuous conduction. Using a smaller area, a lower barrier height metal can be employed to reduce Schottky forward voltage ($-V_{fS}$) without contributing significant I_{DSS} leakage to the device's OFF-state characteristics. Moreover, by incorporating anode-connected trench gates into the Schottky, during reverse bias, the interface is shielded from reverse biased-induced barrier lowering and diode leakage [70]–[72].

Because the LSS synchronous rectifier MOSFET conducts in quadrant III, switching between ON and OFF with low applied drain potentials less than 1 V (with essentially no Miller effect), the role of C_{GD} is less important in the Buck synchronous rectifier than it is in the control switch. Since most Buck converters operate with low duty factors, e.g., producing a 1 V output from a 12 V input where $D = 8\%$, then the synchronous rectifier spends the majority of the switching period conducting current. As such, specific ON-resistance is the primary factor in choosing the synchronous rectifier's technology and size. In contrast, the high-side connected control switch in a Buck converter does not exhibit diode conduction and has no need for the integrated Schottky. Instead, the HSS performs high speed switching with the full input voltage V_{IN} present across its drain-to-source terminals and is therefore adversely impacted by the Miller effect and feedback capacitance C_{GD}. Accordingly, the HSS implementation shown in Fig. 13(a) uses a low feedback capacitance method such as split-gate trench VDMOS, a RSO trench VDMOS, or a trench superjunction to improve synchronous Buck efficiency.

A similar optimization is required in isolated dc/dc converters shown in Fig. 14 including the synchronously rectified (SR) flyback converter [73], and the SR forward converter [74]–[76]. Because of stray inductance associated with the magnetics, the BBM interval in isolated converters is generally longer than in nonisolated supplies, exacerbating reverse recovery losses and increasing the magnitude of diode recovery voltage spikes.

E. W-Switched Trench VDMOS (Light Load Operation)

In dc/dc conversion, another consideration is "light load" operation, a condition that occurs when the load of a switching

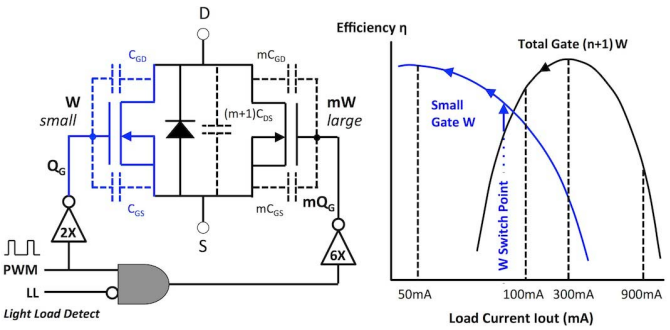

Fig. 15. PWM Light load operation of W-switched trench VDMOS.

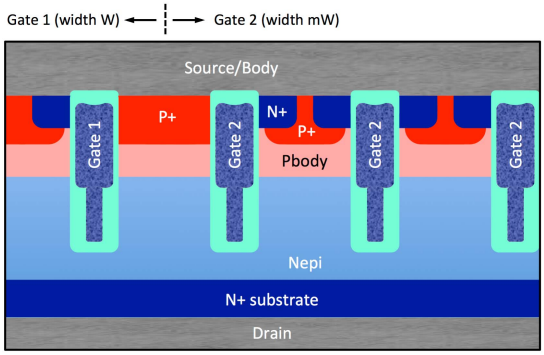

Fig. 16. Cross section of dual-gate W-switched trench VDMOS.

voltage regulator is drawing low currents. Because constant high speed switching consumes power, regulator efficiency in fixed frequency PWM operation declines rapidly with decreasing load current. Several methods are required to combat this effect. First, to prevent oscillations in the output filter, the synchronous rectifier is switched OFF in light load. Since conduction loss is minimal with low currents, p-n diode conduction and reverse recovery losses are negligible.

Second, the converter can be operated in variable frequency, pulse skipping, hysteretic, or burst mode. In burst mode for example, in a manner similar to a thermostat's operation, the regulator momentarily stops switching till the output voltage sags then it turns back on to recharge the capacitor to a specified voltage, shutting OFF again. The cycle repeats so long that the light load condition persists. Although improving light load efficiency, such hysteric mode operations suffer several disadvantages including: 1) poor step load regulation; 2) wide spectrum conducted and radiated noise; 3) unpredictable converter bandwidth; and 4) a large output ripple. Given these disadvantages, burst or hysteric mode operation should be invoked only at the lowest load currents.

An attractive alternative is to employ W-switching, a method where at intermediate currents the *size* of a converter's main switch is dynamically reduced during operation by charging the size of the transistor being switched in PWM operation, i.e., keeping only a small portion of the transistor switching. As shown in the equivalent schematic of Fig. 15, a W-switched trench VDMOS comprises a transistor divided into two parallel devices with separate gate connections [78]–[80]. The smaller device used in light load has a gate width W and corresponding gate charge Q_G. The larger device, used in normal operation, has a much larger gate width m•W and a higher corresponding gate charge mQ_G (where $m = 3$ to 30 depending on the converter's requirement).

In normal operation, both devices are switched by the PWM input signal at full frequency requiring a total gate charge $(m+1)Q_G$. Upon detecting a light load condition [81], the signal LL (connected to an inverting input of an AND gate) goes high disabling switching of the larger device, and the effective gate charge becomes Q_G, roughly m times smaller reducing switching losses and improving converter efficiency without changing the its operating frequency, converter bandwidth, or transient and step-load regulation capability. Unlike variable frequency methods, the device size can be W-switched rapidly, within a single PWM pulse period. The W-switch may be realized using any type of trench VDMOS, including field plate, split gate, RSO, and superjunction type devices. As shown in Fig. 16, the device utilizes two separate gate connections and therefore requires not one, but two gate pads for wire bonding.

It should be noted, although W-switching dramatically reduces gate charge by m times, the drain-to-source capacitance remains the same as the full size device, i.e., at $(m+1)C_{DS}$, reducing its utility in higher voltage regulators.

F. Pseudo-Schottky Effect in Quadrant III Operation

The Schottky trench VDMOS while able to reduce reverse recovery losses in synchronous converters is disadvantaged by higher manufacturing costs and increased OFF-state leakages. An alternate method to limit charge storage in a trench power MOSFET can be achieved through application specific design and fabrication methods to invoke, i.e., exaggerate, physical mechanisms uniquely present in quadrant III operation. These methods *temporarily* lower threshold voltage electrically, thereby enhancing channel conduction during BBM operation. Rather than forming a channel by driving the trench VDMOS gate with a precisely timed separate gate signal, a channel inversion layer is formed by electrically lowering the device's threshold using an enhanced *body effect*. In this manner, channel conduction can shunt junction current despite having less than 0.6 V to bias and operate the device.

Although it is well known that the body effect describes an increase in threshold voltage when a MOSFET's source-to body junction is reverse biased, it is often overlooked that slightly forward biasing the junction (but not enough to cause diode current to flow) has the opposite effect, causing V_t to decrease whenever $V_{SB} < 0$. The effect is described in a MOSFET's threshold voltage

$$V_t = V_{t0} + \gamma\left[\sqrt{|V_{SB} + \Psi_B|} - \sqrt{\Psi_B}\right] \tag{5}$$

where V_{t0} is the device's threshold without an applied source-to-body bias (i.e., $V_{SB} = 0$) and where ψ_B is the bulk potential, generally approximated as twice the Fermi potential, i.e., $\psi_B \approx 2\phi_f$ (although this is not precisely correct for moderate inversion). For cases where $V_{SB} = 0$, the two square root terms cancel and $V_t = V_{t0}$. Whenever $V_{SB} < 0$, however, the first radical in (5) becomes smaller than the second, and the

threshold is reduced, causing $V_t < V_{t0}$ and inducing majority carrier channel current. The magnitude of the effect, limited to the voltage range $0 > V_{SB} > -0.6$ V by the source-to-body junction, is a function of the process related parameter Υ given by gamma body effect equation

$$\gamma = \sqrt{2q\epsilon_{si}N_B}\left(\frac{x_{ox}}{\epsilon_{ox}}\right). \quad (6)$$

The magnitude of Υ depends on the channel doping concentration N_B and on the gate oxide thickness x_{ox}. Although thicker gate oxides and higher body doping increases Υ and correspondingly amplifies the body effect in quadrant III, it also increases a device's threshold V_{t0}. In order to compensate for higher threshold voltage, the channel can be implanted with a shallow threshold adjusting implant, which in the case of a trench VDMOS requires the use of a tilt implant into the trench sidewall. Of the two process variables affecting Υ, thicker gate oxides reduce transconductance. Increasing N_B to optimize the device is therefore preferable to modifying the oxide thickness.

The net benefit of this method results in a device with a normal threshold but with a significantly enhanced Υ factor, i.e., a greater threshold dependence on body bias. In operation, the lower threshold occurs electrically only during BBM (quadrant III) operation and therefore does not increase OFF -state leakage when the synchronous rectifier is OFF and supporting a voltage, i.e., when $V_{SB} = 0$ and $V_{DS} > 0$. Because the threshold is low only during the ON state, the modified trench VDMOS exhibits the conductance of a low threshold device (when it is on) and exhibits the low leakage of a high threshold device (when it is OFF). Low threshold devices, by comparison, exhibit high leakage in their OFF state. Although it is possible to control the body effect by actively driving the source to body junction by a separate bias supply [82], [83], in conventional switching converter operation during the BBM interval, the gate of the synchronous rectifier is electrically shorted to its source i.e., where $V_G = V_S = V_B$. During BBM, energy stored the inductor drives the drain potential V_D of the n-channel trench VDMOS negative with respect to its source V_S in the polarity that forward biases the p-n body diode.

Operating in quadrant III with its drain at the most negative potential, drain terminal D functions electrically as source S′ (and conversely source terminal S functions electrically as drain D′) whereby $V_{GS'} > 0$ induces weak inversion and $V_{S'B} < 0$ lowers the source-to-body junction barrier increasing the carrier density in the channel. The resulting two-terminal device [84] conducts not through p-n junction current but by channel conduction, exhibiting an I–V characteristic similar to that of a Schottky diode. As shown in the center curve of Fig. 17(a), the ON-state "pseudo-Schottky" voltage is substantially lower than the threshold voltage of the same trench VDMOS biased in quadrant I and lower than the forward voltage drop on a p-n junction at comparable current densities. Based on barrier lowering, the majority carrier channel conduction characteristic slope is very similar to a real Schottky (shown for comparison). In its OFF state, however, the pseudo-Schottky exhibits significantly lower leakage current than the Schottky.

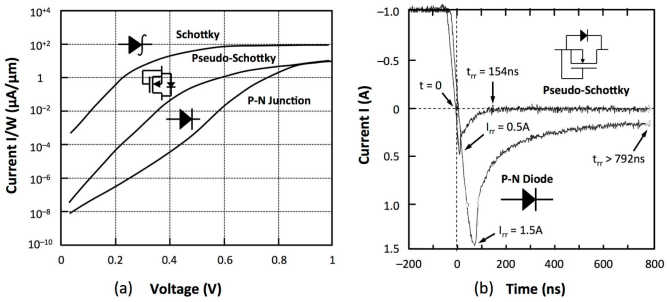

Fig. 17. Pseudo-Schottky trench VDMOS operation in quadrant III. (a) Comparison of conduction characteristics to Schottky and junction diodes. (b) Reverse recovery compared to p-n junction diode.

In the comparison to a conventional device shown in Fig. 17(b), the impact of the enhanced pseudo-Schottky effect in trench VDMOS offers a significant reduction in reverse recovery charge Q_{rr}, recovery current I_{rr}, and time t_{rr}. Various optimization strategies have been reported [85] controlling threshold, oxide thickness, and doping. Care must be employed when employing extreme gate thinning or V_{t0} reduction as they may adversely impact device OFF state leakage and breakdown.

G. ABS Solenoid Driver

In the automotive application for ABS, electronically controlled solenoid valves are opened or closed to control brake fluid pressure, slowing or stopping the vehicle in response to a driver's actions. In the case of emergency braking, however, the ABS module takes control, automatically pumping the brakes at a rapid rate, typically at tens of hertz, to prevent skidding during rapid stopping. Because of the slow response time of electromechanical valves, the automatic pumping of brakes requires solenoid valves to be rapidly and repeatedly magnetized and demagnetized, requiring high current switch mode control using low resistance trench VDMOS. To survive voltage transients normally present in automotive electrical systems (e.g., load dump), the devices must be rated at 50–80 V despite the fact that the nominal battery voltage in automobiles is only 12 V.

While channel conduction is employed to magnetize the solenoid, various studies have revealed the fastest way to remove energy from a magnetized solenoid is achieved, not by diverting current in a shunt transistor, but by avalanching a p-n junction. As such, the preferred switch-load topology for an ABS drive system today employs a single LSS comprising an n-channel trench VDMOS driving a battery connected solenoid. In operation, the LSS is turned on letting the inductor current ramp to a prescribed level then the device is switched OFF. Immediately the solenoid's inductance drives the trench VDMOS into avalanche breakdown forcing the device to survive full current while in avalanche. The ABS operating condition is identical to the unclamped inductive switching (UIS) test used to evaluate MOSFET ruggedness (see UIS section IV-A of this paper).

The exclusive use of *ruggedized* trench VDMOS devices [86], [87] is therefore a critical requirement for realizing a reliable ABS system. Such ruggedized devices should operate

free of any parasitic bipolar snapback, even during high current avalanche. Absent parasitic electrical failure mechanisms, the limiting failure mechanism is thermal. Accordingly, the die size is not set by ON-resistance or cell density, but by transient thermal power dissipation.

H. Motor Drive

Low-voltage motor drives represent a wide application area for trench power MOSFETs. The devices are used in forklifts, power tools, mining vehicles, or light electric vehicles including battery driven vehicles at airports, Segway transport, motorized skateboards, power wheelchairs, or electric scooters. Common motor driver topologies include half-bridge, H-bridge, and three-phase bridge configurations, with each winding connected to a push–pull driver comprising two totem pole connected n-channel trench VDMOS. Depending on the electronic commutation driving sequence employed, electrical stresses placed on trench VDMOS (and their intrinsic antiparallel diodes) vary. Theses stresses can be considered in three categories [88]. In some drive commutation schemes, diode conduction is allowed to decay naturally or is shunted by a synchronous rectifier so that high dV/dt is prevented by the inductive time constant of the motor. Alternatively in hard commutation drives commonly employed at moderate frequencies (switching up to hundreds of kilohertz), forced diode reverse recovery between the recovering diode and the series connected trench VDMOS within the same half-bridge can produce high dV/dt transitions and EMI. Voltage overshoot and avalanche in such drives may also occur on a repetitive basis.

As many motor control applications (such as power tools or small vehicles) are also battery-powered, battery life and driver efficiency is also a key factor. To minimize conduction losses, often trench VDMOS are configured in parallel to achieve high currents and extremely low resistances where packaging and low thermal resistance are important design considerations. Matching device thresholds while minimizing Q_{GD} and Q_{rr} are important factors in balancing power losses across parallel devices while improving reliability, limiting voltage overshoot, reducing noise, and avoiding the need for snubber circuits. During short circuit and stuck rotor fault conditions the devices must survive high currents and possibly avalanche (during fault recovery). Like in solenoid drivers, trench VDMOS ruggedness is key in achieving reliable motor drive operation.

IV. Reliability Considerations

As described in the previous section, the important reliability considerations for the trench power MOSFET depend not only on its fabrication but also in its application including single pulse and repetitive avalanche, hard commutation ruggedness, and forward bias safe operating area (FB-SOA) involving linear circuit mode operation.

A. Single Pulse Avalanche (UIS)

In power electronic circuits, prudent component selection, i.e., using power devices with breakdown voltage ratings higher than the input supply, can avoid operating a power device in breakdown. But in circuits driving inductive loads, voltages may be generated outside the supply range and exceeding a device's voltage ratings. Specifically, whenever current flowing in an inductor is interrupted, the inductor generates a counter opposing electromotive force to combat the change. The magnitude of the inductor's reaction is proportional to the rate of change of current, i.e., $V_L = LdI_L/dt$. If this change occurs from an ON–OFF "switching" operation (i.e., with a high dI_L/dt) then unless it is otherwise clamped, the inductor's generated voltage will most certainly exceed the supply rails.

The impact of the inductor's voltage spike depends on the switch load topology used. Specifically for the "LSS" switch-load topology comprising a single grounded power switch driving an inductor, there is nothing to limit the inductor's voltage other than the device itself. In the event, the LSS is a trench VDMOS, the inductive spike will cause avalanche breakdown of the device's antiparallel drain-to-source diode, the p-n junction diode formed by the n-type drain and p-type body. During switching, turning OFF the LSS unavoidably forces the body diode into breakdown to absorb the energy within the inductor, a condition known as UIS. Even in cases such as a half bridge topology where an inductor appears schematically to be diode clamped, high voltage may still momentarily occur across the device because of stray inductance. Examples include motor commutation, diode reverse recovery (shown previously in Fig. 11), and during the automotive "load dump" condition. Accordingly, for applications involving inductive loads, a power device's *avalanche ruggedness*, its ability to operate in avalanche without self-destruction, is an important reliability device parameter.

During a single UIS event, there are two main mechanisms competing to destroy a device [89]. The first mechanism is related to energy absorption and the transient heat-dissipation capability of the device and thus is referred to as *energy-related destruct*ion. A typical example is shown in Fig. 18(a). Because inductor current cannot change instantaneously, in order to maintain current continuity upon gate turn OFF, the inductor voltage rapidly rises driving the device into avalanche breakdown. Provided the device survives the initial switching transient, the inductor current then ramps down as the trench VDMOS absorbs energy from the inductor.

Due to the simultaneous presence of a high electric field and a high current density, the silicon device's lattice temperature increases rapidly, heat being generated locally at a rate too fast to thermally diffuse. As shown, the breakdown voltage V_{br} rises due to increased carrier-phonon interaction caused by the increase in temperature, i.e., V_{br} exhibits a positive temperature coefficient of voltage, which (like a positive temperature coefficient of resistance) supports homogenous current distribution. In operation, any local hot spot will conduct less diverting current to its surroundings thereby preventing the formation of current filaments. As long that current persists in the inductor, energy transfer from the inductor's magnetic field into electric current will continue, the silicon temperature rising until it approaches the so-called

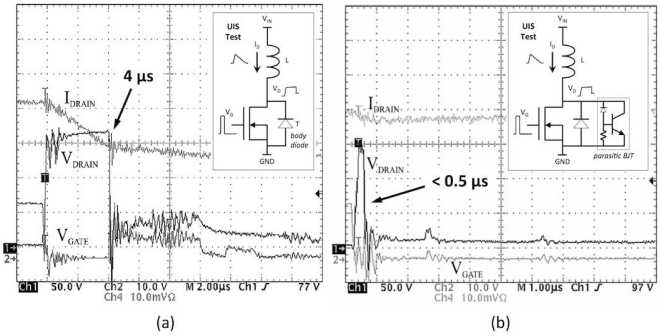

Fig. 18. UIS operation of a trench VDMOS. (a) Energy-related failure. (b) Current-related failure. Energy related failure is thermal, while the faster current related failure is electrical resulting from n-p-n parasitic BJT turn ON.

intrinsic temperature T_{int}. The intrinsic temperature is defined as the temperature at which the intrinsic carrier concentration $n_i(T)$ equals the background doping value N_D. An empirical relation for T_{int} [90] is given (in iterative form) in (7)

$$n_i(T_{\text{int}}) = (3.88 \cdot 10^{16}\ \text{cm}^3) T_{\text{int}}^{3/2} \exp\left(\frac{700°\text{K}}{T_{\text{int}}}\right) \equiv N_D. \quad (7)$$

At the intrinsic temperature, thermally generated carriers exceed extrinsic dopant concentrations and the device begins to behave as an intrinsic semiconductor material with conduction properties entirely governed by temperature and not by doping. At this point, the devices become unable to absorb or dissipate more energy. If current continues to flow, the device will be destroyed due to excessive temperature leading to melting of the silicon crystal or from failure of metal contacts. Equation (7), while providing a guideline for the intrinsic temperature T_{int}, is only an estimate. The actual intrinsic temperature is technology specific and should be confirmed empirically by measuring the avalanche destruction current I_{aval} at different temperatures and for various inductances. By numerically extrapolating a plot of I_{aval} versus T for several inductances, the intersection of these lines cross the abscissa at one point defining the intrinsic temperature T_{int} of the particular technology.

In a study comparing a 100 V charge compensation (superjunction) field plate trench VDMOS to conventional planar VDMOS, the trench devices exhibited a T_{int} of 480 °C, while the planar devices exhibited a T_{int} of only 380 °C. In accordance with (7), the measurement confirms the higher doping of the superjunction device's epitaxial layer. In operation, the higher intrinsic temperature means that an SJ or RSO trench VDMOS can absorb greater avalanche energies without damage. As the failure mechanism is related to the thermal properties of extrinsic silicon, the measured population of avalanche current density $I_{\text{aval}}/A = J_{\text{aval}}$ is tightly distributed statistically, with the avalanche current J_{aval} decreasing with increasing inductance (i.e., higher energy densities limit the maximum avalanche current).

The second mechanism causing device destruction during UIS is called *current-related destruction*. Unlike energy-related destruction requiring time for a temperature rise to occur, current-related destruction occurs nearly instantaneously at the moment of switching (when the inductor current and *dV/dt* is greatest). In well-designed power MOSFETs, current-related destruction typically occurs at high currents. In poorly designed VDMOS with inadequate body contact, however, it can also occur at unacceptably low currents. The origin of current-related destruction is electrical, involving turn-ON of the parasitic n-p-n bipolar formed by the n+ source, p_{body}, and n_{epi} drain. During UIS avalanche, holes generated by impact ionization combine with capacitive displacement current flowing through the VDMOS p_{body} region. As majority carriers, these holes create a voltage drop in the base of the device's parasitic n-p-n BJT, the magnitude of the drop further exacerbated by the high pinch resistance of modern short channel VDMOS.

If this potential drop exceeds the built-in potential of the base-emitter diode, the parasitic BJT will turn ON and begin to inject minority carriers (electrons) into the parasitic BJT's base. Since the BJT exhibits a positive temperature coefficient of current, the higher current density induces local heating generating additional minority carrier injection spontaneously forming a localized hot spot leading to destructive thermal runaway. Concurrently, local heating increases parasitic base resistance so that the metal source-body short of the surface contact no longer biases the intrinsic (pinched) base region. As such, the intrinsic base begins to acts as an open circuit and the BJT's breakdown suddenly collapses from its $V_{(\text{br})\text{DSS}} = V_{\text{CES}}$ value to a much lower V_{CEO} voltage, a value dependent on the beta of the parasitic bipolar (which is also rising from the elevated temperatures). The resulting sudden drop in avalanche voltage, commonly referred to in BJT vernacular as *bipolar snapback*, generally is an irreversible step toward current filamentation, excessive current densities, and inevitable device destruction. The collapse in blocking capability is also referred to as fold-back, latch-back, or latch-up (not to be confused with the term latch-up used to mean triggering a p-n-p-n thyristor into its latched ON state).

Fig. 18(b) gives an example of the current-related destruction of a device. The short survival time ($\ll 1\ \mu$s) and rapid device destruction indicates a different mode than energy-related destruction. In sharp contrast to energy-related UIS failures, current-related UIS failures exhibit a broad statistical distribution in avalanche failure currents I_{aval} and do not exhibit a monotonic dependence on energy or inductor value. Mechanistically, this variability is explained by small doping variations in p-type body doping affecting pinch resistance, by variability in body contact resistance, and even by bond wire placement affecting 2-D transient currents at the onset of UIS avalanche.

Under normal use, the state-of-the-art trench power-MOSFETs today are well designed and rarely impacted by parasitic BJT turn-ON. As cell densities increase and specific ON-resistance is continuously reduced, current densities are constantly increasing. This trend represents a challenge for future trench VDMOS designs to manage current related UIS failures, as the body doping concentrations usually cannot be increased commensurate with the higher current densities. Consequently, a precise control of technological parameters is required to provide a low-resistive path for the avalanche

current through the body region without affecting the threshold voltage value and its tolerance range. Once method facilitating greater precision control of body doping profiles is the use of an all ion implanted VDMOS not relying on double diffusion but instead utilizing high-energy ion implantation (HEI) to form the "as-implanted" final body doping profile [91], [92] using a succession of implants of varying energies (i.e., body engineering).

Continuing reduction in specific ON-resistance, wafer thinning, and die size reductions also presents a challenge for avoiding UIS energy-rated failures in future designs. Smaller volume devices heated up faster, meaning less energy is needed to reach the intrinsic temperature limit of the device. As described previously charge-compensation devices increase doping concentrations, increasing the intrinsic temperature, but this method appears limited in how much farther it can be extended. Other methods to increase energy capability must be devised. For example one method could be the increase of the front-side metallization layer thickness using the metallization layer acts as a heatsink [93]. Using a 20-μm copper layer the temperature rise for single pulses in the 10-μs range can be reduced by 50% at a given power density [94].

B. Repetitive Avalanche

Avalanche events may also occur repetitively. In contrast to single-pulse avalanche operation, which is well understood, easily characterized and tested, the repetitive avalanche operation of trench VDMOS is a difficult and complex topic. Conditions vary greatly and no standardized tests for repetitive avalanche capability are agreed upon [95] especially in regard to dissipated energy per cycle. Depending on the application, repetitive avalanche may occur exclusively as a result of a system failure or may occur in every switching cycle, e.g., in dc/dc converters operating in soft avalanche. Categorization of failures into two modes may be insightful, including the following.

1) Parametric drift of leakage currents, threshold voltage, and output capacitance resulting from repetitive UIS induced cumulative hot carrier damage
2) Material degradation, particularly metallization and ohmic contact changes, resulting from repetitive UIS induced temperature cycling, indirectly affecting electrical parameters (such as ON-resistance).

In the case of hot-carrier parametric drift, repetitive avalanche events are often caused by small yet unavoidable parasitic inductances in power loops, e.g., bond wires, package leads, and even PCB traces. These events can occur at each switching cycle. As the parasitic inductances are small, their impact is greatest in fast-switching applications where high dI/dt is present, for example in synchronous rectification stages of power supplies. The high number of repeated avalanche cycles, even dissipating low energies in the range of 1 μJ or less only, gradually impact device behavior, especially in trench VDMOS not engineered for avalanche operation.

In one study [96], a commercially available 750-W, 12-V server power supply unit (PSU) with secondary-side synchronous rectification was used to perform a repetitive UIS investigation. The topology of this PSU is a phase-shift, full-bridge rectifier on the primary side [97] with hard-switched, center-tapped synchronous rectification stage on the secondary side. To monitor potential changes in the device characteristics during the test, efficiency and voltage overshoots in the synchronous rectification stage were monitored. The device under test comprised a 2 mΩ 60 V charge-balanced (RSO) field-plate trench VDMOS. After a harsh repetitive avalanche stress test comprising $I_{\text{aval}} = 46$ A, $E_{\text{aval}} = 240$ μJ, $f = 80$ kHz, and $T_a = 55$ °C, measured changes in efficiency were found to be very low (less than 0.2% change) indicating the hot carrier robustness of the state-of-the-art trench VDMOS is quite good. New generations of trench VDMOS must however, be re-evaluated case-by-case.

Applications where material degradation from repetitive UIS is more likely involve high energy per cycle pulses intentionally used to achieve fast demagnetization in solenoids or electromagnets. Examples include solenoid valve drivers for gasoline and diesel injection valves and ABS systems during antiskid braking. Other examples include UIS spikes arising from large stray inductances from cabling, wire harnesses, or high current PCB layouts, especially in motor drive and in automotive applications. In actual applications, the high energy contained in each UIS pulse is dissipated by the trench VDMOS at regular intervals, momentarily heating up the device and allowing it to cool before repeating the pulse again. In the event, the device's temperature rise during successive UIS pulses does not return to the same baseline temperature, because it is unable to conduct away the heat in time, and then, the average temperature of the device will gradually rise over repeated pulse cycles and eventually, unless operation is interrupted, the power MOSFET will be destroyed. Temperature rise from residual heat is a thermal problem arising from an inability to dissipate heat fast enough, often because of a high ambient temperature (e.g., an overheating engine block) or because of increased thermal resistance resulting from a degraded thermal interface. Using an over-temperature shut down circuit, system failures from such cumulative heating effects can be prevented by temporarily suspending operation until the cause is eliminated or the ambient temperature returns to normal.

In the event repeated high-energy UIS pulses do not cause a cumulative heating failure, the device will operate normally until material degradation occurs. Similar to power-cycling and thermal-cycling tests performed in burn-in, such failures generally involve a top metallization fatigue failures [98], [99] or degradation of the interface between the top metal and bond wires or in contact windows between the metal and the underlying barrier metal and silicon. Such morphological changes have been confirmed in the standard power aluminum metallization of trench VDMOS. For example, in the focused ion beam cross section shown Fig. 19(a), repeated power cycling using 150 K temperature excursions reveals aluminum–copper metallization exhibits electrical failures and corresponding severe plastic deformation of the power metal after only 3 million pulses. In contrast the device using copper-based power metallization shown in Fig. 19(b) does not show any visible deformation even after 150 million pulses.

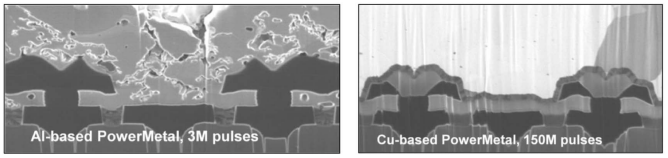

Fig. 19. Cross section of trench VDMOS top metal after $\Delta T = 150$ K power cycling. (a) Al top metal after 3M pulses. (b) Cu top metal after 150M pulses.

In conclusion, depending on the nature of the repetitive avalanche events, different trench power MOSFET devices must be chosen as device design and fabrication methods have a significant impact on the repetitive avalanche robustness [98]. When selecting a MOSFET for a repetitive avalanche survival, it should first be determined whether UIS is an infrequent event (like load dump, short circuit) resulting from a system failure or irregular operation, or is it a normal operating condition of the application (like switching an inductive load). In the former case, the number of avalanche pulses is typically limited to a few thousand UIS pulses, whereas in the latter case, the number can be much larger depending on the expected use-life of the product or power system.

C. Hard Commutation and Forced Diode Recovery Ruggedness

In push–pull and other dual-switch topologies driving inductors, operation may involve forward biasing the drain-to-body p-n junction of the trench VDMOS. This condition floods the epitaxial drain of the device with minority carriers. Depending on gate drive waveforms of the two devices, in high speed applications like synchronous dc/dc converters or in fault conditions (like short circuit protection), one of the devices may intentionally turn-ON commencing channel conduction *before* the injected minority carriers stored in the other device have had time to recombine. As a result, the minority carriers are forcibly extracted from the conducting diode, expediting diode recovery and turn-OFF. The process whereby the body diode is subjected to fast transition from diode conduction into its blocking state is referred to as *forced diode recovery* or as *hard commutation*.

Forced diode recovery occurs normally in switching operation of synchronous dc/dc converters such as the synchronous Buck converter (see waveforms of Fig. 11). In motor drive, however, hard commutation does not normally appear under regular operating conditions but in critical operating conditions such as a short-circuit event or emergency braking. In such cases, because of the presence of stray inductances and high dI_L/dt slew rates, the resulting inductive electromotive force can drive the OFF state device into breakdown.

The origin of device damage during forced diode recovery originates from inhomogeneity in the charge extraction process. As the conducting diode turns off and its current reverses polarity and direction, the expanding depletion region located directly beneath the P-type body regions extracts holes below and adjacent to the junction. Minority carriers (holes) injected into the high-voltage edge termination, however, remain too distant from the nearest junction to be forcibly extracted, and must diffuse or recombine. As the depleted space charge expands, voltage appears across the recovering device despite continuing current flow emanating from stored charge in the termination area. The simultaneous presence of high voltage and diode recovery current in the termination contributes to intense localized heating and localized avalanche leading to device destruction.

To improve the dynamic blocking capability of the trench VDMOS, design measures to reduce carrier injection into the edge termination and improve its extraction or alternatively to utilize carrier lifetime control methods. One study [100] subjected a 12-mΩ, 80 V trench VDMOS to high slew rates of $dI/dt = 1900$ A/μs using stepwise increases in current till device failures were observed. Using the foregoing techniques, the measured controllable commutation current increased from 125 to over 200 A with a significant statistical improvement in the observed population distribution variance. Alternatively, application specific trench VDMOS with integrated Schottky or pseudo-Schottky can be used to reduce the magnitude of injected minority carriers.

D. Forward Bias Safe Operating Area

Another application of trench VDMOS is to operate them, not as switches, but as controlled current sources in their *saturation* region of operation, i.e., with drain current and drain voltage simultaneously present in the device. Circuit methods used to bias and controllably operate a power MOSFET in its saturation region of operation are commonly referred to as "linear" circuits or linear mode (a term not to be confused with a MOSFET's linear operating region), because feedback is required to control current or voltage gain, especially in devices with large gate widths and correspondingly high transconductance. The product of conduction current and simultaneously sustained voltage results in power dissipation $P = I_D V_{\mathrm{DS}}$ that in any case cannot exceed the maximum safe junction temperature $T_{j\,\max}$ of the device for a given ambient temperature T_a and a package junction-to-ambient thermal resistance θ_{ja} as given by

$$T_j = T_a + \theta_{ja}(I_D V_{\mathrm{DS}}) < T_{j\,\max}. \tag{8}$$

Typically represented on a graph of current versus voltage (I–V graph), the resulting thermal safe operating area (SOA) of a trench VDMOS is rectangular bound by $I_{D(\max)}$ on the ordinate axis, by $V_{(\mathrm{br})\mathrm{DSS}}$ on the abscissa, and "clipped" by $T_{j\,\max}$ on the upper right hand corner where the product or high current and voltage product an unsafe amount of heat. This safe operating area for a conducting device is sometimes referred to as the FB-SOA to contrast it to the reverse biased safe operating area for OFF devices. The term FB does not, however, refer to the forward bias of a p-n junction but only to denote ON-state conduction.

While this the FB-SOA defines a thermal boundary for safe operation, it does not tell the whole story in regards to reliably operating in the linear circuit mode. First, hot

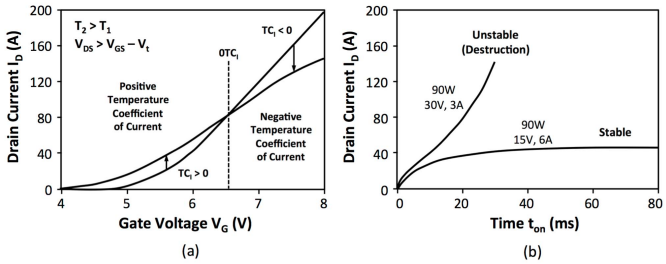

Fig. 20. Thermal stability of trench VDMOS in linear circuit mode operation. (a) Temperature effect on saturation current. (b) Stable and unstable operation.

carrier generation near the trench gate can shorten the reliable use life of trench VDMOS by charging, shifting threshold voltage, degrading transconductance, and even rupturing the gate dielectric. Gate drain engineering can be employed to minimize hot carrier effects by misaligning the location of peak electric fields away from high current density regions in the epitaxial drain (see example in Fig. 9).

Another phenomenon affecting FB-SOA device reliability involves a power MOSFET's gate voltage and the impact of gate bias on device thermal stability. Because of its widely recognized advantage of a negative temperature coefficient of current (i.e., where hot spots conduct less current automatically diverting the current elsewhere), the power MOSFET is often promoted as a device free from thermal runaway and current filamentation, a distinguishing advantage of unipolar device conduction over bipolar conduction devices (such as the BJT and the GTO). This belief, however, is not entirely true when using a operating a power MOSFET in saturation.

As shown in Fig. 20(a), when biased in saturation in the so-called "threshold" connection, i.e., with $V_{GS} = V_{DS}$, the transfer characteristics for a MOSFET measured at two temperatures reveal three operating regions. The intersection of the two curves represents a zero temperature coefficient (0TC) point—the gate bias where the impact of a decrease in threshold voltage with increasing temperature (as described by the expression $V_{GS} = V_{t0} + \Delta T(dV_t/dT)$) precisely cancels a decline in channel carrier mobility μ (T). For gate biases above the 0TC point, the effect of dV_t/dt is too small to offset the impact of increased carrier scattering and declining mobility μ (T), so the device exhibits a negative temperature coefficient of current.

Since switch operation always involves a large gate voltage, all power MOSFETs operated as switches exhibit a negative temperature coefficient of current and an associated thermal stability. If, however, the gate bias is below the 0TC point, then the decline in threshold voltage with increasing temperature is significant, resulting in an increase in gate drive not cancelled by the declining mobility, and device current increases with temperature (i.e., a positive temperature coefficient of current).

A positive temperature coefficient of current means inhomogeneous conduction in a portion of the trench VDMOS causes a local increase in heat generation. If the transient thermal resistance is too great to immediately disperse the heat, a hot spot will form and grow in magnitude, the resulting thermal instability leading to current filamentation, localized thermal-runaway, and ultimately device destruction [101]. Whether the device is stable or destroyed depends entirely on the bias conditions, i.e., the drain voltage, the drain current, and the duration, the condition exists, not simply on the average power. For example, as shown in Fig. 20(b), a 900-W pulse power application realized as 6 A with $V_{DS} = 15$ V is stable but at 30 V and 3 A the device goes into destructive thermal runaway. Using the temperature coefficient of current $\alpha_T = \Delta I_D/\Delta T$ as an electrical indicator of transient thermal resistance, a method to distinguish regions of instability from unconditionally stable operation was reported [102], [103]. At higher cell densities and greater channel widths, thermal resistance increases and the safe operating region for linear circuit mode is reduced [104] whereby even relatively short durations of current saturation during start-up or shutdown may lead to device failure.

V. Trench Lateral DMOS and Integration

Lateral DMOS (LDMOS) are widely used as high voltage devices integrated into power ICs, because they avoid the limitations of uniformly doped MOSFETs in power applications including problematic short channel, hot carrier, and snapback breakdown issues. Unlike planar and trench VDMOS which have a drain contact on the backside of the die, however, LDMOS employ "surface" conduction, i.e., current flow is concentrated near the surface, and where the distance between the source and the drain determines the devices rated voltage and its ON-resistance.

In order to improve the performance of conventional LDMOSs, several types of trench LDMOS were proposed. Although trench LDMOS are referred to as *lateral* conduction devices (because both source and drain contacts are present on the die surface), actual current flow includes a vertical component down or along the side of a trench gate. This quasi-vertical current increases the cross sectional area of conduction thereby reducing on resistance and moving locations of possible impact ionization into the bulk, away from high surface fields and interfacial charge. The devices can be broken into several broad categories, trench LDMOS, trench charge balanced (RSO or superjunction) LDMOS.

A. Trench Lateral DMOS

Type I trench LDMOS shown in Fig. 21 reduces the distance between source and drain by employing conduction combining a trench VDMOS device with a low-resistance "up-drain" connection similar to trench quasi-vertical DMOS. In operation, (electron) current flows vertically [105] along a trench from the n+ source through the p_{body} DMOS channel region and into a subsurface drain region located on the bottom of the trench, generally formed by implantation into the trench bottom. Unlike conventional LDMOS, the breakdown of the trench LDMOS device is therefore set one dimensionally.

In one implementation shown in Fig. 21(a), drain current returns to the surface n+ drain contact through a conductive plug located *within the same trench* containing the DMOS gate polysilicon, thereby minimizing any lateral resistive components and achieving a high channel density. As reported for 80 V devices, cell pitch and specific

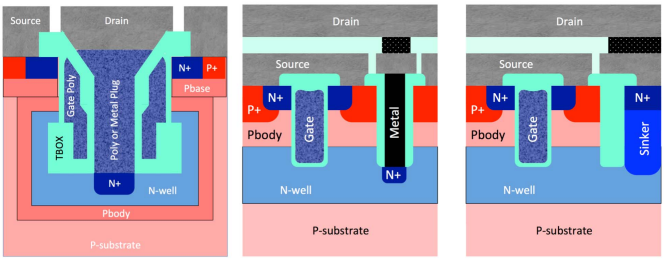

Fig. 21. Type-I trench LDMOS. (a) Single trench up-drain. (b) Dedicated trench up drain. (c) Oxide isolated diffused up drain.

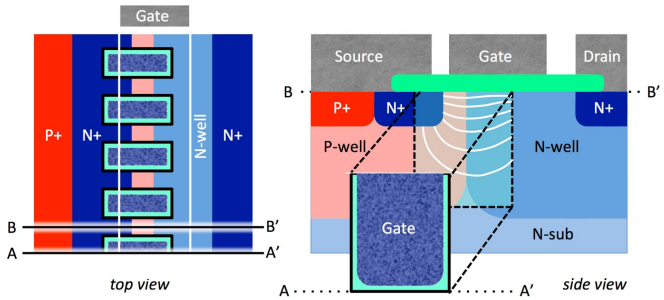

Fig. 22. Type-II trench LDMOS top view and cross section.

ON-resistance was reduced by 50% over comparably rated conventional LDMOS. Numerous variations of the structure have also been reported [106]–[114]. Disadvantages include a complex fabrication process and the impact of the intratrench gate-to-drain oxide thickness, which in addition to limiting the device's maximum drain voltage also introduces significant drain to gate feedback capacitance C_{DG}.

In the version shown in Fig. 21(b), the conductive plug is isolated in its own trench eliminating the adverse impact trench oxide thickness on capacitance or breakdown. Although the channel density is reduced, forming the conductive plug in a dedicated trench has the advantage that the trench up-drain polysilicon can be silicided, using metal to lower the parasitic drain resistance. Fig. 21(c) illustrates another variation using an oxide filled trench to constrain and limit lateral diffusion of a heavily doped sinker diffusion with the advantage that it can easily be integrated into an existing process.

Type-II trench LDMOS shown in Fig. 22 achieves an increased channel density by conducting channel current laterally along the sidewall of a trench gate [115]–[117] oriented orthogonal to current flow.

In operation, electrons emanating from the n+ source flow both vertically and laterally along the side of the trench gate forming a network of current paths of vary length and depth before emerging into the n-type drift region. These multiple parallel conduction paths effectively increase the channel width W of the device in proportion to the trench depth. Additional trench gates are included in parallel to scale the device size and total gate width. Reported results for a 20 V trench LDMOS having a 1 μm depth and a cell comprising alternating trench gate and mesa dimensions of 0.4 μm confirm a 3.5-times increase in channel density and a 50% reduction in ON-resistance compared to conventional LDMOS. Because the channel current flowing near the bottom of the

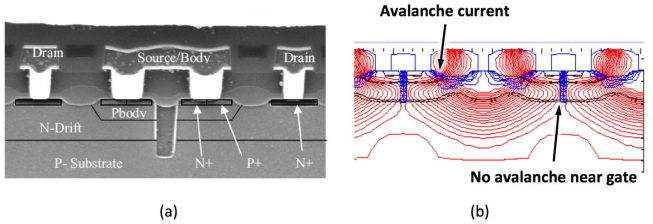

Fig. 23. Type-III trench LDMOS. (a) Cross section. (b) Avalanche current and equipotential contours. No avalanche occurs near trench gate.

trench must travel farther vertically, the deeper conduction components exhibit a longer channel length and higher channel resistivity [$R_{DS}W$]. As such, the benefit in reducing ON-resistance does not scale linearly with trench depth. Further improvements may involve including a deep n+ source to improve current uniformity along the trench.

Type-III trench LDMOS shown in Fig. 23(a) employs a trench gate both for controlling channel current and to function as a vertical current spreader, i.e., using a gate induced accumulation layer to improve current uniformity throughout the entire cross sectional depth of the lateral drift drain [118], [119]. To further improve current uniformity, the drift layer is formed using multiple high-energy phosphorus implants (multiple HEIs of differing target depths).

The total implanted drift dose is selected to meet the surface charge balance (RESURF) criteria, thereby achieving uniform electric fields across the drift (to maximize OFF-state breakdown) while insuring highly uniform drain current distributions (to reduce drift region resistance). Like the HEI drift fabrication, for integration into low thermal budget IC technology platforms, e.g., at 0.35, 0.18 μm, or beyond, the vertically oriented DMOS channel is also formed using multiple high-energy ion implantations of boron [120] without the need for tilt implants, high-temperature double diffusions or well diffusions incompatible with deep submicron IC processes.

The structure [120], [121] offers several advantages over conventional high-voltage RESURF devices including: 1) drain current flows more uniformly throughout the drift; 2) less current flows at the surface thereby reducing surface impact ionization and improving avalanche reliability; 3) the JFET formed by the p_{body}/n_{drift}/p-substrate sandwich pinches off at high voltage (even during current conduction in saturation) shielding the thin gate oxide from high electric fields and minimizing C_{DG}; and 4) hot carrier generation does not occur in the vicinity of the gate.

In a direct comparison against conventional LDMOS fabricated on the same wafer, the trench LDMOS greatly improved HCI performance while concurrently reducing ON-resistance. As shown in the cross-sectional simulation of Fig. 23(b), the drift region around the gate is depleted and shielded from high electric fields and impact ionization [122]. As a result, the measured impact of hot-carrier degradation on I_D decreases by more than one order of magnitude.

B. Charge Balanced Trench LDMOS

Using trench LDMOS, the RESURF concept can be extended to produce lateral superjunction devices, further improving the tradeoff between breakdown voltage and spe-

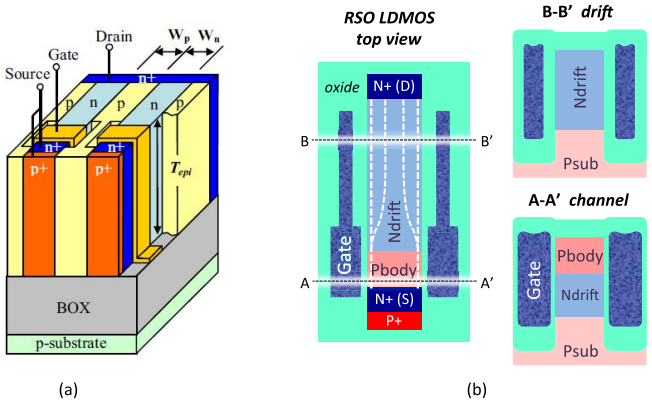

Fig. 24. Charge control (superjunction) trench LDMOS cross sections. (a) SOI based p-n junction lateral SJ drift. (b) Field plate lateral charge balance.

cific ON-resistance. In the SJ device of Fig. 24(a), the combination of the type-II trench LDMOS and laterally oriented p-type and n-type drift columns is formed atop and buried oxide layer to create a lateral superjunction drift [123], the lateral counterpart to a multi-epi vertical superjunction device. In case of a 4-μm deep superjunction LDMOS, an 18-mΩmm^2 specific ON-resistance, better than the 1-D silicon limit, was reported. Fig. 24(b) illustrates an alternative to a lateral superjunction using field plate [124] instead of a p-type column to force two-sided depletion of the n-type drift.

The field plate may comprise a trench field plate extending laterally along the drift or comprise a polysilicon electrode placed atop STI field oxide. The advantage the STI method is that it requires no additional processing needed to fabricate the charge control structure.

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