Effective 3-D Device Electrothermal Simulation Analysis of Influence of Metallization Geometry on Multifinger Power HEMTs Properties

Aleš Chvála, Juraj Marek, Patrik Príbytný, Alexander Šatka, Martin Donoval, and Daniel Donoval, *Member, IEEE*

***Abstract*— In this brief, obtained results of the electrothermal analysis of multifinger power high-electron mobility transistors (HEMTs) are presented. The analysis of thermal and electrical behavior is supported by effective 3-D electrothermal device simulation method developed for Synopsys TCAD Sentaurus environment using mixed-mode setup. The effects of multifinger HEMT structure metallization layout design are described and studied. Simulation results depict the significant effect of metallization geometry on the electrothermal properties and behavior of the power multifinger HEMTs.**

***Index Terms*— 3-D electrothermal simulation, metallization layout, power multifinger high-electron mobility transistor (HEMT).**

I. Introduction

NONUNIFORM thermal dissipation inside the power high-electron mobility transistors (HEMTs) and corresponding self-heating is one of the critical issues due to their capability to locally reach high power density and temperature, which reduces overall device performance and reliability [1]. For high-power devices with compact multifinger layout, thermal crosstalk between individual gate fingers significantly increases structure temperature and reduces power density. Therefore, thermal management is crucially important to the viability of power HEMTs [2]–[4].

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Analysis and optimization using finite-element modeling (FEM) electrothermal simulations are very time-consuming and require high-performance hardware particularly for complicated 3-D structures. Lot of existing works propose effective approaches to electrothermal simulation based on the coupling of an equivalent electrical circuit model and *RC* thermal network [5], [6]. However, the *RC* thermal impedance needs to be extracted from measurement and/or FEM thermal simulation and 3-D geometry-based *RC* thermal mesh needs lot of elements or structure simplifications. Dedicated effort to improve simulation time and accuracy applied in many applications [7]–[9] demonstrates the very active research field in recent electrothermal modeling. Recently Yun *et al.* [10] and Nallet *et al.* [11] applied so-called "mixed-mode" setup in Sentaurus Device [12], which interconnects a 3-D FEM thermal model of the package and a 2-D FEM electrothermal description of the structure by thermal nodes.

In this brief, the electrothermal analysis of multifinger power HEMTs is presented. Analysis and optimization strategy of the metallization layer geometry design are performed and discussed. An efficient 3-D electrothermal device simulation methodology proposed previously in [13] and [14] based on coupling FEM thermal model, FEM electrical model of metallization, and electrical circuit model in mixed-mode setup is used. The advantage of the method is in the high speed of the electrothermal simulation with respect to take into account the current nonuniformity caused by parasitic electrical resistance of the multifinger metallization to electrothermal behavior of active device.

II. Structure and Mixed-Mode Simulation Description

The investigated structure is the power InAlN/GaN HEMT. The thermal model of the device is defined by a 300-nm-thick AlN nucleation layer on a 300-μm-thick SiC substrate followed by a 2.5-μm-thick GaN buffer layer and 8 nm of the InAlN barrier layer on the top [15]. Top ohmic drain/source and Schottky gate contacts are created by Al/Au and Au metallization layers with thicknesses 0.375/0.125 μm and 0.125 μm, respectively [Fig. 1(a)]. The HEMT structure is packaged in DPAK 2 and placed on the printed circuit

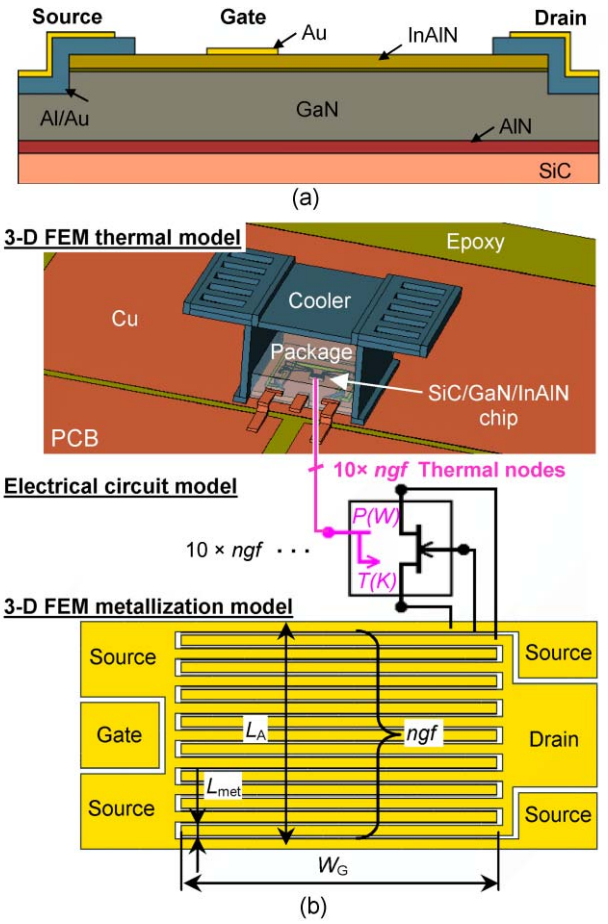

Fig. 1. (a) 2-D cross section of the HEMT structure. (b) Schematic diagram of mixed-mode approach for electrothermal simulation. Thermal nodes provide temperature exchange and heat flux between 3-D thermal model and HEMT circuit model. Current flow is solved in 3-D metallization model. *ngf* represents the number of the gate fingers.

board (0.035/1.6-mm-thick Cu/FR4 layers) including a cooler FK 244 13 D PAK. The HEMT device layout metallization has a multifinger-shaped gate electrode [Fig. 1(b)] with the gate length 1.6 μm, gate to drain distance 4.8 μm and gate to source distance 1.6 μm. The thermal coefficients of used materials are taken from [16] or from default Synopsys parameter file. The conductive surface boundary conditions 20 W/m^2 represent heat transfer to the air.

Mixed-mode setup in Sentaurus Device was used for electrothermal simulations of the proposed HEMT model. The approach interconnects HEMT circuit temperature-dependent model with 3-D thermal model and 3-D electrical model of the metallization by thermal nodes and electrical nodes, respectively [Fig. 1(b)] [14]. The analyzed structure is uniformly split into ten segments along each gate electrode width, and each segment is represented by one circuit model connected with corresponding thermal contacts and metallization. The HEMT circuit model was calibrated according the I–V–T characteristics from [13]. This methodology allows fast and effective simulation of complex systems including all semiconductor layers, metallization, package, and up to cooling assemblies. Simulation of one I–V curve with self-heating effects takes about 15 min.

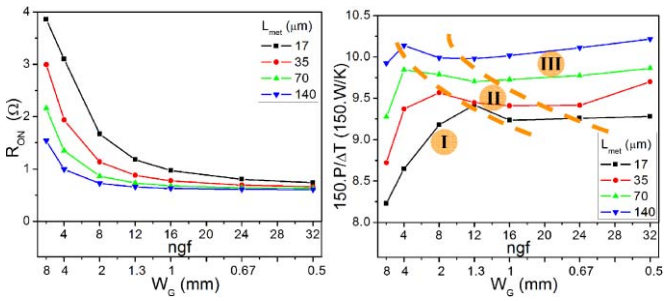

Fig. 2. Dependences of on-state resistance R_{ON} (left) and dissipated power capability $P/\Delta T$ (right) corresponding to a channel temperature increase of 150 K on metallization layer geometry.

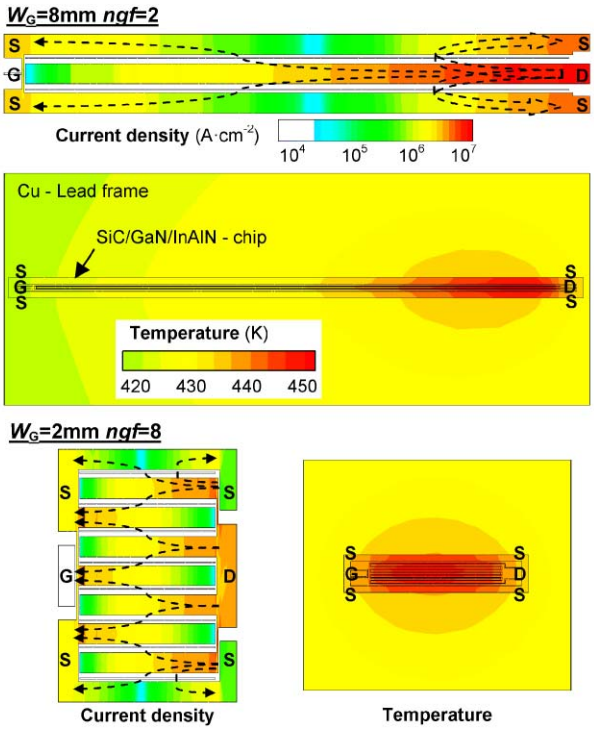

Fig. 3. Current density in metallization and temperature distribution for two different metallization layers geometry of HEMT structure (L_{met} = 35 μm).

III. Electrothermal Analysis of Multifinger HEMT

This section describes the electrothermal analysis of a multifinger power HEMT supported by mixed-mode simulation approach. The analysis of the multifinger HEMT is focused on the metallization layer geometry influence on the electrothermal properties and transistor behavior. The investigated variables are the number of the gate fingers *ngf* and their width W_G. The total gate width of the whole HEMT structure is 16 mm in all the cases. Another investigated variable is drain/source metallization layer thickness.

Fig. 2 shows geometry dependence of the ON-state resistance R_{ON} and dissipated power capability $P/\Delta T$ corresponding to a channel temperature increase of 150 K for different finger spacing, which is given by drain/source metallization width L_{met}. The parasitic resistance of the metallization is more dominant for higher W_G and lower *ngf*, which increases R_{ON} of the analyzed HEMT. The decrease of R_{ON} with W_G

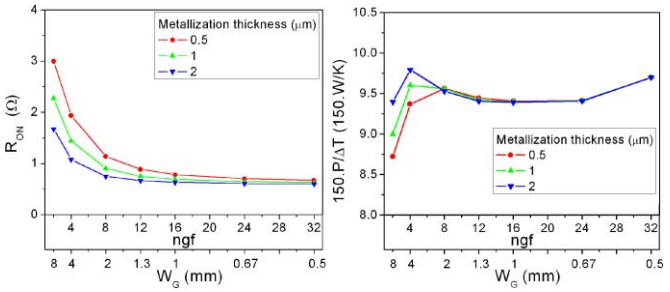

Fig. 4. Drain/source metallization thickness dependences on on-state resistance R_{ON} (left) and dissipated power capability $P/\Delta T$ (right) for L_{met} = 35 μm.

lowering is caused by decreasing of metallization resistance. The lowest value of the R_{ON} is given mainly by the electrophysical properties of HEMT structure. The higher R_{ON} at lower L_{met} is caused by lower width of drain/source metallization layer with higher resistance. Due to additional voltage drop on the high metallization resistance, the current density and power load are nonuniformly distributed in the structure. The nonuniform power load reduces dissipated power capability $P/\Delta T$ of the structure. $P/\Delta T$ increases in region I [Fig. 2 (right)] due to the current flow uniformity improvement when metallization resistance becomes negligible compared with HEMT structure resistance. As can be seen in Fig. 3 (structure with $W_G = 8$ mm), the major part of current flows from drain to source on the drain pad side, where maximal power load and temperature occur. Current density and temperature are homogeneously distributed in structure with $W_G = 2$ mm, where metallization resistance is markedly lower. The following $P/\Delta T$ drop in region II is caused by the dominant thermal interaction of individual gate fingers [2], [3]. As ngf increases, the maximal temperature is higher and $P/\Delta T$ decreases. At the interface of regions II and III, the structure geometry has approximately square shape ($W_G/L_A \approx 1$) with the worst case heat sink condition. There is local minimum of the dissipated power capability. The ratio W_G/L_A becomes lower than 1 with W_G shortening and ngf increases in the region III. The structure is more effectively cooled through the longer L_A edge. Therefore, $P/\Delta T$ increases in this region. The higher distance of gate fingers (higher L_{met}) provides lower thermal coupling and higher P/T for all values of ngf.

Fig. 4 shows drain/source metallization thickness dependence on the ON-state resistance R_{ON} and dissipated power capability $P/\Delta T$ for $L_{met} = 35$ μm. As the metallization thickness increases, the metallization resistance is lower and its impact on R_{ON} decreases. Lower metallization resistance improves current flow and temperature uniformity. Therefore, dissipated power capability $P/\Delta T$ is higher for higher metallization thickness in the region of structures with low ngf and wide W_G.

IV. Conclusion

The electrothermal analysis of the multifinger power HEMTs has been presented. The analysis of thermal and electrical behavior was supported by effective 3-D electrothermal device simulation using mixed-mode setup. The simulation approach helps to assess the device properties by means of evaluating both temperature and current distribution in the HEMT structures operating under different bias conditions and topology in a short time. The effects of structure metallization layers design have been studied and analyzed. We point on the fact that metallization geometry may significantly affect the electrothermal properties of power multifinger HEMTs. Significant growth of R_{ON} occurs mainly for the structure with increasing gate fingers width and thin drain/source metallization layers. As a result, the nonuniform current density and power load reduces dissipated power capability of the structure. Our observations contribute to on-going optimization of power transistor structures with respect to effective metallization layers design.

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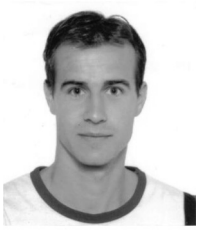

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