Lateral InAs/Si p-Type Tunnel FETs Integrated on Si—Part 1: Experimental Devices

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***Abstract*— Tunnel FETs (TFETs) have been identified as the most promising steep slope devices for ultralow power logic circuits. In this paper, we demonstrate in-plane InAs/Si TFETs monolithically integrated on Si, using our recently developed template-assisted selective epitaxy approach. These devices represent some of the most scaled TFETs with dimensions of less than 30 nm, combined with excellent aggregate performance with average subthreshold swing (SS), of around 70 mV/decade combined with I_{ON} of a few μA/μm for $|V_{DS}| = |V_{GS}| = 0.5$ V. Here, we will discuss the device fabrication as well as the experimental electrical data. Extensive low temperature characterization and activation energy analysis is used to gain insights into the factors limiting device performance. Combined with the simulation study presented in part 2 of this paper, this will elucidate how traps are ultimately limiting the SS.**

***Index Terms*— Heterojunction device, InAs, selective epitaxy, tunnel FET (TFET).**

I. Introduction

THE scaling of operating voltages beyond 0.5 V poses a problem for the MOSFETs due to their fixed turn-ON subthreshold swing (SS), which is given by

$$\mathrm{SS} = \ln\ (10)\frac{k_B T}{q}\left(1 + \frac{C_d}{C_{\mathrm{ox}}}\right) \tag{1}$$

where k_B is Boltzmann's constant, T is the temperature, q is the elementary charge, C_d is the depletion layer capacitance, and C_{ox} is the gate-oxide capacitance. At 300 K, this results in an ideal value of 59.5 mV/decade, which is usually referred to as the 60 mV/decade limit of the MOSFET. Hence, there is a fundamental limit of how steep the turn-ON of the MOSFET can be; independent of device design or charge carrier mobility in the material. Actual scaled devices usually have slightly worse SS due to nonoptimal electrostatics. Tunnel FETs (TFETs) based on band-to-band tunneling (BTBT), however, are based on different operating mechanisms and may achieve subthermal swings. Although subthermal minimum slopes have been demonstrated, experimentally observed slopes averaged over 2–3 decades of current are as of yet larger than 60 mV/decade. This paper is part 1 of a two-part paper, which summarizes the collaboration of two research groups. Part 1 discusses the device fabrication and electrical characterization of InAs/Si TFETs integrated laterally on a conventional silicon-on-insulator (SOI) substrate. An important aspect of this paper was to establish a CMOS-like device integration flow on Si, which is extendable to a complementary III–V TFET integration platform [3]. In this paper, we will present a detailed analysis of the fabrication and experimental characterization of our high-performance InAs/Si TFETs. Part 2 will focus on the detailed simulation of these same devices, to investigate the factors, which at present limit SS and guidance will be given as to which trap density (D_{it}) levels at the junction and at the semiconductor–dielectric interface must be achieved in order to observe the subthermal swing over several decades of current.

II. Device Fabrication

A schematic of the process flow is shown in Fig. 1. The p^+-Si drain is defined by boron diffusion doping through openings in an oxide mask. The hole concentration is mid 10^{19} cm^{-3} throughout the thickness of the Si layer, determined by the secondary ion mass spectroscopy analysis. This correlates well with four-point-probe measurements on pieces from the same SOI wafer used for the calibration of the diffusion doping process, which resulted in average active carrier concentrations in the low 10^{19} cm^{-3}. The device features are defined by *e*-beam lithography using an Hydrogen silsesquioxane mask and dry etching of the SOI layer using HBr. The template is fabricated by depositing ~50-nm-thick SiO_2, and an opening at one end is created by patterning with polymethylmethacrylate and etching the oxide using buffered hydrofluoric acid (BHF). The Si, which is to be replaced by InAs, is etched in 2% TMAH at 75 °C leaving a hollow oxide nanostructure, which we refer to as the template. This anisotropic etch leaves smooth (111) planes in the remaining Si. Metal-organic chemical vapor deposition is used to selectively grow an InAs source within the template which is *in situ* n-doped (2×10^{18} cm^{-3}) using Si_2H_6. From previous results [1], we know that the InAs material quality is high, with electron Hall mobilities of 5400 cm^2/Vs in nonintentionally

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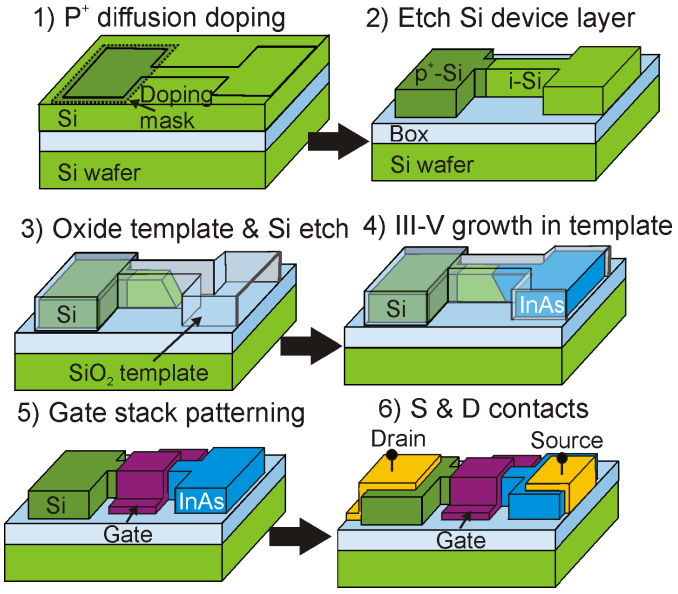

Fig. 1. InAs-Si TFET process flow. (1) p^+-Si drain is defined by diffusion doping using an oxide mask (not shown). (2) Device is dry-etched into the SOI layer. (3) SiO_2 is deposited to create the template, which is opened by BHF at one end and the sacrificial Si, to be replaced by InAs, is etched back in TMAH. (4) n-doped InAs is grown within the template. (5) Gate-stack is deposited and patterned. (6) Source and drain contacts are created by lift-off of Ni/Au.

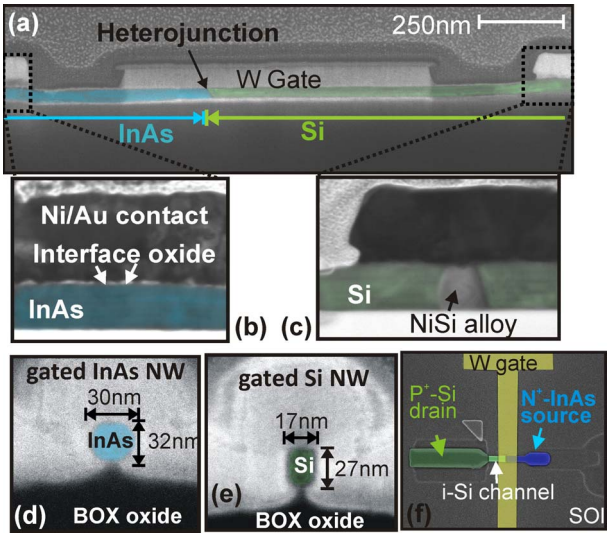

Fig. 2. SEM images of devices. (a) Cross-section of device DF41 along the channel, the heterojunction is visible with an inclination according to the (111) plane resulting from TMAH etching. (b) InAs-Ni interface shows the presence of an interface oxide, which seems to be partially perforated. (c) Si-Ni interface shows Ni-alloy formation. Cross-sections of the (d) InAs NW segment constituting the TFET source, and (e) Si NW channel. (f) Top view of device illustrating the lateral integration approach. The triangle on the Si side indicates the position of the Si p^+ doping mask. Color is applied on top of SEM to highlight the individual regions.

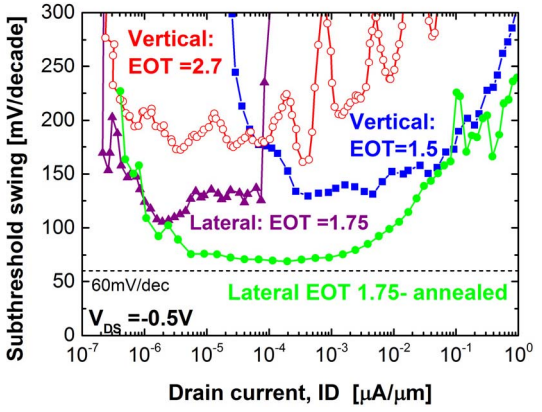

Fig. 3. Comparison of lateral InAs/Si TFETs presented in this paper before (purple triangles) and after (green circles) contact anneal with previously reported vertical TFETs based on the same material combination and here shown for two different EOT thicknesses [7]. EOT scaling was found to mainly impact I_{ON}, whereas what we observe here is that geometrical scaling substantially improves SS, but with an expected smaller impact on I_{ON}. Contact annealing (5 min at 300 °C in Ar) significantly improves performance, we believe this is mainly due to the formation of NiSi at the Si drain contact.

doped material (4×10^{17} cm^{-3}).

Following InAs growth, the template oxide is stripped in BHF, and a gate-stack is deposited, consisting of 20 cycles Al_2O_3 followed by 33 cycles HfO_2 deposited at 250 °C, and a gate metal of 50-nm sputtered tungsten (W). This results in an equivalent oxide thickness (EOT) of ~1.75 nm.

At this point, a forming gas anneal in 25% H_2 in Ar at 300 °C for 10 min is carried out. Subsequently, the gate metal is patterned by SF_6-based dry etching. Source and drain contacts are created by lift-off of Ni/Au metal layers. A cross section along the channel in one of the measured devices (DF41) is shown in Fig. 2(a). The gate length is roughly 850 nm, of which about 250 nm overlap the InAs source.

The cross section of the Si nanowire (NW) is about 17×27 nm^2, and the InAs NW cross section is 30×32 nm^2, the difference in dimensions is due to the use of a diluted HF-dip right before growth which etches the inner walls of the template. Minor thickness variations (±1–2 nm) might occur from one device to the next, as a result of variations in the oxidation process thinning down the SOI wafer. For normalization purposes, an effective width $W_{eff} = 100$ nm is used, which assumes a gate-all-around geometry and is intermediate between the values on the Si and InAs side. As the tunneling path is nonlocal, both sides of the junction matters, and a normalization simply taking the smallest geometry is not justifiable.

First measurements were carried out at this point and showed relatively poor ON-current and SS with large variation between individual devices. A contact alloying step (5 min at 300 °C in Ar) was performed, which improved device performance substantially as observed in Fig. 3. Transmission line measurement structures on Si which are not included here showed a strong improvement in contact resistance following the annealing step. We believe this to be due to NiSi formation visible in Fig. 2(c).

The initial high contact resistance on the highly doped p^+ Si is expected to be caused by the existence of an atomically thin boron-rich oxide at the Si interface, a known common side effect of some types of diffusion doping [4].

This boron-rich layer is not removed in the HF steps, but is penetrated during the annealing step, as it can be seen

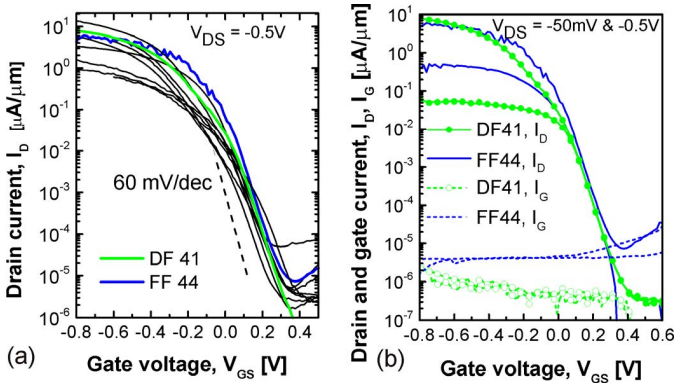

Fig. 4. (a) Transfer characteristics of a number of TFETs, showing reproducible characteristics in terms of I_{ON} and V_t. The two devices on which the most extensive temperature characterization was carried out are highlighted in color, DF41 and FF41. (b) Transfer characteristic and gate current at both –50 mV and –0.5 V V_{DS} for DF41 and FF41. Note that for clarity fewer points (circles) than actually measured are shown in this graphic.

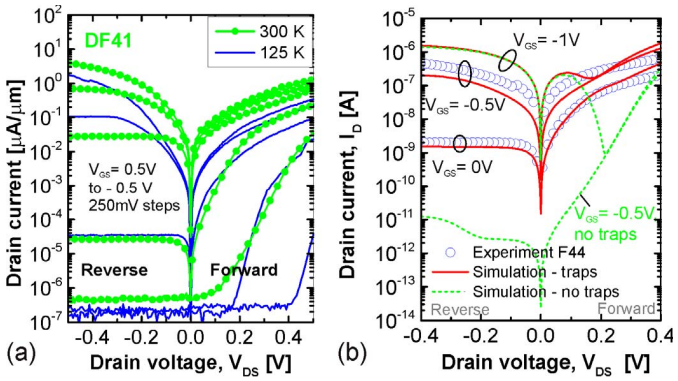

Fig. 5. (a) Gated diode current as a function of gate bias for device DF41, measured at room temperature and 125 K. The reverse bias branch corresponds to the TFET output characteristics. (b) Comparison of experimental I_D (FF44, blue circles) and the simulated I_D, red curves correspond to the trap level found *using* the fitting of the entire characteristic in this device, whereas the green dotted lines shows what the simulation would look like when neglecting all sources of traps. In both cases, it is clear that for our measurement conditions NDR is not expected, only for $V_{GS} > 0.75$ V does a plateau start to appear.

in the SEM picture showing the formation of NiSi regions underneath the Ni contact.

In Fig. 2(b), remnants of an interface oxide on the InAs contacts are observed and no formation of a Ni–InAs alloy is visible, and thus this might still limit I_{ON}. However, in this case it is likely due to rapid reoxidation of the InAs surface during the transfer to the evaporation chamber. InAs contact resistance is generally fairly low. In the past, we have measured around 10^{-6} Ωcm^2 to low-doped InAs on dedicated contact test structures, and with sulfur-passivation prior to the metal evaporation, which is known to reduce the contact resistance [5], we measured 9.5×10^{-8} Ωcm^2 as reported in [1].

Fig. 3 shows a comparison of the new devices before and after the contact anneal with previously fabricated vertical InAs/Si TFETs [6], [7] with two different EOT thicknesses. Previous devices had cross sections of about 100 nm, while the lateral TFETs are in the sub-30 nm regime. We have chosen the SS versus I_D graphical representation as this does not require matching of threshold voltages or similar. The ON-currents of present devices are comparable with vertical devices demonstrated in the past [7], although the EOT in present samples was kept slightly more conservative. On the vertical TFETs, we mainly found EOT scaling to improve I_{ON} and with little impact on SS. The greatest improvement in the new devices lies in the average SS, which is now as low as 70 mV/decade.

III. Electrical Characterization

Transfer characteristics of a number of TFETs from the same wafer are shown in Fig. 4(a). Here, it can be observed that the device characteristics are reproducible, and that the devices we focus on in the following are representative.

The device DF41 (green bold line) is one of the four devices on which we carried out the most extensive temperature characterization, and also the device which was cut in the focused ion beam and imaged (Fig. 2), in order to extract all relevant geometrical parameters. The device FF44 (blue bold line) is the device which has been mainly used for fitting of the simulation parameters in part 2. Thus, the characteristics of these two devices will primarily be displayed in the following. However, it is evidenced in Fig. 4(a) that those two devices are generally representative. From a fabrication point-of-view, the difference between these two devices is that the intrinsic length is 300 nm longer in the case of FF44, and thus the gate might be slightly underlapping the drain. However, when comparing our devices in general we have not observed an impact of this parameter on device performance, and simulation has also not shown this to be significant. Fig. 4(b) shows the transfer characteristics of the two chosen devices at –50 mV and –0.5 V V_{DS} bias, respectively, along with the gate current. From this, it may be observed that gate leakage current is not limiting performance in the transition region, although it is the cause of the higher I_{OFF} in the OFF-state in the case of FF44. The flatness of I_{ON} at 50 mV, in particular for DF41, is indicative of a potential barrier (for example an interface oxide) limiting the current levels in general, and in particular for V_{DS} values which are low in comparison with the thermal voltage. This will be discussed further in relation to the low-temperature measurements.

In addition to the transfer characteristics, we also measured the gated diode characteristics [Fig. 5(a)] as a function of gate bias. The reverse bias branch corresponds to the output characteristics $I_D(V_{DS})$ of the TFET. As detailed in [3], a negative differential resistance (NDR), in the forward bias was observed in the InAs/Si diodes of [8] having a high doping concentration on both sides of the junction. An NDR in this materials system requires simultaneously very high doping concentration on both sides of the heterojunction.

Fig. 5(b) shows why an NDR is absent in the present devices in the measurement range investigated. Here, the blue circles represent experimental diode characteristics at a gate bias of 0 and -0.5 V for device FF44. The red curves correspond to a simulation, including all the sources of traps in the same

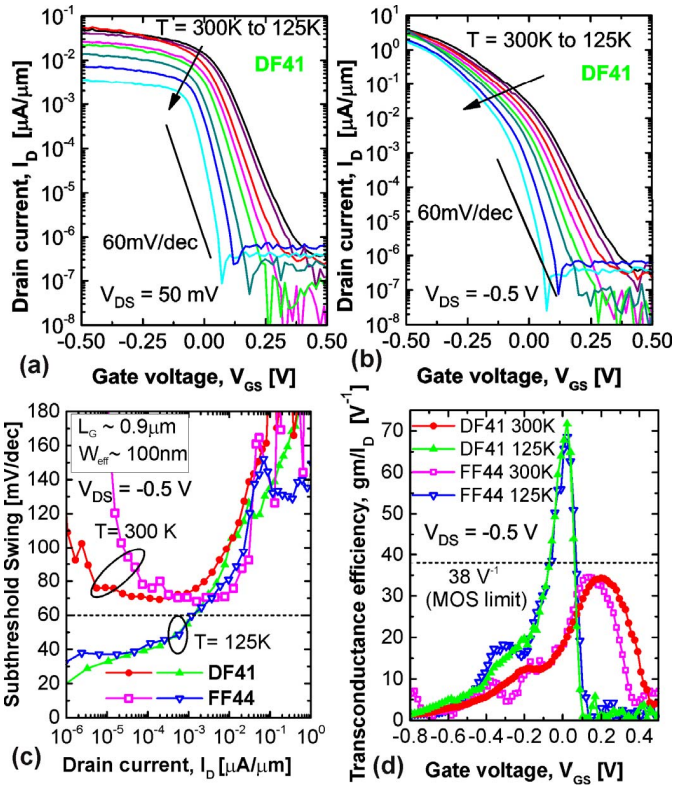

Fig. 6. Transfer characteristics of device DF41 with T-sweep from 300 to 125 K for V_{DS} bias levels of (a) −50 mV and (b) −0.5 V. (c) Comparison of SS as a function of I_D for two different devices at 300 and 125 K. (d) Transconductance efficiency for the same two devices at 300 and 125 K.

device, with levels based on the fitting of the transfer curves in part 2. The gate overlaps the InAs segment (source), so as we increase the hole concentration in the Si channel, by biasing the gate, we are simultaneously reducing the electron concentration in the InAs. Because of this device design, it is revealed that the doping levels on both sides at $V_{GS} = -0.5$ V are insufficient to observe an NDR, which is only predicted at a V_{GS} of about −1 V. In Fig. 5(b), a simulation neglecting any contribution from traps (green dotted line) is shown and indicates that the high current level for low and intermediate gate bias is due to the presence of traps.

IV. Low-Temperature Analysis

Transfer characteristics of device DF41 at temperatures from 300 down to 125 K are shown in Fig. 6 for $V_{DS} = -50$ mV and $V_{DS} = -0.5$ V. In the case of the low V_{DS} bias, the flatness for V_{GS} greater than about −0.1 V along with the strong temperature dependence in this region is a signature of the presence of a potential barrier. For higher bias levels, the impact of this potential barrier is reduced, and we observe the small I_{ON}-dependence expected for a TFET, as illustrated here for $V_{DS} = -0.5$ V. SS and transconductance efficiency for two different devices with the same geometry as a function of temperature are shown in Fig. 6(c) and (d), respectively. The 60 mV/decade room temperature limit is indicated by a dotted line, the corresponding limit at 125 K would be 25 mV/decade, according to (1).

Low-temperature measurements are commonly used to distinguish TFET from MOSFET behavior. I_{ON} in a MOSFET is mainly determined by the carrier mobility (neglecting parasitic series resistances), which for silicon reduces at higher temperatures. In an ideal TFET, it is not the mobility but rather the BTBT rate, which determines the achievable current. The material parameters influencing the tunneling probability are the effective tunnel gap and the tunneling masses. In a heterojunction, the former is influenced by the energetic position of the band edges at both sides of the source-to-channel junction. The temperature dependence is mainly determined by the effective change in tunneling gap—the exact nature of this dependence might be difficult to establish for heterostructure devices, but only a negligible temperature dependence should be observed.

In the case of the high V_{DS} bias [Fig. 6(b)], the temperature dependence of I_{ON} is very limited, and reduces even further when we go to V_{GS} bias levels beyond −0.5 V. For the low V_{DS} bias level of 50 mV [Fig. 6(a)], we observe a strong temperature dependence of I_{ON}. We believe this to be caused by the existence of a potential barrier caused by an interface oxide at the InAs contact, which the carriers need to overcome. Note that due to the low bandgap of InAs and Fermi-level pinning, the formation of a Schottky barrier on InAs is very unlikely. Even if this would be the case, the physical distance between the source contact and the channel would prevent the formation of a Schottky barrier FET like reported in [9].

Fig. 6(d) shows the transconductance efficiency for those same two devices. Similar to the 60 mV/decade limit one might derive a limit on the maximum achievable transconductance efficiency of 38 V^{-1} for a MOSFET at room temperature. Both devices shown here reach a maximum of about 34 V^{-1} at 300 K.

The SS exhibits a fairly strong temperature dependence as shown in Fig. 6(c). This is most likely due to the presence of traps at the heterojunction interface, and this mechanism will be explained in more detail in part 2 of this paper. Although the devices are true TFETs, the device operation in the transition region is dominated by the generation of carriers via interface traps, which has significant consequences on the TFET characteristics. How this mechanism works is explained in detail in part 2 of this paper, but it results in an SS which is limited by thermionic emission, so that a MOSFET-like SS temperature dependence is observed rather than the temperature independence expected for pure BTBT processes. For higher levels of gate bias, BTBT dominates and determines the magnitude of I_{ON}.

Recently, the best TFET results (see Fig. 9) seem to converge toward average SS values between 60–80 mV/decade similar to our devices here and suspiciously close to the thermionic limit of the MOSFET, despite theoretical predictions of subthermal slopes. We believe that in many cases when a sufficiently good TFET geometry in terms of electrostatics is achieved, what is observed is the limitation due to trap or defect processes. In the present case it converges toward the thermionic limit, as it will be explained in part 2. Hence, in order to achieve sub-60 mV/decade operation, reduction of the defect concentration is crucial.

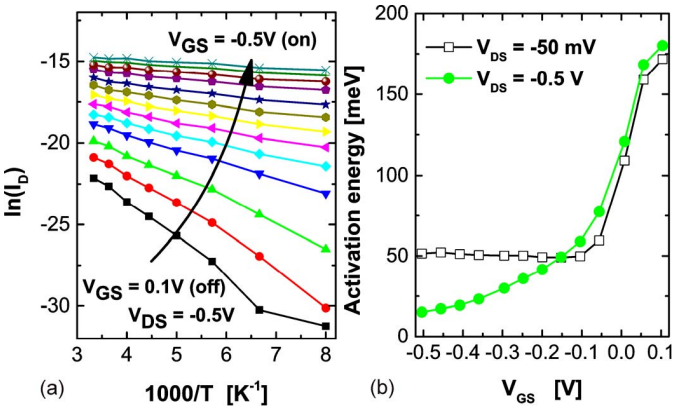

Fig. 7. (a) Arrhenius plot of $\ln(I_D)$ versus inverse temperature for different gate bias levels covering the turn-ON transient of the TFET, curves shown here are for $V_{\rm DS} = -0.5$ V for device DF41 Fig. 6(b). (b) Activation energy extracted for two different $V_{\rm DS}$ bias levels.

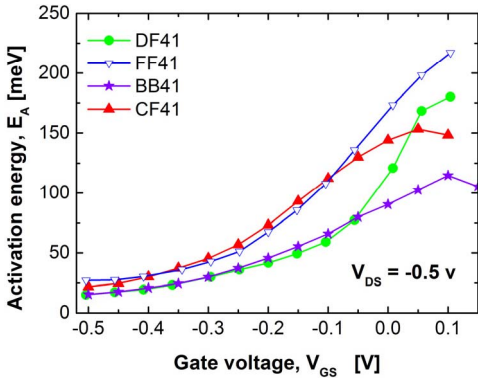

Fig. 8. Activation energy for the four TFETs on which full temperature sweeps were done, all shown for $V_{\rm DS} = -0.5$ V.

In our case, we believe the origin of the defects to be the lattice mismatch at the InAs/Si heterojunction (about 11%), which gives rise to misfit dislocations which usually terminate within a few nanometers. Tomioka and Fukui [10] have investigated both InAs/Si and other material systems and predict that these defects are reduced with the scaling of the NW diameter, but that a very small NW diameter is necessary to fully avoid their formation, in the case of the InAs/Si material combination substantially below 10 nm.

In order to further investigate device physics, we have carried out an activation energy analysis of these devices. The result is shown in Fig. 7 based on the transfer characteristics of Fig. 6(a) and (b). One assumes that the current follows an Arrhenius relation:

$$I_D = Ae^{-\frac{E_A}{k_B T}} \tag{2}$$

where A is a constant, k_B is Boltzmann's constant, T is the temperature, and E_A is the activation energy. For the low $V_{\rm DS}$ bias of 50 mV, the activation energy in the ON-state remains pinned at a value around 50 meV. We attribute this to a barrier at the InAs contact, which the carriers have to overcome. At higher bias levels, we see no effect of the contact barrier; hence, we have used a $V_{\rm DS}$ of 0.5 V for the data analysis.

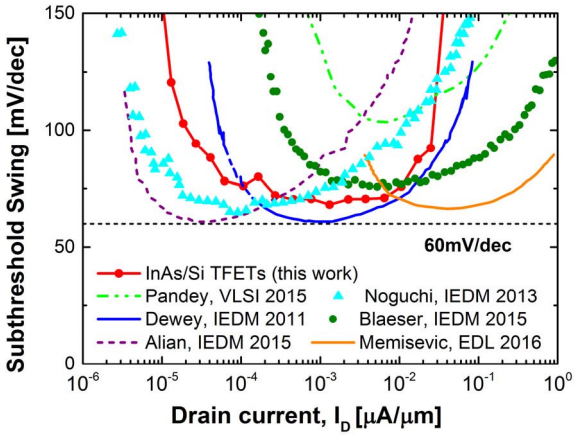

Fig. 9. SS as a function of drain current, extracted from a number of published TFET works [11]–[16]. Values are adapted from pdf data so minor variations might appear. In all cases, we have chosen values close to 0.3 or 0.5 V.

Fig. 8 shows the activation energy extracted for four devices on which we did a full temperature sweep. The behavior is similar among devices, with some variation expected due to the nanoscale geometry, which means that small changes in interface quality, defects, and metal contacts can have a large impact. Note that for high gate bias where BTBT dominates, (1) is not valid, and only a weak temperature dependence due to the bandgap should be expected.

V. Benchmarking and Outlook

In the field of TFETs, it can be difficult to compare various devices as a result of vastly different geometries and biasing conditions. In the past, we have attempted to benchmark devices based on average SS versus $I_{\rm ON}/V_{\rm DS}$ [7], as there tends to be a tradeoff between SS and $I_{\rm ON}$, we believe any metric should incorporate both. The difficulty with the methodology we used in the past was that we attempted to cover the entire body of published TFETs, i.e., a very broad range of current levels, ultimately leading to some arbitrariness introduced by the definition of $I_{\rm OFF}$.

In Fig. 9, we compare the SS versus I_D for this paper with that extracted from a number of experimental references. A few other good experimental devices are not included because they either did not include an SS versus I_D plot or I_D values were not normalized to effective width. The purpose is not to discuss the merits of each one; those are all among the very best experimental TFETs in their own right, but with different merits and challenges, nevertheless none achieve subthermionic slopes over a significant range of currents. The majority of fabricated devices lie outside of this chart, because slopes are too large or current levels much too low for practical use.

Based on our own experience and recent conclusions of others [17], we may conclude that in our case once device geometries have been fine-tuned and sufficiently scaled, trap mechanisms ($D_{\rm it}$, heterojunction, doping, material defects) are responsible for the performance limitations. Hence, to experimentally realize the promises of TFETs, which we know from

simulation studies, we have first to establish the nature of the traps and then find appropriate solutions to deal with these.

As it is evident from Fig. 9, our devices show the state-of-the art performance, but they are limited by heterojunction defects. How these impact the device performance will be discussed in detail in part 2 of this paper, which will also provide guidelines on design optimization. Beyond performance, the merit of our devices lie in being fully scalable and integrated in a CMOS-like process flow, which has been our target from the onset. In [3], we have established the basis for a complementary TFET platform, by combining these p-channel TFETs with n-channel InAs/GaSb devices.

Recent works [17], [18] have shown that body-thickness scaling is the most important parameter when it comes to achieving subthermal swings, scaling is more easily achieved in this lateral template, so we wish to explore this further in the future.

VI. Conclusion

In this paper, we have presented InAs/Si TFETs which are monolithically integrated on Si using Template Assisted Selective Epitaxy—a technology which allows for Very Large Scale Integration compatible integration of III–V heterojunction devices directly on Si. The device scaling afforded us by this approach down to sub-30 nm, is shown to improve average SS compared with our previous works on vertical InAs/Si TFETs. Further reduction of SS is limited by defects, in our case particularly at the heterojunction, as it will be discussed more in detail in part 2 of this paper. Furthermore, we show an improved benchmarking of experimental devices, and the overall performance of the devices presented here are among the best for any TFETs.

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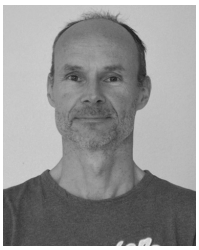

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