High-Voltage Organic Thin-Film Transistors on Flexible and Curved Surfaces

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***Abstract*— A pentacene ($C_{22}H_{14}$)-based high-voltage organic thin-film transistor (HVOTFT) was demonstrated on both a rigid and a flexible substrate. The HVOTFT showed minimal degradation of the current–voltage (I–V) characteristics under flexure. Consistent with the previous reports on amorphous silicon (a-Si) TFTs, the offset drain/source structure enabled high-voltage operation, allowing for the HVOTFT to switch very large drain-to-source voltages (V_{DS} > 300 V) with a relatively lower controlling voltage (0 V < V_G < 20 V). The HVOTFT was evaluated with three different gate insulators to assess how the dielectric constant and interface states influence device performance. Due to the high electric field generated in the device, the HVOTFT suffered from impeded charge injection into the gated semiconductor channel, similar to that reported in a-Si-based high-voltage TFTs, as well as from a nonsaturating I–V characteristic behavior similar to the short-channel effects found in FETs. A field plate was implemented to improve charge injection into the gated semiconductor channel. Output characteristics of the HVOTFT were numerically corrected to demonstrate that the device I–V can be modeled with the existing Si-based FET models.**

***Index Terms*— Flexible substrates, high-κ gate dielectrics, high-voltage thin-film transistors (HVTFTs), organic semiconductors.**

I. Introduction

THERE EXIST many applications that require drive voltages beyond the typical operating range of the conventional thin-film transistors (TFTs). Among these applications are ferroelectric liquid crystals, electrophoretic or $Pb_{1-x}La_x(Zr_yTi_z)_{1-x/4}O_3$ electrooptic displays for electrographic plotters [1], [2], digital X-ray imaging [3], [4], poly-Si cold cathodes [5], and sophisticated integrated MEMS [6]. For these applications, the large drive voltages take precedence over large drive currents, which aptly suits the high-voltage TFT (HVTFT) as a voltage driver for these applications.

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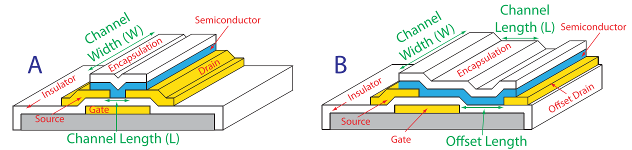

Fig. 1. Comparing the structures of (A) OTFT and (B) HVOTFT with the offset by the drain.

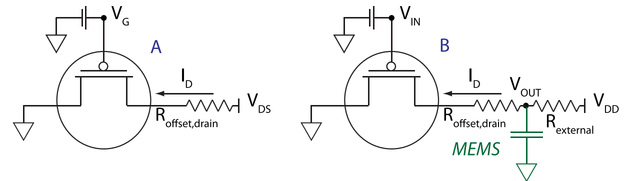

Fig. 2. (A) Effective circuit schematic for HVOTFT with offset drain structure modeled as a resistor. (B) Example of how the HVOTFT can be used to drive MEMS, which is modeled as a capacitor.

The realization of such applications on flexible substrates widens the use for the traditional MEMS. For example, flexible substrates can improve portability, giving rise to compact digital X-ray imaging devices. In addition, the ability to integrate MEMS and its driving circuitry on a single flexible substrate could motivate shape-shifting fabrics, for potential robotic and autonomous systems. To enable such systems, the appropriate driving circuitry that includes the HVTFT must be demonstrated on a flexible substrate. While organic semiconductors are frequently used to enable electronic devices on flexible substrates, there are few to no reports of organic semiconductors for flexible high-voltage electronics.

This paper reports that high-voltage organic TFTs (HVOTFTs) are viable for high-voltage circuits and have the potential to enable new flexible MEMS applications. The HVOTFTs can be placed on flexible substrates with minimal change to its current–voltage (I–V) characteristics under flexure, operate similar toamorphous silicon (a-Si) HVTFTs, and can be described by models developed for Si-based FETs.

II. Device Design and Fabrication

Fig. 1 shows the OTFT and HVOTFT device structure with a bottom contact architecture. The gated and offset (ungated) structure employed successfully in [1] and [7] for poly-Si- and a-Si-based HVTFTs, respectively, was used for the HVOTFTs

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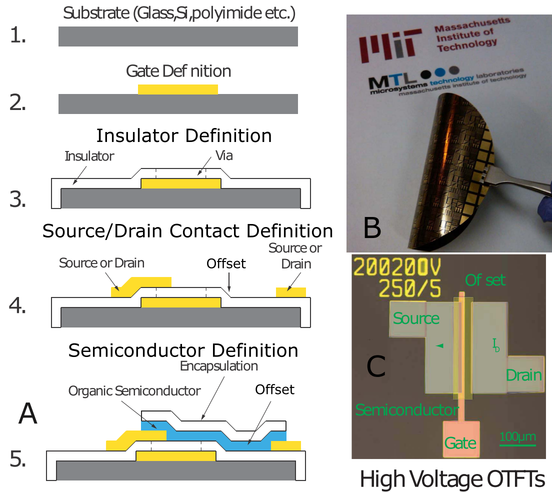

Fig. 3. (A) Process flow for fabricating OTFTs. (B) Completed 100-mm wafer. (C) Micrograph of completed HVOTFT.

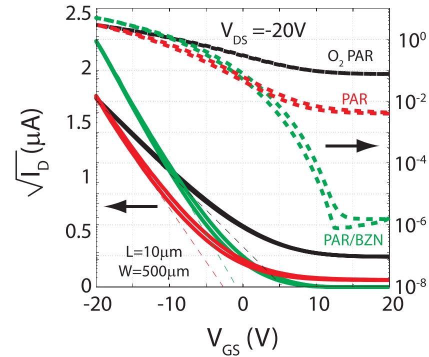

Fig. 4. Transfer Characteristics for OTFT with PAR, O_2 PAR, and PAR/BZN insulators. The channel width and length are $(W) = 500$ μm and $(L) = 10$ μm, respectively. V_{DS} is stepped from -5 to -20 V in -5 V increments while V_{GS} is swept from 20 to -20 V in -0.25 V increments.

TABLE I

DEVICE PARAMETERS FOR PAR, O_2 PAR, AND PAR-/BZN-BASED OTFTs

PARAMETERS	PAR	O_2 PAR	PAR/BZN
t_{ins} (nm)	500	350	200/200
κ	3	3	6
V_T (V)	-1.7	5.4	-0.24
μ (cm^2/Vs)	0.068	0.023	0.014
I_D (μA)	3	2.5	6.5

in this paper. The gate electrode allows for charge to be accumulated in the gated region. The offset region enables high-voltage operation. An equivalent circuit of the HVOTFT is shown in Fig. 2(A), where the offset is modeled simply as a resistor. Fig. 2(B) shows how the HVOTFT would be used as a driver for MEMS by placing the HVOTFT in series with an external resistor to build an inverter circuit. The MEMS is then connected to the offset and external resistor or V_{OUT} node of the inverter. Reports in the literature show this structure and layout to be effective for driving MEMS [2], [6].

The process techniques used to fabricate HVOTFTs are derived from similar approaches reported in [8]. The substrate was a 100-mm glass or flexible Cirlex wafer. The 10-nm Cr adhesion layer followed by a 100-nm Au gate metal are both deposited by e-beam evaporation and patterned by photolithography and a wet etch. Gate insulator stack consisting of parylene-C and/or $Bi_{1.5}Zn_1Nb_{1.5}O_7$ (PAR/BZN) dielectrics were tailored to achieve specific device performance. Chemical vapor deposition is utilized to deposit PAR, with vias patterned by photolithography and a dry O_2 plasma etch. RF magnetron sputtering is employed to deposit BZN with the substrate at room temperature, RF power at 95 W and 9:3 argon to oxygen gas ratio at a pressure of 3 mtorr. The stoichiometry of the sputter target is BZN, which is the intended composition of the film. The BZN is patterned by photolithography and wet etched with a very dilute BOE. For the source/drain electrodes, 100 nm of Au is deposited by e-beam evaporation and patterned by photolithography and a wet etch. A surface treatment, exposing the PAR to O_2 plasma, is used to shift the threshold voltage (V_T) by creating interface traps (Q_{it}) [9]. The pentacene semiconductor layer, transparent with a blue-ish tint, is deposited by thermal evaporation to a thickness of 10–40 nm at a rate ~2nm/min at a pressure of 2×10^{-7} torr. The pentacene is then encapsulated by PAR to protect the pentacene from the solvents. The device is completed by patterning the semiconductor and encapsulation layer by O_2 plasma. An illustration of the device processing is shown in Fig. 3 with the completed wafer and device.

III. RESULTS AND DISCUSSION

A. Electrical Characterization: Devices on Flat and Rigid Substrates

When comparing the MEMS applications that require high frequency [fast charging and discharging, large drive currents (I_D)] to those that need to generate large forces (high voltages, large V_{DD}), the different circuits and devices designs are necessary. Therefore, we explored the effectiveness of insulator engineering to tailor the HVOTFT for such high-voltage switching. Surface treatments and high-κ insulators [9]–[11] are proven methods of tuning OTFT performance in terms of increased drain current and/or altering the V_T.

Performance tuning was investigated through three dielectric options: 1) low-κ PAR; 2) O_2 plasma treated PAR (O_2 PAR); and 3) a composite stack consisting of PAR/BZN. The transfer characteristics of the conventional OTFTs were measured to determine V_T, mobility (μ), and I_D resulting from the gate insulator engineering, as shown in Fig. 4 and tabulated in Table I. Shifting V_T from -1.7 V (PAR) to 5.4 V (O_2 PAR) is achieved by O_2 PAR which changes the density of charges at the interface Q_{it} in (1), which was shown to be effective in [9]. To increase I_D and reduce V_T, a composite insulator stack of PAR/BZN was used. Choi *et al.* [11] first demonstrated BZN to be a viable high-κ gate insulator for OTFTs. The composite insulator stack combines the high-dielectric constant [κ in (1)] of BZN with the high-breakdown field of PAR. The dielectric composite (PAR/BZN) had an effective dielectric constant of 6, such that twice as much charge was accumulated in the gate insulator for the same voltage. As indicated by (2), the drive current ($-I_{D,\text{sat}}$) extracted at V_{GS} and $V_{DS} = -20$ V

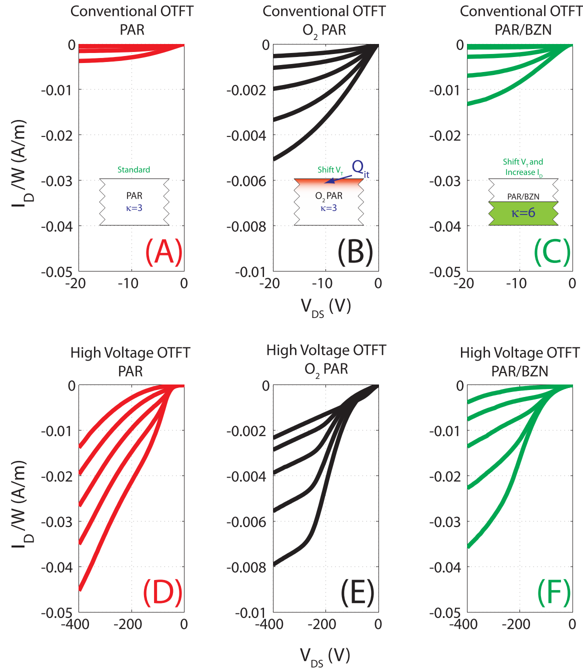

Fig. 5. (A)–(C) Standard OTFTs with no offsets at lower operating voltages. They are plotted for comparisons with HVOTFTs which should saturate at the same I_D/W. (D)–(F) HVOTFTs with a channel length (L) is 10 μm with a 20-μm offset at the drain, at high operating voltages. Gate-to-source voltage (V_{GS}) stepped from 0 to -20 V in -5 V increments. Drain voltage (V_{DS}) stepped from 0 to -400 V in -5 V increments.

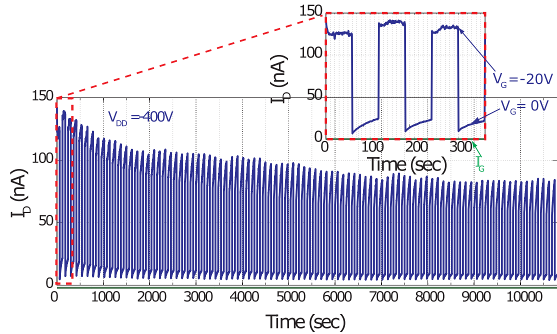

Fig. 6. 180 min high-voltage stressing of the HVOTFT. The channel length (L) is 10 μm with a 20-μm offset at the drain. The gate insulator is 300 nm of PAR. I_D decreased during the first cycles of the test then stabilizes.

approximately doubles.

$$V_T = (\phi_M - \phi_S) - \frac{t_{\text{ins}}}{\epsilon_O \kappa}\left(Q_{\text{it}} - \int_0^{t_{\text{ins}}} \frac{t}{t_{\text{ins}}} \rho_{\text{ins}}(t) \cdot dt\right) \quad (1)$$

$$-I_{D,\text{sat}} = \frac{\mu W \epsilon_O \kappa}{2 L t_{\text{ins}}} (V_{\text{GS}} - V_T)^2 \quad (2)$$

Fig. 5 compares the output characteristics of the conventional OTFTs and HVOTFTs. For HVOTFTs, the gate is influencing the drain current; however, the drain current does not saturate and suffers from what Martin *et al.* [2] describe as an impeded charge injection due to metastable states at the boundary of the gated and ungated regions. These issues obscure the impact of gate insulator engineering. Sections III-C and III-D discuss these two issues in more detail.

The HVOTFT was also tested in extended use for feasibility assessment with V_{DS} held at -400 V, V_G switching between

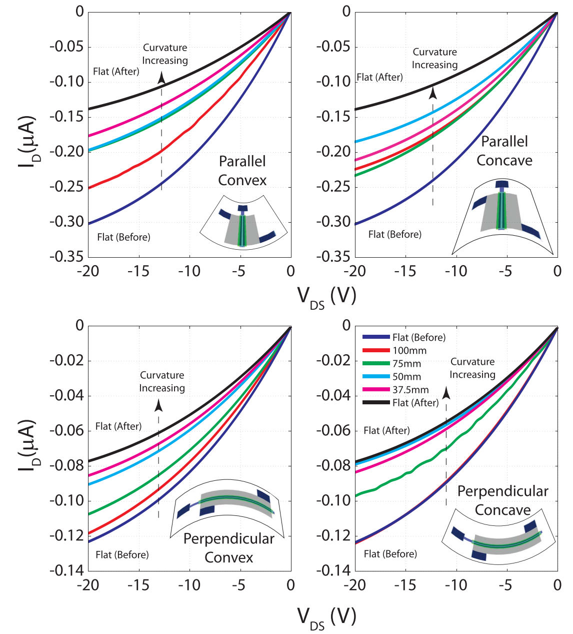

Fig. 7. Comparison of output characteristics for the conventional OTFTs at different radii of curvature. Flexure causes a significant permanent decrease of the drain current. The channel length (L) is 20 μm. The channel width (W) is 500 μm. V_{GS} was kept constant at -20 V.

0 and -20 V every minute, for 3 h, and I_D sampled every 2 s. I_D decreased rapidly during the first cycles of the test, but appears to stabilize over time, as shown in Fig. 6. This behavior suggests that in its current form, the HVOTFT is best suited for applications that require short periods of operation. There is room for improvement regarding μ and $I_{\text{ON}}/I_{\text{OFF}}$ ratio, which is believed to be achievable by optimizing the device architecture and materials processing.

B. Electrical Characterization: Devices Under Flexure

There are reports that show flexure can alter electrical parameters and device performance [12], [13]. To assess the HVOTFT under flexure, both the conventional OTFT and the HVOTFT were fabricated and electrically characterized on a flexible substrate. The OTFT suffered permanent damage from the flexure while the HVOTFTs appeared robust and stable. The difference in performance of the two devices suggests that damage and degradation caused by flexure and/or testing may manifest as electronic defects that act as charge traps, where the high fields in the HVOTFT during operation assist in charge release from the traps.

Flexure was applied to the wafer in two different ways: parallel and perpendicular to the direction of charge flow in the transistor, as shown in Fig. 7. For both cases, the output and transfer characteristics were measured:first with no applied flexure, second with alternating convex and concave curvatures of the same magnitude, and finally with again no applied flexure to assess permanent changes in the electrical characteristics. For both the OTFTs and HVOTFTs, the output and transfer characteristics showed gate control and current saturation under flexure. The radii of curvatures to which the wafers were flexed were ∼100, 75, 50, and 37.5 mm.

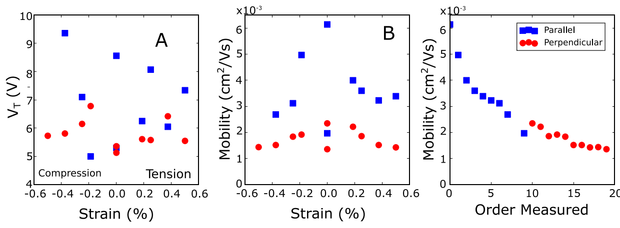

Fig. 8. Comparison of output V_T and μ for the conventional OTFTs at different radii of curvature. A) Flexure causes the V_T to vary randomly. B) Flexure causes μ to decrease with increasing strain. C) Flexure causes a significant permanent decrease in μ.The channel length (L) and width (W) is 20 and 500 μm, respectively. V_T and μ were extracted at $V_{DS} = -20$ V and V_{GS} between -20 and -15 V.

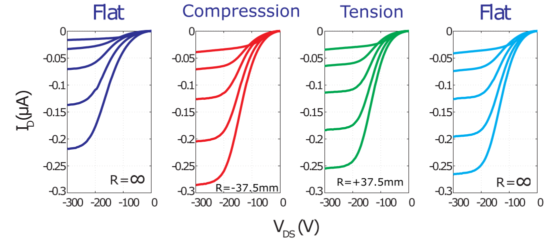

Fig. 9. Comparison of high-voltage output characteristics of HVOTFTs at different radii of curvature under parallel flexure. Flexure changes I–V behavior minimally. The channel length (L) is 10 μm with a 20-μm offset at the drain. The channel width (W) is 250 μm. V_{GS} stepped from 0 to -20 V in -5 V increments.

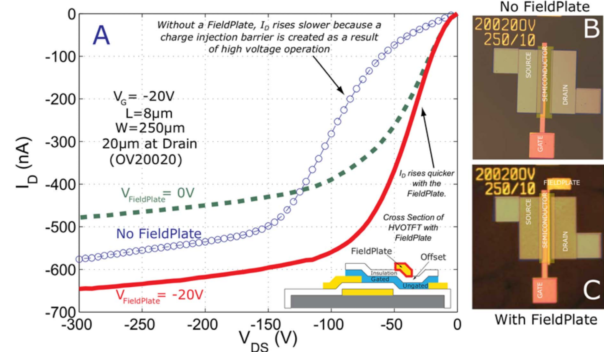

Fig. 10. (A) Addition of field plate reduces V_x similar to the a-Si HVTFT. (B) HVOTFT without a field plate. (C) HVOTFT with a field plate.

For the conventional OTFTs, V_T varied with flexure though no clear trend with strain was observed, as shown in Fig. 8(A). The μ steadily decreased under flexure for both convex and concave and for both parallel and perpendicular orientation with higher variation in the perpendicular case, as shown in Fig. 8(B). It can be concluded that any mechanical stress will degrade device performance where the parallel orientation is most disruptive.

A clear trend were observed with correlating μ with test order, as shown in Fig. 8(C). It should be noted the higher variation in μ was observed in the first few devices tested. Additional tests with a different testing order will confirm if parallel orientation is truly more disruptive than perpendicular orientation or if the devices initially degrade rapidly then stabilize.

For the HVOTFTs, I_D did not change significantly with flexure. As can be seen from Fig. 9, there is a modest increase in I_D during and after flexure, but this change was smaller than the decrease in I_D observed with the conventional OTFTs. This implies that μ and V_T are more stable and recoverable in the HVOTFT compared with the conventional OTFT.

A plausible reason for the degradation of μ in the conventional OTFTs is the creation of point defects due to mechanical failure during flexure in the pentacene [14]. Such defects imply a more disordered thin film, which would consist of more charge traps and charge carrier scattering compared with an unstressed film. Furthermore, the difference in change in μ between the parallel and perpendicular cases can be explained by the orientation of the point defects created due to stress. Applying flexure parallel to the current direction expands defects perpendicular to I_D, while applying flexure perpendicularly expands defects parallel to I_D. Thus, it would be expected that parallel flexure causes a greater reduction in μ than perpendicular flexure, as was observed. Assuming the same defects are created in both the OTFT and HVOTFT under flexure, similar degradation in the mobility for the HVOTFT devices is expected. However, current through the HVOTFT is mediated by Frenkel–Poole conduction [15]–[18] where μ is enhanced by high electric fields. It is plausible that mobility enhancement from the high fields in the HVOTFT are likely compensating for any flexure-induced mobility degradation.

C. High Field Effects: A Barrier to Charge Injection

Shaw *et al.* [19] and Martin *et al.* [2], [20] reported a barrier to charge injection into the gated semiconductor region in the HVTFT at high voltages. This barrier arises from charge traps that are created due to high fringing fields at the transition between the gated and offset regions. They report using a field plate to improve device performance by weakly accumulating charge at the transition of the channel and offset. Biasing the field plate provides more free charges to respond to the large electrostatic fields as opposed to creating trap states. In the case of the HVOTFT, a similar charge injection barrier was observed and was quantified in Fig. 10(A) as V_x, the additional voltage required to inject charge in the presence of such a barrier [19], [20]. Similarly to the Si-based HVTFT, the addition of a field plate for the HVOTFT also reduced V_x, as shown in Fig. 10(A). This indicates that the barrier to charge injection in the HVOTFT may have similar origins to the a-Si case. Additional studies regarding charge trapping and detrapping kinetics would elucidate the exact mechanisms that impede charge injection in the HVOTFT.

D. High Field Effects: Parasitic Space-Charge-Limited Current, Channel Length Modulation

The I–V characteristics of the presented HVOTFTs show what appears to be space-charge-limited currents (SCLCs) and channel length modulation (CLM). There are numerous reports of submicrometer OTFTs suggesting that such high field effects can be treated similar to those found in Si-based submicrometer MOSFETs [21]–[29]. The adjustments to the I–V characteristics by subtracting the drain current induced by SCLC and correcting for CLM suggest that the saturating current conditions are achievable and that the HVOTFT can be modeled with the existing and fundamental FET models.

In short-channel OTFTs and MOSFETs, nonsaturating I_D are known to occur at submicrometer length scales. For the

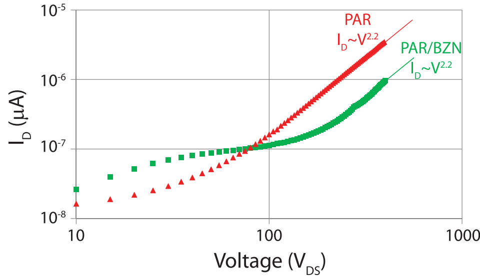

Fig. 11. I_D versus V_{DS} at $V_G = 0$ V shows a quadratic relationship for PAR and PAR/BZN. The quadratic dependence between I_D and V_{DS} is indicative of an SCLC [30]. The channel length (L) is 10 μm with a 20-μm offset at the drain. The channel width (W) is 250 μm.

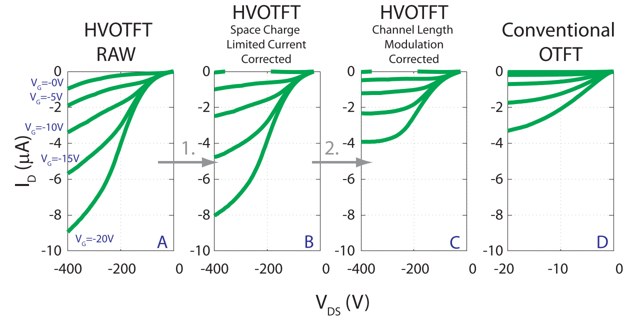

Fig. 12. PAR-/BZN-based HVOTFTs corrected for SCLC and CLM. A) Raw IV Output Characteristic. B) Corrections made for Space Charge Limited Currents. C) Corrections made for Space Charge Limited Currents and Channel Length Modulation. D) Conventional OTFT. The channel length (L) = 10 μm and channel width (W) = 250 μm with a 20-μm offset at the drain, $\lambda^{-1} = V_A + |V_x| = 380$ V.

TABLE II

COMPARISON OF THE PERFORMANCE OF VARIOUS HIGH-VOLTAGE TFTs

Source	Unagami and Kogure [1]	Martin et al. [2]	Karim et al. [3]	This Work
Structure	Offset Drain and Source	Offset Drain	Offset Drain Soft Contact	Offset Drain and Source
Semiconductor	poly-Si	a-Si	a-Si	pentacene
Insulator	SiO_2	SiN	SiN	Various
t_{ox} (nm)	150	300	250	350-500
V_T (V)	2.7	1-2	4.5	-1.5-+5.4
Saturation	No	Yes	Yes	No
Flexible	No	No	No	Yes
Year	1988	1993	2004	2015

presented HVOTFT, the length scales are larger than submicrometer; however, the power supply is scaled up (>200 V) such that the source-to-drain electric field in the semiconductor channel exceeded 0.1 MV/cm. Lee and Gan [30] report SCLC currents in evaporated pentacene films at ~0.1 MV/cm. Therefore, it can be inferred that the physical mechanisms giving rise to current nonsaturation in short-channel OTFTs at lower voltages are also likely active in the presented HVOTFT at high voltages. This current nonsaturation can be seen in Fig. 5(D)–(F), albeit the device gate being able to modulate drain current to a notable extent.

Regarding parasitic SCLC, Tukagoshi *et al.* [27] attributed nonsaturation in submicrometer pentacene-based TFTs to SCLC enhanced by the Frenkel effect [31]. The expression proposed in [27] is [31]

$$J_{\text{SCLC}} = \frac{9}{8}\mu_0 \kappa \epsilon_o \frac{V^2}{L^3}\left(\frac{\rho_f}{\rho_f + \rho_t}\right). \quad (3)$$

Consider I_D versus V_{DS} for an HVOTFT with $V_G = 0$ for the two insulators, as shown in Fig. 11. The relationship between I and V [$\log(I_D)$ versus $\log(V_{DS})$] for each insulator indicates a likely conduction mechanism (~2 for SCLC) [30]. The I–V behavior is quadratic ($\sim V_{DS}^2$) at high voltages for the PAR and PAR-/BZN-based devices ($V_{DS} > 100$ V), indicative of SCLC similar to the that reported in [27] and [30]. However, the SCLC does not appear in O_2 PAR HVOTFT which may be a consequence of the interface states (Q_{it}) that were engineered at the insulator/semiconductor to shift the threshold voltage. Refer to (3), a larger trap density (ρ_t) due to the interface states (Q_{it}) could reduce the SCLC.

The parasitic SCLC were removed by subtracting $V_{GS} = 0$ sweep from the rest of the output characteristics, as shown in Fig. 12(B). However, even accounting for SCLC, there is still no saturation, implying that there is likely another mechanism operating that inhibits current saturation.

CLM has also been reported in a-Si-based HVTFTs in [3] and in organic-based TFTs in [26]. Likewise, by extracting a CLM parameter and accounting for the instability (V_x), the I–V behavior can be corrected, as shown in Fig. 12(C). The following equations are expressions for these corrections:

$$I_{D,\text{corrected}} = \frac{I_{D,\text{measured}} - I_{\text{SCLC,leakage}}}{(1 + \lambda V_{\text{DS}})} \quad (4)$$

$$\lambda^{-1} = V_A + |V_x|. \quad (5)$$

In addition to CLM in the conventional OTFTs, there is a positive V_T shift for higher values of V_{DS} from which it was extracted, though not shown in this paper. This is similar to drain-induced barrier lowering in Si-based MOSFETs. As a result of the offsets in the HVOTFT, V_T cannot be extracted without a complete understanding of the conduction mechanisms operative at the transition from gated to ungated regions. Haddock *et al.* [26] report a similar V_T instability in short-channel OTFTs, suggesting that it is also possibly operative in HVOTFTs. This is the subject of future investigations.

IV. CONCLUSION

Pentacene has been shown to be a viable semiconductor for HVOTFTs on flexible substrates. This is a notable demonstration as other instances of HVTFTs use a Si-based semiconductor. The HVOTFTs were fabricated with three different gate insulators to explore how electrical parameters change with the gate insulator. While all insulators were viable for implementation in HVOTFTs, the impact of the gate insulator performance was obscured by current nonsaturation due to high electrics fields. Under flexure, both the HVOTFTs and OTFTs displayed clear gate control. The electrical characteristics of the HVOTFTs at high V_{DS} reveal: 1) a barrier to charge injection (V_x) into the gated channel and 2) a nonsaturating I_D. The barrier to charge injection into the gated channel was suppressed with the addition of a field plate. The nonsaturating I_D at high V_{DS} was believed to be caused by a parasitic SCLC and a behavior similar to CLM. By applying

numerical corrections derived from FET models developed for Si-based short-channel devices, the output characteristics of the HVOTFT were more ideal. Further evaluating the influence of different device geometries, gate insulator materials, and sized offsets would help elucidate the exact nature of these high field effects and determine how effectively they can be mitigated and controlled.

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