High-Q Inductors on Locally Semi-Insulated Si Substrate by Helium-3 Bombardment for RF CMOS Integrated Circuits

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***Abstract*— A helium-3 ion bombardment technique is proposed to realize high-Q inductors by creating locally semi-insulating substrate areas. A dose of 1.0×10^{13} cm^{-2} helium-3 increases a Si substrate resistivity from 4 $\Omega \cdot$ cm to above 1 k$\Omega \cdot$ cm, which improves the quality factor of a 2-nH inductor with a 140-μm diameter by 38% ($Q = 16.3$). An aluminum mask is used for covering active areas, and at least 15-μm distance from the mask edge is required to avoid the p-n junction leakage. The proposed technique is applied to an 8-GHz oscillator, and an 8.5 dB improvement of the measured phase noise has been achieved.**

***Index Terms*— CMOS, helium-3 bombardment, high-Q inductor.**

I. Introduction

THE on-chip spiral inductor is one of the most important components in RF CMOS circuits. It becomes indispensable for RF circuits, such as voltage controlled oscillators (VCOs), low noise amplifiers, and power amplifiers. On-chip spiral inductors can realize high integration without need for 50-Ω interface, which is usually required by off-chip inductors. However, RF circuits have suffered from the poor performance of on-chip inductors due to several reasons. The first one results from large series resistance of thin metal lines, which become thinner with CMOS process scaling down. Another one is low substrate resistivity. A low substrate resistivity is commonly used for protection against latch-up of digital circuits. The low resistivity causes higher substrate loss and decreases the quality factor of inductors. For the former reason, thick metals [1]–[3] can be used to decrease the metal loss. For the latter one, the proton bombardment [4]–[6] and the use of postpassivation interconnect (PPI) [7]–[10] have been proposed for realizing high-Q inductors by decrease the substrate loss. However, the PPI inductor cannot be used for high-frequency applications due to the large parasitics of the high aspect ratio vias, which are used to connect PPI inductors and circuits, resulting in a low self-resonance frequency of 16 GHz [7]. Furthermore, this method is limited to wafer-level packaging. The bombardment technique can decrease substrate loss by creating locally semi-insulating substrate areas with substrate resistivity [5]. However, the proton bombardment [4]–[6] requires an enormous dose of 10^{15} cm^{-2} to realize a resistivity of more than 10^3 $\Omega \cdot$ cm for an originally 15-$\Omega \cdot$ cm substrate [5], which results in less reliability and high process cost. Other methods such as silicon on insulator (SOI) technique can also improve the quality factor [11]. However, it is reported that SOI substrates are of high cost and amount to about 25% of the total wafer cost [12].

In [13], a helium-3 ion bombardment technique is proposed. Compared with proton, helium-3 ion has higher irradiation efficiency, higher throughput, and less lateral scattering. Therefore, helium-3 bombardment needs less dose and lower process cost, and realizes higher reliability. To realize a 10^3 $\Omega \cdot$ cm resistivity, the required irradiation time for helium-3 is reduced from 3 h for proton to 3.7 min, which saves the product cost about 97%. Table I summarizes several methods to realize high-Q on-chip inductors. The effect of helium-3 bombardment is also verified by an on-chip dipole antenna [14].

TABLE I
SUMMARY OF METHODS TO IMPROVE THE QUALITY FACTOR OF ON-CHIP INDUCTORS

Method	Reliability	Cost	Q improvement
Thick Metal [1]	Good	Fair	Good (thickness limitation)
PPI [7]	Good	High	Good (package limitation)
Silicon on Insulator [11]	Good	Very high	Fair (failed at high frequency)
Proton [5]	Poor	High	Good
Helium-3 [13]	Good	Fair	Good

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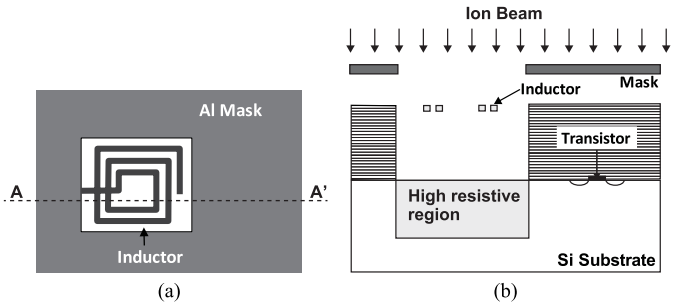

Fig. 1. Helium-3 bombardment process. A 0.5-mm-thick aluminum mask is used to cover active areas from the irradiation. (a) Top view. (b) Cross view at A–A′.

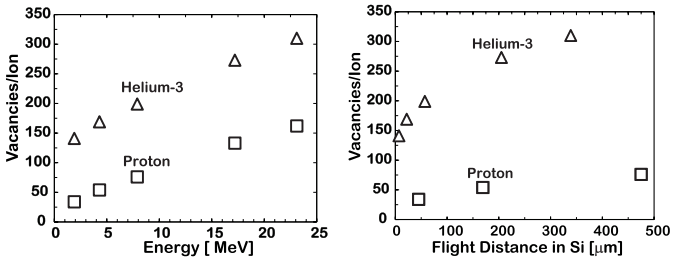

Fig. 2. Calculation results by using an ion-implantation simulator called TRIM calculating 10 000 times with 95% ion falling within the range. (a) Vacancy generation with ion energy. (b) Vacancy generation with flight distance in silicon.

This paper is organized as follows. Detailed helium-3 bombardment technique is discussed in Section II. Section III shows the experimental results. The conclusion is given in Section IV.

II. Helium—Bombardment

Fig. 1 shows a simplified process of helium-3 bombardment technique. A 0.5-mm-thick aluminum mask is used to protect transistors, and the window in the aluminum mask is opened for bombardment at inductor area. Helium-3 ion beam is accelerated by a cyclotron and irradiated from the top of the chip. The cyclotron has a maximum beam current of 10 μA and can accelerate helium-3 ion with an energy up to 24 MeV. The distance between beam scanning magnet to wafer is about 8 m, and the beam cut slit diameter is about 30 cm. Therefore, the incident angle is less than 1.07°. After helium-3 bombardment, a high-resistivity region is created under the inductor in silicon substrate, while the substrate resistivity keeps the same under active devices.

The increasing of substrate resistivity is due to charge trappings created by the irradiation and Coulomb scattering of the charged traps [4], [5]. As mentioned previously, helium-3 has higher irradiation efficiency and less lateral scattering. The calculated vacancy generation per ion is shown in Fig. 2(a). At an energy of 17.2 MeV, the vacancy generation ability of helium-3 is about 273 vacancies/ion, while that of proton is only 133 vacancies/ion. The calculated vacancy generation per ion at the same flight distance in silicon substrate is compared in Fig. 2(b). The value of helium-3 is 5–6 times larger than that of proton at the same flight distance in silicon substrate. Both are calculated using an ion-implantation simulator called transport of ions in matter (TRIM), which calculates 10 000 times with 95% ion falling within the range [15].

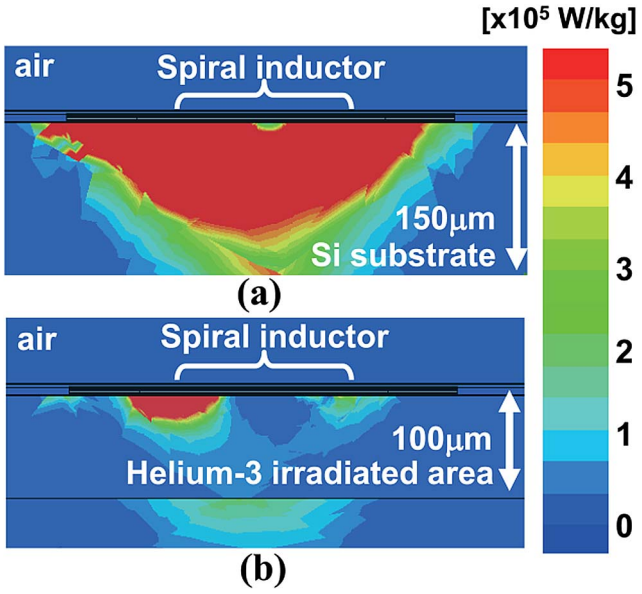

Fig. 3. EM simulation results of specific absorption rate (a) without and (b) w 100-μm-depth helium-3 bombardment.

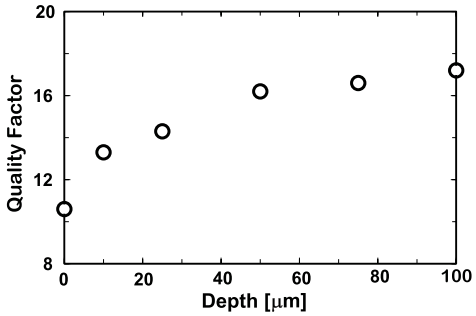

Fig. 4. EM simulated quality factor at 8 GHz with respect to irradiated-region depth.

To investigate the effect of helium-3 bombardment, an on-chip spiral inductor is simulated with and without helium-3 bombardment using an electromagnetic (EM) simulator. Fig. 3 shows the simulated distribution of the power to weight ratio for a 140-μm-diameter spiral inductor. The open deembedding method is implemented to remove the parasitics of the pads. A 100-μm-depth helium-3 bombardment region with a 1-k$\Omega \cdot$ cm resistivity is assumed under the inductor. The silicon substrate thickness is about 150 μm. As shown in Fig. 3, the loss due to eddy current in silicon substrate is drastically reduced with helium-3 bombardment. The simulated quality factor of the inductor with different irradiation-region thickness is also shown in Fig. 4. The quality factor peak value increases as the irradiation-region thickness increases.

III. Experimental Results

A. Substrate Resistivity

The measured resistivity of bare wafers is shown in Fig. 5. A Czochralski N-type wafer with 1×10^{15} atm/cm^3 boron dopant is utilized for the test. A spreading resistance profiler

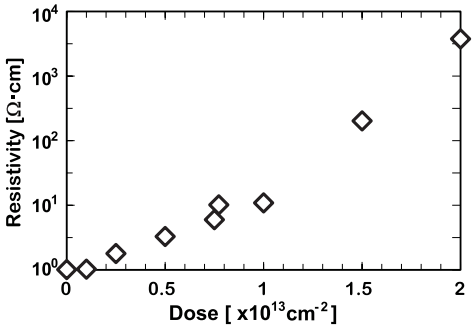

Fig. 5. Measured substrate resistivity with dose amount.

TABLE II
CONDITIONS OF THE IRRADIATION IN FIG. 6. EACH PEAK CORRESPONDS TO THE TARGET IRRADIATION DEPTH

Condition	Total time [s]	Target irradiation depth [μm]	Total dose [cm^{-2}]
#1	444	15, 30	2.0×10^{13}
#2	332	15, 30, 45	1.5×10^{13}
#3	66	15, 30, 45	3.0×10^{12}

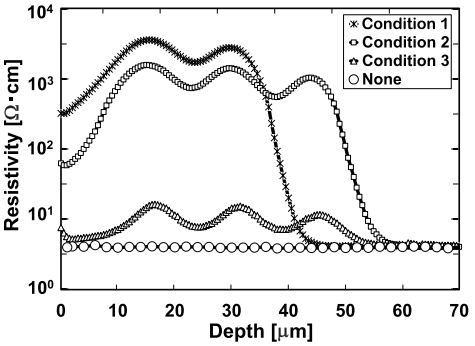

Fig. 6. Substrate resistivity variation as a function of depth from the surface of Si wafer with various conditions listed in Table II.

method is used to measure the resistivity of the silicon substrate. A helium-3 dose of 1×10^{13} cm^{-2} increases a Si substrate resistivity from 4 $\Omega \cdot$ cm to 1 k$\Omega \cdot$ cm, while for proton, the required dose is above 1×10^{15} cm^{-2} for the same type wafer [5]. Compared with proton, the required irradiation time is reduced from 3 h to 3.7 min, which saves the product cost about 97%. Fig. 6 shows the measured resistivity profile. The bombardment conditions have been summarized in Table II. For condition #1, a helium-3 dose of 1×10^{13} cm^{-2} is irradiated twice into the target depth of 15 and 30 μm, which corresponds to the two peaks in Fig. 6. The effect of annealing is also studied by annealing the wafer at 200 °C and 400 °C for 1 h at condition #1. The results are shown in Fig. 7. The decreasing of resistivity is small at the target depth, while it is evident at the transit area.

B. Inductor

1) Quality Factor Improvement: Two-port inductors are implemented in a 180-nm CMOS process with six metal layers. Top metal layer is used to implement the inductors. The S-parameters are measured for all inductors and open circuits. Shunt parasitic capacitance of pads are deembedded

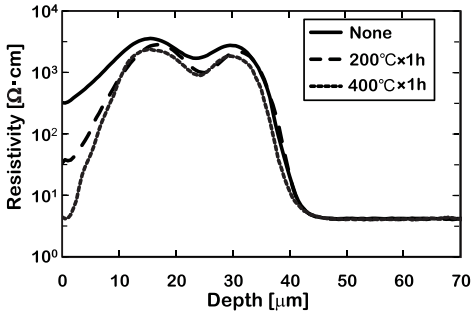

Fig. 7. Irradiated substrate resistivity before and after annealing at condition #1 in Table II.

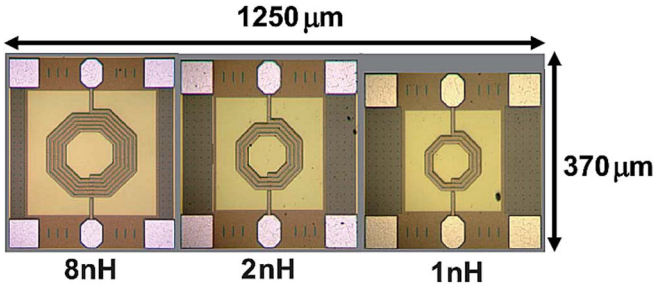

Fig. 8. Micrographs of spiral inductors fabricated by a commercial 180-nm CMOS process with six aluminum layers.

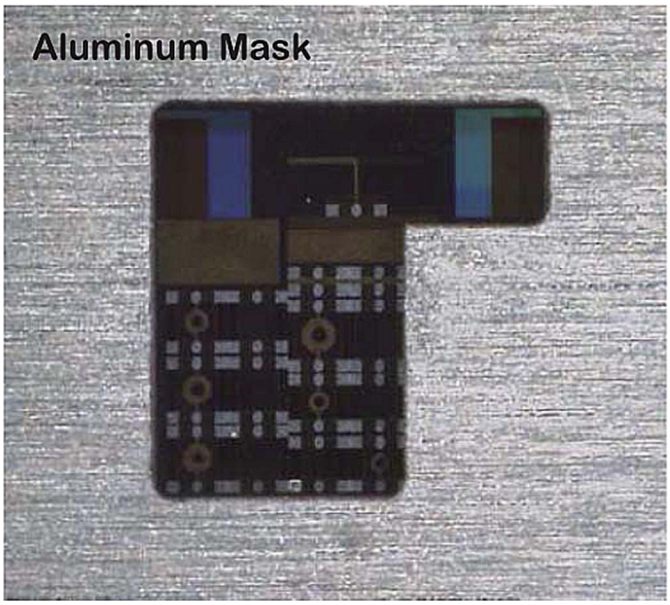

Fig. 9. Micrograph for the whole chip with aluminum mask.

using open deembedding method. The chip photos for the 8, 2, and 1-nH inductors are shown in Fig. 8. The micrograph for the whole chip and aluminum mask for helium-3 irradiation is shown in Fig. 9. The window is opened over inductor area.

Fig. 10 shows the measured inductances and quality factors with and without helium-3 bombardment (condition #2). More than 36% improvement ratios for quality factor have been realized for all inductors. The peak values of Q are shifted to higher frequency, while the self-resonance frequency keeps

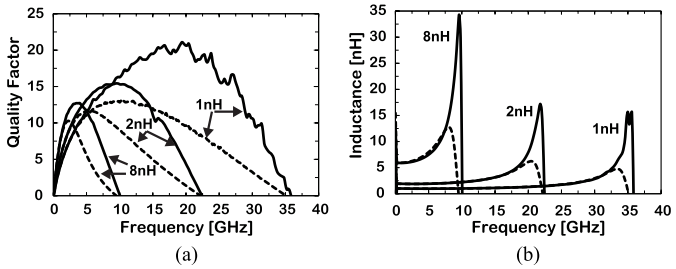

Fig. 10. Measured inductance and quality factor with (solid lines) and without (dotted lines) helium-3 bombardment. (a) Quality factor. (b) Inductance.

TABLE III
INDUCTOR QUALITY FACTOR IMPROVEMENT

Inductor	Q (w/o helium-3)	Q (w/ helium-3)	Improvement Ratio
1 nH	13.0	20.0	54%
2 nH	11.6	16.3	38%
8 nH	10.3	14.1	36%

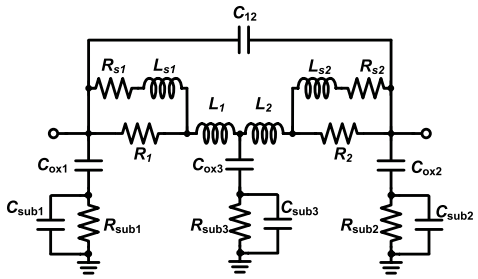

Fig. 11. Equivalent circuit of inductors. Parameters, $R_{\rm sub1}$, $R_{\rm sub2}$, and $R_{\rm sub3}$, characterize the influence of the substrate resistivity.

the same. The inductance has little change for each inductor. The performance are summarized in Table III.

2) Inductor Modeling: The inductors are modeled after helium-3 bombardment. The two-π type equivalent circuit of two-port inductors is shown in Fig. 11, where L_1 and L_2 are the serial inductance, R_1 and R_2 are the serial resistance, $L_{\rm sx}$ and $R_{\rm sx}$ represent the inductance and resistance due to skin effect, respectively, C_{12} is the coupling capacitance between two ports, $C_{\rm ox1}$, $C_{\rm ox2}$, and $C_{\rm ox3}$ are the oxide capacitance between the spiral and substrate, and $R_{\rm subx}$ and $C_{\rm subx}$ are the silicon substrate resistance and capacitance, respectively. The parameters are determined using the S-parameter fitting technique. The fitting results are illustrated in Fig. 12. The model parameters are shown in Table IV. The bombardment effect are reflected by substrate-related parameters, $R_{\rm sub1}$, $R_{\rm sub2}$, and $R_{\rm sub3}$.

C. Quality Assessment

1) Metal Line: Fig. 13 shows a micrograph of meander-line test element group (TEG) for evaluating metal reliability with/without the bombardment. The lengths of the bended metal 1 and 6 lines are 151 and 15.3 mm, respectively. Both have its minimum width according to design rules. DC pads are used for the on-chip measurement. For each metal line, a force and sense pad are used to deembed the resistance

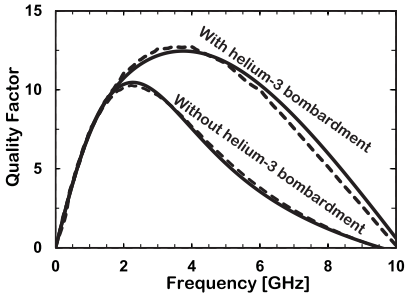

Fig. 12. Comparison of quality factor of the 8-nH inductor obtained from measurement (dotted lines) and model (solid lines) of the case with/without the helium-3 bombardment.

TABLE IV
EXTRACTED PARAMETERS FOR THE EQUIVALENT CIRCUIT IN FIG. 11

Parameter	Without helium-3	With helium-3
L_1, L_2 [nH]	2.87	
R_1, R_2 [Ω]	4.19	
L_{s1}, L_{s2} [nH]	0.56	
R_{s1}, R_{s2} [Ω]	4.73	
C_{12} [fF]	36.40	
$C_{\rm ox1}$ [fF]	23.40	
$C_{\rm ox2}$ [fF]	24.10	
$C_{\rm ox3}$ [fF]	47.50	
$R_{\rm sub1}$ [kΩ]	1.00	7.60
$R_{\rm sub2}$ [kΩ]	3.04	16.50
$R_{\rm sub3}$ [kΩ]	0.75	5.21
$C_{\rm sub1}$ [fF]	5.00	
$C_{\rm sub2}$ [fF]	2.12	
$C_{\rm sub3}$ [fF]	7.12	

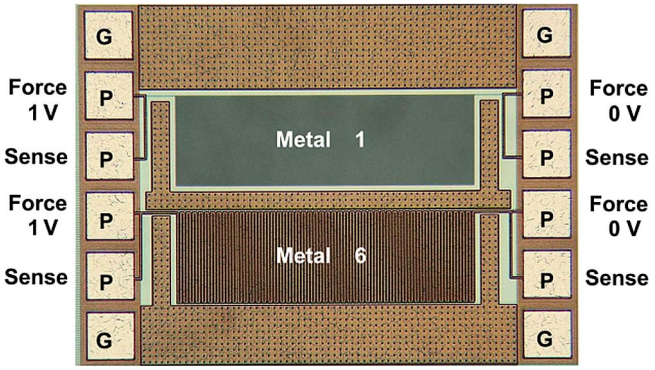

Fig. 13. TEG for evaluating metal resistance with/without the bombardment (not the same chip).

of lead lines. The resistances of metals 1 and 6 become 51.2 kΩ (+0.9%) and 35.5 kΩ (−0.5%), respectively, which are less than the process variation.

2) Transistor: Fig. 14 shows the TEG structure for evaluating the p-n junction leakage. Transistors are arranged symmetrically with a 10-μm pitch (A1–A5 and B1–B5). The width of the irradiated area is 294 μm, which covers transistor A1 and B1 by 5 μm. The distance of transistors at A1 (B1)–A5 (B5) to the edge of the irradiated area are −5, 5, 15, 25, and 35 μm, respectively. Therefore, the transistors at A1 and B1 are exposed, while the others are covered by the aluminum mask. Ground-signal-signal-ground RF pads are used for on-chip measurement since RF probes have less leakage. For the same reason, RF cables are used

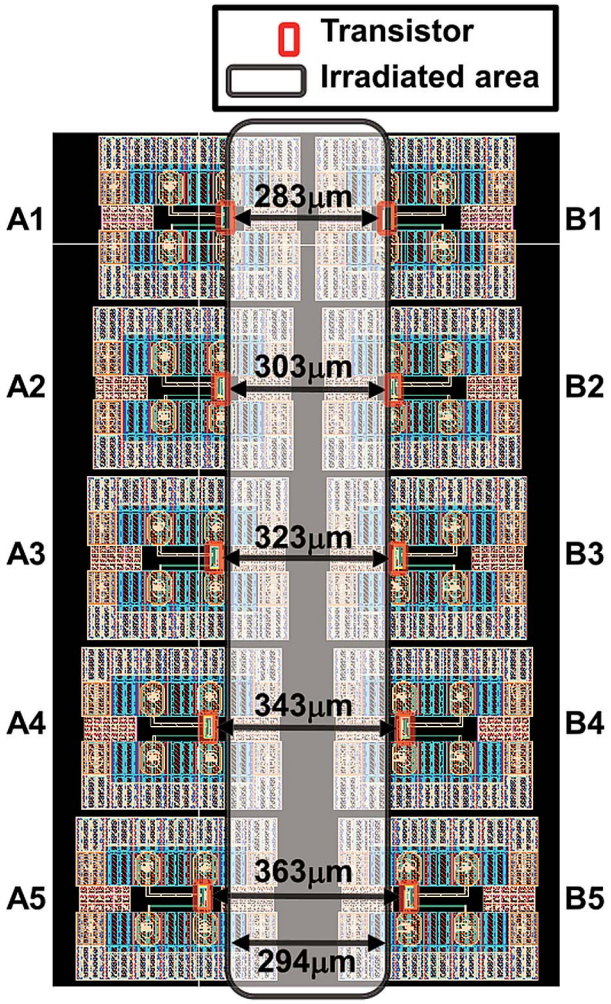

Fig. 14. TEG structure for evaluating transistor damage from the bombardment.

instead of dc cables. Agilent 4157B Modular Semiconductor Parameter Analyzer is used to measure the dc, which has a resolution of 10 fA with medium-power source/monitor units.

Fig. 15 shows I–V characteristics after the bombardment of condition #2 in Table II. Fig. 16 shows the leakage current as a function of distance from the mask edge before/after the bombardment. Before irradiation, the leakage current for all transistors are around 10^{-10} A, while after irradiation, the leakage current of the transistor near the mask edge increases to as large as 10^{-5} A. From the measured results, when the distance is larger than 15 μm, the leakage current of transistors on both sides does not increase, which indicate that the irradiation has no effect on the transistors. Therefore, a distance of at least 15 μm is the required margin for transistors including the mask alignment, while 50 μm is required in the proton bombardment [6] due to the enormous dose and lateral scattering.

D. Phase Noise Improvement

An 8-GHz tail-feedback VCO is implemented in the same 180-nm CMOS technology. Tail-feedback VCO is proposed in [16] and [17]. This kind of VCOs modulate the tail current of differential nMOS VCOs using a signal feedback from the

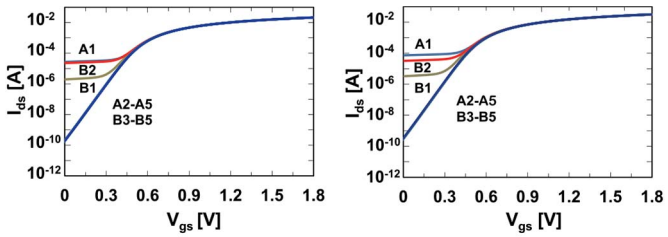

Fig. 15. I–V curve after the bombardment. Condition #2 in Table II is applied. A1–A5 and B1–B5 correspond to the position of transistors in Fig. 14. (a) Transistor width of 40 μm. (b) Transistor width of 60 μm.

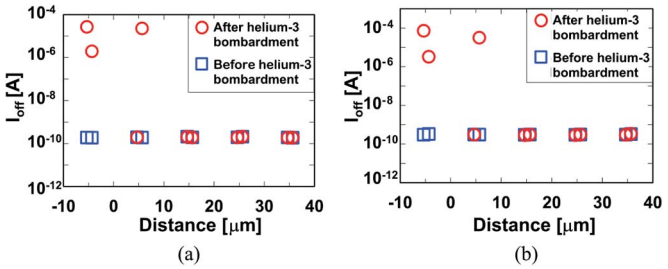

Fig. 16. Leakage current at $V_{gs} = 0$ V as a function of distance from the mask edge. The same transistors are measured before/after the bombardment. A design margin of at least 15 μm is required including mask alignment. (a) Transistor width of 40 μm. (b) Transistor width of 60 μm.

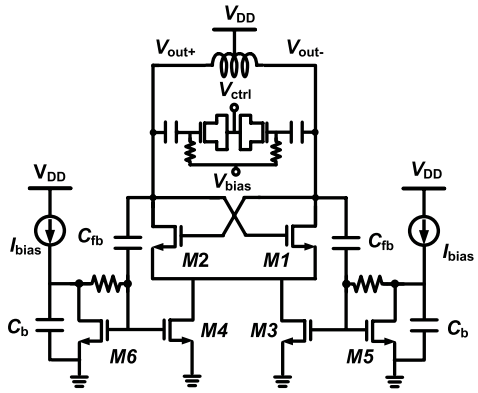

Fig. 17. Circuit schematic of tail-feedback VCO, designed for 8-GHz oscillation. A 1-nH inductor is used.

TABLE V
VCO PERFORMANCE SUMMARY

	without helium-3	with helium-3
V_{dd} (V)	1	1
P_{dc} (mW)	4.83	4.75
PN@1 MHz off-set (dBc/Hz)	-94	-102.5
f_{osc} (MHz)	8027	8044

output node, which leads to a better phase noise performance compared with traditional nMOS VCO. Fig. 17 shows the circuit schematic and Fig. 18 shows the micrograph with irradiated area. The core area of the VCO is 0.13 mm^2. The performance of the VCO with and without helium-3 bombardment is summarized in Table V. Fig. 19 shows the measured phase noise with/without the bombardment (condition #2). The phase noise without bombardment is -94.0 dBc/Hz at 1-MHz offset, while -102.5 dBc/Hz is achieved after the bombardment at the same 4.8 mW power consumption from

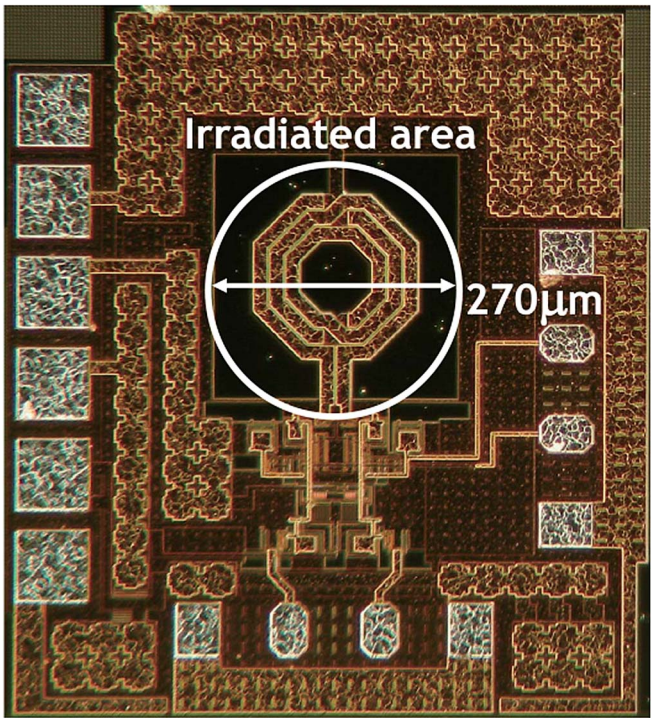

Fig. 18. VCO chip photo with the irradiated area (condition #2). The active area covered by the aluminum mask.

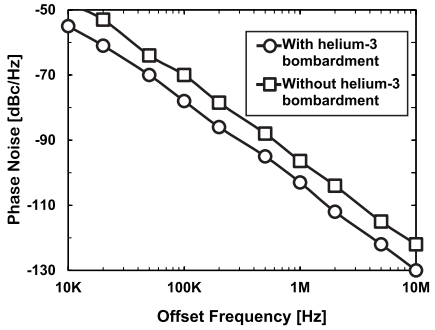

Fig. 19. Measured phase noise with/without the bombardment.

a 1 V supply voltage. The power consumption of 18.0 mW is required to achieve the same phase noise performance without the bombardment. The oscillation frequency is slightly shifted to high frequency due to the inductance decreasing after helium-3 bombardment, as shown in Fig. 10.

IV. Conclusion

In this paper, we have demonstrated a helium-3 ion bombardment technique to realize high-Q inductors by creating locally semi-insulating substrate areas. A dose of 1.0×10^{13} cm^{-2} helium-3 increases a silicon substrate resistivity from 4 $\Omega \cdot$ cm to above 1 k$\Omega \cdot$ cm, while the required proton dose is 1.0×10^{15} cm^{-2} for the same type silicon substrate. The product cost is successfully reduced by about 97%. The quality factor of a 2-nH inductor with a 140-μm diameter is improved by 38% ($Q = 16.3$). The resistance variation of metal lines due to helium-3 ion bombardment are less than the process variation. To avoid p-n junction leakage, the required placement margin from the mask edge is reduced from 50 to 15 μm compared with the proton bombardment. The proposed technique is applied to an 8-GHz oscillator, and an 8.5-dB improvement of the measured phase noise has been achieved.

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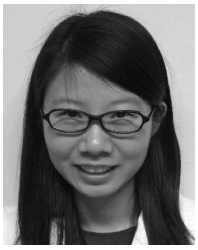

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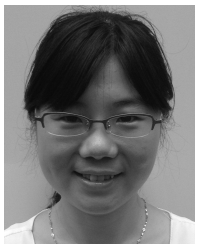

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