Zigzag-Shaped Coil Array Structure for Wireless Chip-to-Chip Communication Applications

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***Abstract*— In this paper, we propose a zigzag-shaped coil array structure for wireless chip-to-chip communication. The proposed structure is designed for high-speed memory, which requires a pad number on the order of tens. First, a general coil array is investigated with respect to undesired coupling between adjacent coils. We also investigated a coil array for which shielding patterns are inserted between adjacent coils to reduce cross-talk problems. To solve the cross-talk and chip area problems associated with coil arrays, a zigzag pattern is proposed. Additionally, a layout technique for the circuit block of the memory transceiver that is connected to the coil array is proposed to minimize the total chip size. With the experimental results, the feasibility of the proposed zigzag-shaped coil array is successfully demonstrated.**

***Index Terms*— 3-D semiconductor, coil array, cross-talk, magnetic coupling, wireless chip-to-chip (WCC) communication.**

I. Introduction

THREE-DIMENSIONAL (3-D) semiconductors are considered as the next generation of semiconductor technology. The 3-D semiconductor resolves the problems of typical 2-D semiconductor technologies, such as speed limits and bulky sizes. Fig. 1 shows a conceptual diagram of the 2-D semiconductor technology. 3-D semiconductor technologies include multichip packaging (MCP), through-silicon via (TSV), and wireless chip-to-chip (WCC) technologies [1]–[6]. In particular, the WCC technology uses wireless communication, unlike other 3-D and 2-D semiconductor technologies which use wire-based forms of communication such as bonder-wires, via-holes, and metal lines on a printed-circuit board (PCB) [7]–[9]. The WCC technologies can therefore obtain high-speed data communication.

In [10], the potential of WCC technologies was successfully demonstrated. However, because the communication method differs from other technologies, there are various design issues that must be addressed before WCC technologies can be used in commercial digital and analog ICs. Fig. 2 shows a conceptual diagram of WCC technology. The coil for wireless communication is one of the key components in WCC technology [11]. The coil structure determines the operating distance between the chips. The loss induced by the coil must therefore be minimized to increase the distance. Additionally, research focused on minimizing the size of the coil is required to adapt this technology to commercial digital and analog ICs. Although a merged-type coil proposed in [10] improved the wireless communication quality and chip area, cross-talk between adjacent coils located in the same IC remains a critical issue that must be overcome before the commercialization of WCC technology can be realized. The cross-talk problem degrades the communication quality and transmitted power from the coil because the transmitted power is coupled with undesired adjacent coils [12].

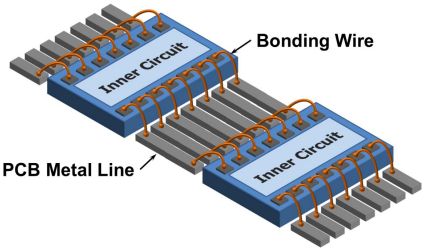

Fig. 1. Conceptual diagram of 2-D semiconductor technology.

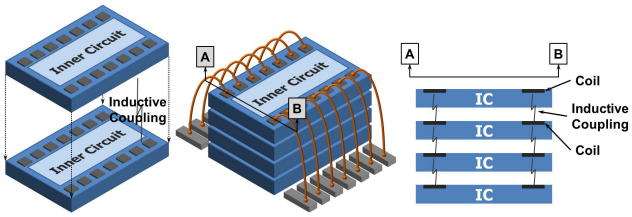

Fig. 2. Conceptual diagram of WCC communication [10].

However, there are no earlier works related to the cross-talk problems of coil arrays with regard to WCC technology. In this paper, we investigate a coil array structure for WCC technology. First, we consider the undesired coupling in a typical coil array. To reduce the undesired coupling between adjacent coils located in the same chip area, shielding patterns between the adjacent coils are inserted. For a coil array with shielding patterns, the increment of the chip area and the level of cross-talk are investigated. Finally, we propose a zigzag-shaped coil array structure to minimize the cross-talk problems

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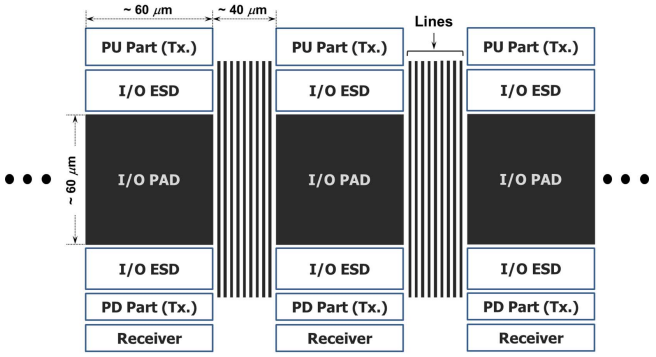


Fig. 3. Conceptual diagram of I/O layout.

and the total chip size. Additionally, a layout technique for the transceiver circuits is proposed to optimize the zigzag-shaped coil array structure.

II. Typical Coil Array Structure

In general, an integrated circuit (IC) has several input/output (IO), ground, and power supply pads. In particular, digital ICs such as DDR3 memory and CPUs have a pad number on the order of tens for the various digital functions carried out by them. Fig. 3 shows a simplified layout of a typical commercial memory IC that is designed for 2-D semiconductor, MCP, and TSV technologies. In Fig. 3, we show the transceiver part and the I/O pad. The transceiver part consists of I/O ESD protection devices, a receiver, and a transmitter. The transmitter is decomposed into a pullup (PU) part and a pulldown (PD) part. The PU and PD parts, respectively, serve as the main driver of the transmitter and the bias circuit of the buffer of the receiver. The PU and PD parts are composed of pMOS and nMOS components, respectively. The PU part is therefore larger than the PD part. In general, the pad size is approximately $60 \times 60\ \mu\text{m}^2$ and the space between adjacent pads is nearly 40 μm. Various lines for signals, power, and interconnections between the PU and PD parts are located in the space between the pads (as shown in Fig. 3).

Accordingly, for successful WCC technology, research on the coil array structure is required. The coil in WCC technology assumes the role of the pad in the 2-D semiconductor, MCP, and TSV technologies. Although WCC communication was successfully demonstrated using a single coil and a transceiver circuit in [6], study of the coil array structure is essential before commercial digital and analog ICs can be realized. Various problems that do not arise in the single coil and transceiver circuit occur in the coil array structure. For example, cross-talk between adjacent coils located in the same chip area is a typical problem that arises in coil array structures as components of WCC technology. One simple solution capable of mitigating the cross-talk problem is to increase the distance between adjacent coils located in the same ICs. However, increasing the distance leads to an increased overall chip size and thus increases the unit cost of production. The cross-talk therefore exists in a tradeoff relationship with the chip area.

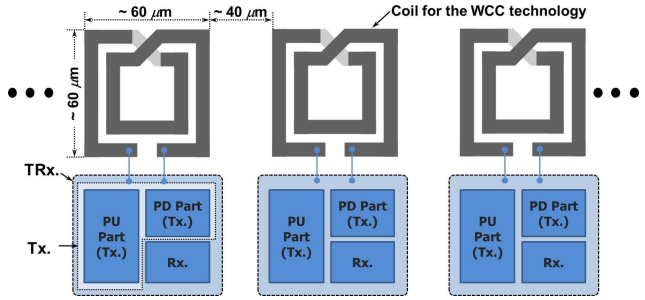


Fig. 4. Typical coil array structure.

A. Simple Array Structure

Although there are no previous works related to coil array structures for WCC technology, a simple coil array structure can be regarded as a typical structure of the type used in applications of WCC technology. A diagram of a simple coil array structure is shown in Fig. 4. In the type of IC used with WCC technology, the circuit blocks of the transceiver must be located on the same side of the coil because the interconnection between the coil and the transceiver is determined by the location of the ports of the coil (as shown in Fig. 4). In this paper, we assume that the unit coil for the coil array is designed using a differential structure [13]. One of the advantages of WCC technology is that I/O ESD protection devices, which are essential components in other technologies, are not required because the I/O of the transceiver is not connected to the PCB lines by bonding wire in WCC technology. The overall area for the transceiver in WCC technology is therefore smaller than that of other technologies.

However, cross-talk in the form of undesired magnetic coupling between adjacent coils degrades the transmitted and received power through the coil and thus the quality of WCC communication. A simple solution which can be applied to the cross-talk problem of a typical coil array structure is to increase the spaces between adjacent coils. However, this requires additional chip area and thus raises the unit cost of production.

B. Array Structure With a Shielding Pattern

To mitigate the cross-talk problems arising in a typical array structure, we can consider the strategy of inserting a shielding pattern between adjacent coils (as shown in Fig. 5) [14], [15]. In general, the shielding pattern is composed entirely of metal layers, from the bottom to the top metal layers. The shielding pattern is connected to the ground or to power lines. The parasitic resistance induced by the metal line of the shielding pattern determines the degree to which cross-talk is suppressed. To minimize the resistance, a large metal width of the shielding pattern is required. However, additional space between adjacent coils is required for the shielding pattern, which increases the overall chip area.

III. Proposed Zigzag-Shaped Coil Array for WCC Technology

Fig. 6 shows the proposed zigzag-shaped coil-array for WCC technology. The layout of the coil and the transceiver

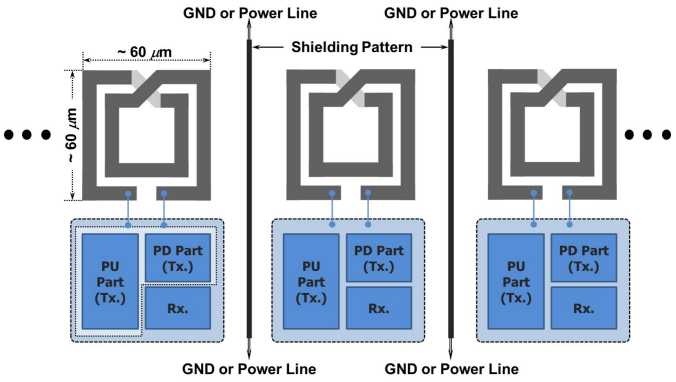


Fig. 5. Coil array structure with a shielding pattern.

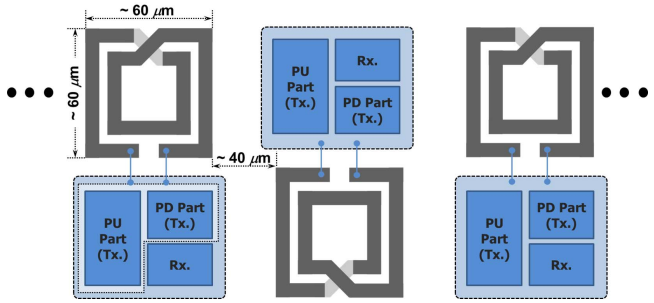


Fig. 6. Proposed zigzag-shaped coil array for WCC technology.

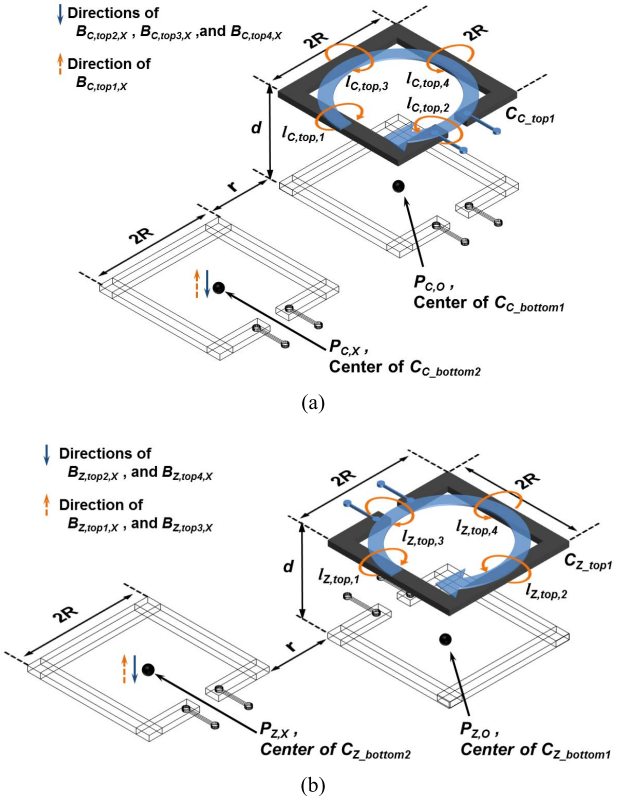


Fig. 7. Simplified diagrams of the numerical analysis. (a) Typical structure. (b) Zigzag structure.

circuit is flipped compared with the adjacent coils and transceiver circuits (as shown in Fig. 6). Accordingly, the distance between the adjacent coils is maximized compared with the other arrays shown in Figs. 4 and 5. The magnetic coupling between adjacent coils is minimized compared with the other coil arrays because the magnetic coupling is in inverse proportion to the distance between two coils. The cross-talk can then also be minimized. Although the distance between adjacent coils is maximized, additional chip area is unnecessary for the zigzag-shaped coil array, unlike for other coil arrays with shielding patterns.

Fig. 7 shows simplified diagrams of the typical and the zigzag structures for a numerical analysis. For the sake of the simplicity of the analysis, we assumed that the number of turns of the unit is one and defined the term of the desired magnetic coupling as the magnetic flux density, $\boldsymbol{B}_{C,\text{Desired}}$ (or $\boldsymbol{B}_{Z,\text{Desired}}$), at $P_{C,O}$ (or $P_{Z,O}$) with C_{C_top1} (or C_{Z_top1}) carrying direct current of I. Similarly, we defined the term of the undesired magnetic coupling as the magnetic flux density, $\boldsymbol{B}_{C,\text{Undesired}}$ (or $\boldsymbol{B}_{Z,\text{Undesired}}$), at $P_{C,X}$ (or $P_{Z,X}$) with C_{C_top1} (or C_{Z_top1}) carrying direct current of I [as shown in Fig. 7(a) and (b)].

To calculate $B_{C,\text{Desired}}$, $B_{C,\text{Undesired}}$, $B_{Z,\text{Desired}}$, and $B_{Z,\text{Undesired}}$, we initially considered the magnetic flux density, B, at a point located at a distance a from a straight wire of length $2R$ (as shown in Fig. 8). The magnetic flux density, B, at this point can then be calculated as follows:

$$B = \frac{\mu_0 I_{\text{EFF}} L}{2\pi a\sqrt{a^2 + L^2}} \tag{1}$$

where μ_0 and I_{EFF} are the permeability and the current of the effective single side of the unit coil, respectively. Given that L and I_{EFF} can be calculated as $R\cos\theta$ and $I\cos\theta$, respectively, and because $\cos\theta$ equals b/a, $\boldsymbol{B}$ of (1) can be expressed with R, a, and b as follows:

$$B = \frac{\mu_0 (I\cos\theta)(R\cos\theta)}{2\pi a\sqrt{a^2 + (R\cos\theta)^2}} = \frac{\mu_0 I}{2\pi}\frac{1}{\frac{a^2}{b}\sqrt{1 + \frac{a^4}{R^2 b^2}}}. \tag{2}$$

By applying (2), $\boldsymbol{B}_{C,\text{Desired}}$, $\boldsymbol{B}_{C,\text{Undesired}}$, $\boldsymbol{B}_{Z,\text{Desired}}$, and $\boldsymbol{B}_{Z,\text{Undesired}}$ of Fig. 7 are calculated as follows:

$$\begin{aligned} B_{Z,\text{Desired}}(C_{Z,top1} \rightarrow P_{Z,O}) &= B_{C,\text{Desired}}(C_{C,top1} \rightarrow P_{C,O}) \\ &= 4 \times \frac{\mu_0 I}{2\pi}\frac{1}{\sqrt{(R^2 + d^2)}\sqrt{1 + \dfrac{R^2 + d^2}{R^2}}} \\ &= \frac{2\mu_0 I R}{\pi\sqrt{(R^2 + d^2)(2R^2 + d^2)}} \end{aligned} \tag{3}$$

$$\begin{aligned} |B_{C,\text{Undesired}}| &= |B_{C,\text{top1},X} - B_{C,\text{top2},X} \\ &\quad - B_{C,\text{top3},X} - B_{C,\text{top4},X}| \\ |B_{Z,\text{Undesired}}| &= |B_{Z,\text{top1},X} - B_{Z,\text{top2},X} \\ &\quad + B_{Z,\text{top3},X} - B_{Z,\text{top4},X}|. \end{aligned} \tag{4}$$

The detailed values are summarized in Table I. The sign of each magnetic flux density is determined by its direction (as shown in Fig. 7).

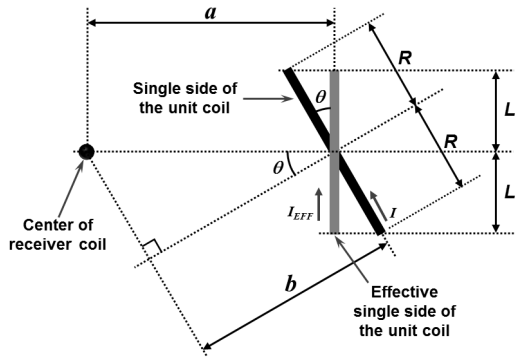


Fig. 8. Current-carrying straight wire.

TABLE I
CALCULATION RESULTS OF THE MAGNITUDE OF UNDESIRED MAGNETIC FLUX DENSITY

Magnitude of the magnetic flux density	a, b	Results
$\boldsymbol{B}_{C,top1,X}$ $(I_{C,top1}\rightarrow P_{C,X})$	$\sqrt{r^2+d^2}$, $\sqrt{r^2+d^2}$	$\frac{\mu_0 I/2\pi}{\sqrt{r^2+d^2}\sqrt{1+\frac{r^2+d^2}{R^2}}}$
$\boldsymbol{B}_{C,top2,X}$ $(I_{C,top2}\rightarrow P_{C,X})$	$\sqrt{R^2+(R+r)^2+d^2}$, $\sqrt{R^2+d^2}$	$\frac{\mu_0 I/2\pi}{\frac{R^2+(R+r)^2+d^2}{\sqrt{R^2+d^2}}\sqrt{1+\frac{\left(R^2+(R+r)^2+d^2\right)^2}{R^2\left(R^2+d^2\right)}}}$
$\boldsymbol{B}_{C,top3,X}$ $(I_{C,top3}\rightarrow P_{C,X})$	$\sqrt{R^2+(R+r)^2+d^2}$, $\sqrt{R^2+d^2}$	$\frac{\mu_0 I/2\pi}{\frac{R^2+(R+r)^2+d^2}{\sqrt{R^2+d^2}}\sqrt{1+\frac{\left(R^2+(R+r)^2+d^2\right)^2}{R^2\left(R^2+d^2\right)}}}$
$\boldsymbol{B}_{C,top4,X}$ $(I_{C,top4}\rightarrow P_{C,X})$	$\sqrt{(2R+r)^2+d^2}$, $\sqrt{(2R+r)^2+d^2}$	$\frac{\mu_0 I/2\pi}{\sqrt{(2R+r)^2+d^2}\sqrt{1+\frac{(2R+r)^2+d^2}{R^2}}}$
$\boldsymbol{B}_{Z,top1,X}$ $(I_{Z,top1}\rightarrow P_{Z,X})$	$\sqrt{(2R+r)^2+R^2+d^2}$, $\sqrt{R^2+d^2}$	$\frac{\mu_0 I/2\pi}{\frac{(2R+r)^2+4R^2+d^2}{\sqrt{R^2+d^2}}\sqrt{1+\frac{\left((2R+r)^2+4R^2+d^2\right)^2}{R^2\left(R^2+d^2\right)}}}$
$\boldsymbol{B}_{Z,top2,X}$ $(I_{Z,top2}\rightarrow P_{Z,X})$	$\sqrt{(3R+r)^2+4R^2+d^2}$, $\sqrt{(3R+r)^2+d^2}$	$\frac{\mu_0 I/2\pi}{\frac{(3R+r)^2+4R^2+d^2}{\sqrt{(3R+r)^2+d^2}}\sqrt{1+\frac{\left((3R+r)^2+4R^2+d^2\right)^2}{R^2\left((3R+r)^2+d^2\right)}}}$
$\boldsymbol{B}_{Z,top3,X}$ $(I_{Z,top3}\rightarrow P_{Z,X})$	$\sqrt{(R+r)^2+4R^2+d^2}$, $\sqrt{(R+r)^2+d^2}$	$\frac{\mu_0 I/2\pi}{\frac{(R+r)^2+4R^2+d^2}{\sqrt{(R+r)^2+d^2}}\sqrt{1+\frac{\left((R+r)^2+4R^2+d^2\right)^2}{R^2\left((R+r)^2+d^2\right)}}}$
$\boldsymbol{B}_{Z,top4,X}$ $(I_{Z,top4}\rightarrow P_{Z,X})$	$\sqrt{(2R+r)^2+4R^2+d^2}$, $\sqrt{4R^2+d^2}$	$\frac{\mu_0 I/2\pi}{\frac{(2R+r)^2+4R^2+d^2}{\sqrt{4R^2+d^2}}\sqrt{1+\frac{\left((2R+r)^2+4R^2+d^2\right)^2}{R^2\left(4R^2+d^2\right)}}}$

For an intuitive comparison of $\boldsymbol{B}_{C,\text{Undesired}}$ and $\boldsymbol{B}_{Z,\text{Undesired}}$ assuming that R, r, and d in Table I are all identical, the calculated ratio of $\boldsymbol{B}_{Z,\text{Undesired}}$ to $\boldsymbol{B}_{C,\text{Undesired}}$ is approximately 3%. From the numerical analysis, we verify that the undesired coupling of the proposed zigzag-shaped coil array is successfully suppressed compared with that of a typical coil array.

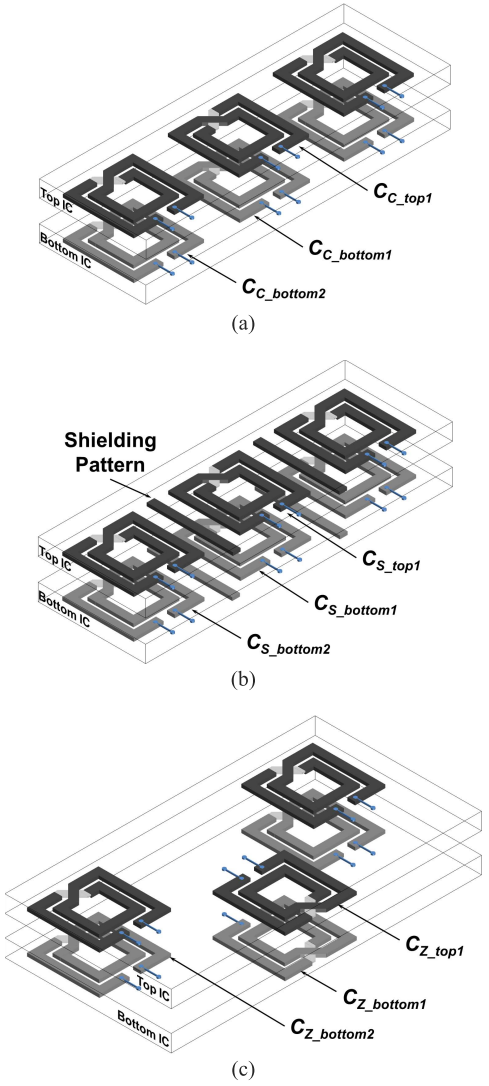


Fig. 9. Conceptual diagram of the EM simulation setup. (a) Typical structure. (b) Shielded structure. (c) Zigzag structure.

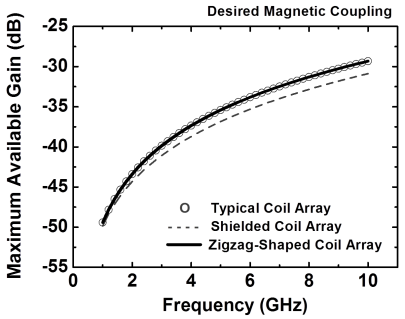
IV. SIMULATION RESULTS

To verify the feasibility of the proposed zigzag-shaped coil array for WCC technology, we performed an electromagnetic (EM) simulation. A conceptual diagram of the EM simulation setup is shown in Fig. 9. For the sake of simplicity, the number of coils is set to three for the coil array and the transceiver circuit blocks are not shown in Fig. 9. The space between adjacent coils for the shielded structure shown in Fig. 9(b) is identical to that of the typical structure. The shielding pattern is connected to an ideal ground node.

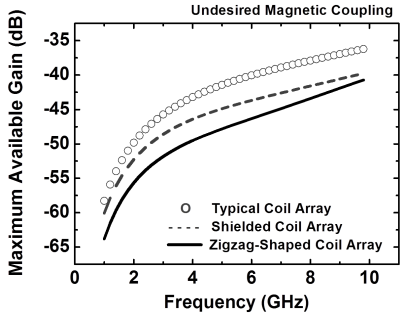
The design parameters for the EM simulations are described in Table II. If the size of the coil is much larger than that of the I/O transceiver, the proposed zigzag structure may require additional chip area compared with typical structures. In general, the chip area for the I/O transceiver of a commercial memory IC, which is one of the possible applications of chip-to-chip communication, is larger than 60×60 μm^2. Accordingly, in this paper, we determine the designed unit coil size as 60×60 μm^2.

TABLE II
DESCRIPTIONS OF THE SIMULATION PARAMETERS FOR THE EM SIMULATIONS

Design Parameters	Values
Number of turns of the unit coil	5
Metal width of the unit coil	3.0 μm
Space between adjacent metal lines	0.8 μm
Distance between coils located in the same chip area	40 μm
Distance between the coil of the top IC and the coil of the bottom IC	50 μm
Metal width of the shielding patterns for the shielded coil array	4.0 μm



(a)



(b)

Fig. 10. Maximum available gain. (a) Desired magnetic coupling. (b) Undesired magnetic coupling.

With the simulation parameters for the EM simulations, we simulated the maximum available gain (MAG, as shown in Fig. 10). Fig. 10(a) shows the quantities of the desired power transmission from C_{C_bottom1} (or C_{S_bottom1}, C_{Z_bottom1}) to C_{C_top1} (or C_{S_top1}, C_{Z_top1}). As shown in Fig. 10 (a), the desired power transmission of the typical and the proposed zigzag structures are very similar. However, the shielded structure has lower power transmission compared with the other structures, as the magnetic coupling between the coil and the shielding pattern degrades the desired magnetic coupling between C_{S_bottom1} and C_{S_top1}. Although the undesired magnetic coupling between C_{C_bottom1} and C_{C_bottom2} degrades the desired magnetic coupling in the typical structure, the distance between the coil and the shielding pattern for the shielded structure is shorter than the distance between the adjacent coils for the typical structure. The MAG for the desired power transmission of the shielded structure is therefore lower than those of the other structures.

Fig. 10(b) shows the quantities of the undesired power transmission from C_{C_bottom1} (or C_{S_bottom1}, C_{Z_bottom1}) to C_{C_bottom2} (or C_{S_bottom2}, C_{Z_bottom2}). We proposed the zigzag-shaped coil array to suppress the quantity of undesired magnetic coupling. As shown in Fig. 10(b), the quantity of undesired magnetic coupling of the proposed zigzag structure is the lowest among the investigated structures. For the shielded structure, the shielding patterns suppress the undesired magnetic coupling between C_{S_bottom1} and C_{S_bottom2}. As a result, the quantity of undesired magnetic coupling of the shielded structure is lower than that of the typical structure. The quantity of undesired magnetic coupling of the shielded structure is between those of the typical and the zigzag structures, as predicted in the previous section. As shown in Fig. 10(b), although the undesired coupling of the typical structure is greater than that of the proposed structure, the amounts of undesired coupling of the typical and proposed structures are relatively low compared with the desired amounts of coupling of the typical and proposed structures. Accordingly, the desired amounts of coupling of the proposed and typical structures are nearly identical on the dB scale.

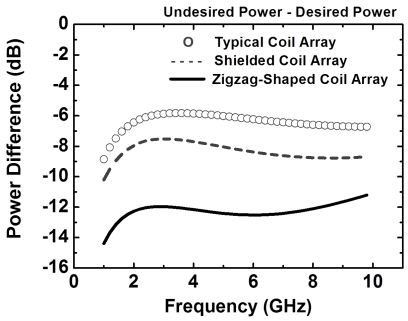


Fig. 11. MAG difference between the desired power and the undesired power.

Fig. 11 shows the simulated results of the MAG difference of the desired power and undesired power. As shown in Fig. 11, the MAG difference of the zigzag structure is lower than those of the other structures. For example, the MAG difference of the zigzag structure is approximately 6 dB lower than that of the typical structure. According to these results, the cross-talk is successfully suppressed without requiring any additional chip area using the proposed zigzag-shaped coil array for WCC technology.

V. EXPERIMENTAL RESULTS WITH A PROTOTYPE

To verify the feasibility of the proposed zigzag-shaped coil array structure, we designed prototypes of the coil arrays using an FR4 PCB. Although the zigzag-shaped coil array is proposed for WCC communication applications, the magnetic coupling characteristics of the coil array itself can be predicted from the measured results of the prototype shown in Fig. 12. The coil array of the prototype is composed of five coils. The design parameters of the prototype are described in Table III. The designed unit coil size is 7.2×7.2 mm^2. As shown in Fig. 12, the directions of the terminals of the even coils differ from those of the coils shown in Fig. 9. This is necessary to accommodate the measurement setup. For example, if the terminals of the even coils are identical to

TABLE III
DESCRIPTIONS OF THE DESIGN PARAMETERS OF THE PROTOTYPE

Design Parameters	Values
Number of turns of the unit coil	2
Metal width of the unit coil	0.2 mm
Space between adjacent metal lines	0.2 mm
Distance between the coils located in the same chip area	3.6 mm
Distance between the coil of the top IC and the coil of the bottom IC	3 mm
Metal width of the shielding patterns for the shielded coil array	0.2 mm

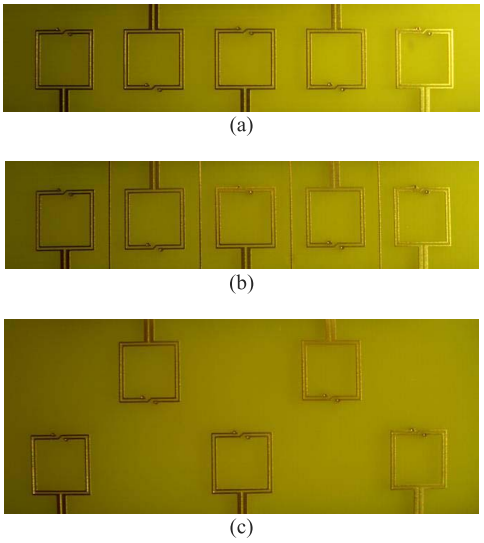


Fig. 12. Photographs of the prototypes. (a) Typical structure. (b) Shielded structure. (c) Zigzag structure.

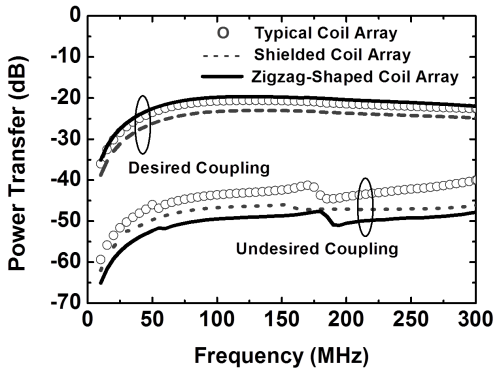


Fig. 13. Measured magnetic coupling and undesired magnetic coupling.

those of the adjacent coils, there is no room for the connectors of the terminals of the adjacent coils. However, from EM simulations, we find that the outcome with different directions of the terminals of adjacent coils does not differ from that with identical directions of the terminals of the adjacent coils. In the prototypes, the area required for the transceiver circuit is omitted given that the aim of the prototypes is to verity the feasibility of the magnetic coupling characteristics of the coil array itself.

Fig. 13 shows the quantities of the desired power transmission and the undesired power transmission, respectively.

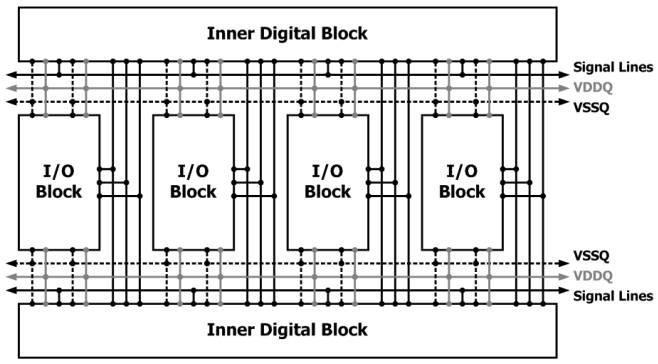


Fig. 14. Conceptual layout of the interface part of general DDR3.

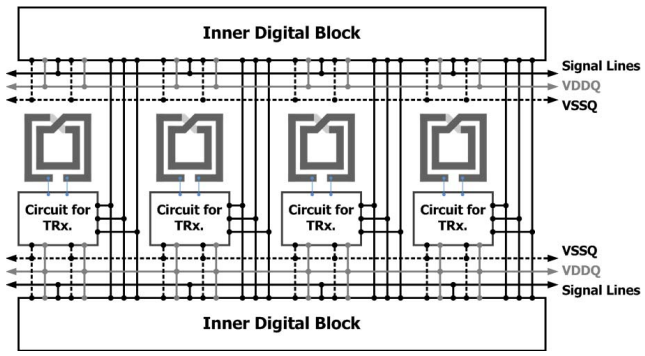


Fig. 15. Possible conceptual layout of the interface part of general DDR3 with WCC technology.

Comparing the measured results shown in Fig. 13 with the simulated results in Fig. 10, the measured results are in general very similar to the simulated results.

Accordingly, the measured results of the prototypes also show that the cross-talk is successfully suppressed without requiring any additional chip area using the proposed zigzag-shaped coil array for WCC technology.

VI. DISCUSSION

Although the proposed zigzag coil array successfully suppresses the undesired coupling, the routing of signal and power lines should be discussed before the zigzag coil array can be adapted to commercial digital ICs. Fig. 14 shows the conceptual layout of the interface part of general DDR3. In general DDR3, the I/O signal should be connected to the upper and bottom inner digital blocks. Accordingly, several signal lines are positioned between the I/O blocks. The power lines for the inner digital block can be shared with the I/O blocks. If WCC technology is used for the I/O part of DDR3, the possible layout can be devised (as shown in Fig. 15). The power mesh and signal lines for WCC technology are nearly identical to those of general DDR3 (as shown in Fig. 14). Similarly, as shown in Fig. 16, the routing of the power and signal lines for WCC technology using the proposed coil array is also nearly identical to the case shown in Fig. 15. Consequently, if WCC technology using the proposed coil array is adapted to general memory ICs, the proposed zigzag structure does not complicate the routing architecture of the power mesh and signal lines.

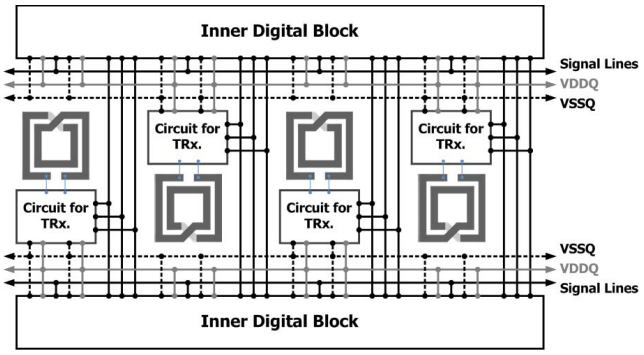


Fig. 16. Possible conceptual layout of the interface part of general DDR3 with WCC technology using the proposed zigzag coil array.

VII. Conclusion

In this paper, we investigated various coil array structures for WCC communication technology. We consider the cross-talk problems and chip area for a comparison of the different array structures assessed here. We proposed a zigzag-shaped coil array to solve the cross-talk problems without the requirement of any additional chip area. For the sake of simplicity, we used three coils for each coil array in an EM simulation. Using a 2.5-D EM simulation, we simulated the maximum available gain to investigate the amounts of desired and undesired magnetic coupling in the aforementioned coil arrays. According to the results, the cross-talk is suppressed by approximately fourfold compared with a typical coil array. These results demonstrate the feasibility of the proposed zigzag-shaped coil array structure.

References

[1] M.-Y. Tsai *et al.*, "Investigation on Cu TSV-induced KOZ in silicon chips: Simulations and experiments," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2331–2337, Jul. 2013.

[2] Y. C. Lee, H. T. Ghaffari, and J. M. Segelken, "Internal thermal resistance of a multi-chip packaging design for VLSI based systems," *IEEE Trans. Compon. Hybrids Manuf. Technol.*, vol. 12, no. 2, pp. 163–169, Jun. 1989.

[3] J.-Q. Lu, "3-D hyperintegration and packaging technologies for micro-nano systems," *Proc. IEEE*, vol. 97, no. 1, pp. 18–30, Jan. 2009.

[4] Z. Xu and J.-Q. Lu, "Three-dimensional coaxial through-silicon-via (TSV) design," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1441–1443, Oct. 2012.

[5] Z. Xu and J.-Q. Lu, "Through-strata-via (TSV) parasitics and wideband modeling for three-dimensional integration/packaging," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1278–1280, Sep. 2011.

[6] L. Zhang, H. Y. Li, S. Gao, and C. S. Tan, "Achieving stable through-silicon via (TSV) capacitance with oxide fixed charge," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 668–670, May 2011.

[7] N. Miura, D. Mizoguchi, T. Sakurai, and T. Kuroda, "Analysis and design of inductive coupling and transceiver circuit for inductive inter-chip wireless superconnect," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 829–837, Apr. 2005.

[8] V. V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro, and T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB transmitter with embedded on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 394–403, Feb. 2009.

[9] N. Miura *et al.*, "A scalable 3D heterogeneous multicore with an inductive thruchip interface," *IEEE Micro*, vol. 33, no. 6, pp. 6–15, Nov./Dec. 2013.

[10] C. Lee, J. Park, J. Yoo, and C. Park, "Study of the coil structure for wireless chip-to-chip communication applications," *Prog. Electromagn. Res. Lett.*, vol. 38, pp. 127–136, Mar. 2013.

[11] C. Lee *et al.*, "Transceiver with inductive coupling for wireless chip-to-chip communication using a 50-nm digital CMOS process," *Microelectron. J.*, vol. 44, no. 9, pp. 852–859, Sep. 2013.

[12] D.-B. Lin, F.-N. Wu, W. S. Liu, C. K. Wang, and H.-Y. Shih, "Crosstalk and discontinuities reduction on multi-module memory bus by particle swarm optimization," *Prog. Electromagn. Res.*, vol. 121, pp. 53–74, Oct. 2011.

[13] M. Danesh and J. R. Long, "Differentially driven symmetric microstrip inductors," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 332–341, Jan. 2002.

[14] D. Mansson and A. Ellgardt, "Comparing analytical and numerical calculations of shielding effectiveness of planar metallic meshes with measurements in cascaded reverberation chambers," *Prog. Electromagn. Res. C*, vol. 31, pp. 123–135, Oct. 2012.

[15] G. Wu, X. Zhang, Z.-Q. Song, and B. Liu, "Analysis on shielding performance of metallic rectangular cascaded enclosure with apertures," *Prog. Electromagn. Res. Lett.*, vol. 20, pp. 185–195, Feb. 2011.

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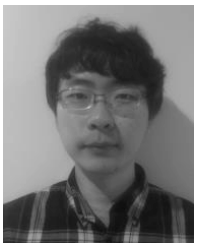

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