Cofabrication of Planar Gunn Diode and HEMT on InP Substrate

Vasileios Papageorgiou, Ata Khalid, *Member, IEEE*, Chong Li, and David R. S. Cumming, *Fellow, IEEE*

***Abstract*— We present the cofabrication of planar Gunn diodes and high-electron mobility transistors (HEMTs) on an indium phosphide substrate for the first time. Electron beam lithography has been used extensively for the complete fabrication procedure and a 70-nm T-gate technology was incorporated for the enhancement of the small-signal characteristics of the HEMT. Diodes with anode-to-cathode separation (L_{ac}) down to 1- and 120-μm width were shown to oscillate up to 204 GHz. The transistor presents a cutoff frequency (f_T) of 220 GHz, with power gain up to 330 GHz (f_{max}). The integration of the two devices creates the potential for the realization of high-power, high-frequency MMIC Gunn oscillators, circuits, and systems.**

***Index Terms*— Gunn diode, high-electron mobility transistor (HEMT), integration, mm-wave.**

I. Introduction

The Gunn diode oscillator was discovered in 1963 [1], while Gunn was examining the current–voltage characteristics of GaAs and indium phosphide (InP). In recent years, research has led to the implementation of increasingly high-frequency Gunn diode oscillators for a range of applications [2]. Typically, Gunn diodes are implemented as a vertical layer stack of materials grown using methods, such as molecular beam epitaxy (MBE). Vertically grown devices have presented a maximum frequency of oscillation of 77 GHz for GaAs-based systems integrated into a rectangular waveguide [3]. Coplanar waveguide (CPW)-based devices that are simpler and cheaper to implement have also been demonstrated, operating at the same frequency [4]. However, the oscillation frequency of the vertical structures is limited by the fixed anode-to-cathode separation that is determined by the epitaxial thickness of the channel layer.

The first theoretical [5] and experimental results [6] indicated that Gunn oscillations can occur on HEMT layer structures. Therefore, the electrodes of the diode can be implemented on the top of the wafer in a planar configuration similarly to the drain and the source of field effect transistors (FETs). The first planar Gunn diodes operating above 100 GHz were presented recently, where L_{ac} was selected accurately through the lithographic design [7]. Using this method, signals at different frequencies can be generated from diodes with different geometries, implemented on the same chip. Recent development of planar Gunn diodes has focused on the modification of the layer structure to increase the output power. The addition of extra doping layers [8] and the introduction of strained $In_{0.23}Ga_{0.77}As$ for the formation of the channel layer [9] led to the significant improvement of the power characteristics. The maximum generated power was boosted to −4 dBm in an alternating $In_{0.23}Ga_{0.77}As$/GaAs layer structure with seven channel layers [10]. However, the current density of the multichannel devices was increased by approximately five times in comparison with the single-channel devices, indicating that not all the channels contribute to the oscillation.

The implementation of planar Gunn diodes and pHEMTs on GaAs substrates side-by-side has been recently studied [11], demonstrating the potential for amplification of the diode signal using a transistor-based amplifier on the same IC. However, the low-power level of −40-dBm suggested that we either improved the layer structure or moved to an InP-based system. Most recently, planar devices with a single channel layer of $In_{0.53}Ga_{0.47}As$ grown on InP have demonstrated exceptional characteristics with 164-GHz maximum frequency of oscillation and −10-dBm generated power [12]. In this paper, we demonstrate the cofabrication of planar Gunn diodes and HEMTs on the same InP substrate for the first time. The InAlAs/InGaAs heterostructure using a single delta-doping layer was designed for the implementation of HEMTs, where $In_{0.53}Ga_{0.47}As$ was used for the formation of the channel and the cap layer. The use of a relatively simple InP-based HEMT structure [12] enabled us to demonstrate cointegration of two types of devices on the same layers, as illustrated in Fig. 1. A new 70-nm T-gate technology has been used for the enhancement of the high-frequency response of the transistor. The detailed layer structure and the fabrication procedure of the HEMT are described extensively in Section II. In addition, the fabrication process of the Gunn diode is also described in detail, presenting the required compatibility with the HEMT material system.

II. Fabrication of the Devices

The layer structure used in this paper was grown on a 355-μm thick substrate of InP, using MBE. We chose to

Manuscript received May 2, 2014; revised June 11, 2014; accepted June 13, 2014. Date of publication July 1, 2014; date of current version July 21, 2014. This work was supported in part by the Engineering and Physical Sciences Research Council, U.K., under Grant EP/HO11862/1, and in part by e2v Technologies (U.K.) Ltd., Chelmsford, U.K. The review of this paper was arranged by Editor K. J. Chen.

V. Papageorgiou, A. Khalid, and D. R. S. Cumming are with the School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K. (e-mail: v.papageorgiou.1@research.gla.ac.uk; ata.khalid@glasgow.ac.uk; david.cumming.2@glasgow.ac.uk).

C. Li was with the School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K. He is now with the National Physical Laboratory, Middlesex TW11 0LW, U.K. (e-mail: chong.li@glasgow.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2014.2331368

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/

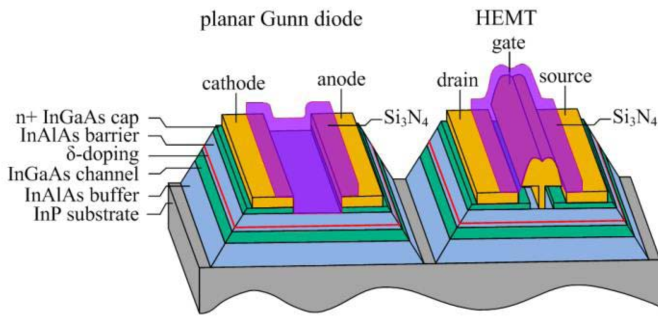

Fig. 1. Cross section illustration of the cofabricated planar Gunn diode and the HEMT (not to scale).

have our designs on a proven layer structure with a Hall mobility (μH) of 2.1×10^{12} cm^{-2} and sheet carrier concentration (n_{sh}) of 7500 cm^2/Vs [13]. A 200-nm thick undoped $In_{0.52}Al_{0.48}As$ buffer layer was grown on the top of the InP substrate, followed by an undoped 15-nm thick $In_{0.53}Ga_{0.47}As$ channel layer. A 3-nm thick layer of $In_{0.52}Al_{0.48}As$ was grown afterward to form the spacer layer. A Si delta-doping layer with 6×10^{12}-cm^{-2} density was deposited on the top of the spacer, followed a 14-nm thick $In_{0.52}Al_{0.48}As$ barrier layer. The growing process was complete after the deposition of a $In_{0.53}Ga_{0.47}As$ cap layer with 14-nm thickness and doping level of 6×10^{18} cm^{-3}.

The first lithographic step incorporates the pattern definition of the Ohmic contacts following the same procedure as presented in [11]. A metal alloy consisting of 14-nm Au/14-nm Ge/14-nm Au/11-nm Ni/70-nm Au was evaporated for the simultaneous formation of the Ohmic contacts for both devices. The contact resistance resulting from the metal stack on the highly doped $In_{0.53}Ga_{0.47}As$ cap layer is equal to 0.12 Ω·mm.

After the fabrication of the Ohmic contacts, the mesa areas of the two devices were isolated from the surrounding areas. A 12% PMMA layer was hard baked in a conventional oven at 180 °C. The samples remained in the oven for 2 h to ensure a high resistivity of the mask to the etching solution. After the development of the resist, the samples were processed by a 1:1:100—orthophosphoric acid:H_2O_2:H_2O solution for 120 s. The isolation of the two devices was tested during the etching procedure via electrical measurements.

The stepped profiles for the implementation of T-gates have traditionally been created by 3-D EBL techniques where different doses are assigned on resist layers with different sensitivities as in UVIII/LOR/PMMA systems [14], [15]. Thus, a sharp profile is created between the head and the foot areas due to the high contrast of the sensitivities between the two layers. In this paper, a new technique is presented using exclusively PMMA resist, as shown in Fig. 2. The PMMA layers were spun at 5 kr/min for 60 s and baked at 155 °C on a hot plate for 90 s, individually.

Following the conventional exposure technique, a low dose is assigned at the side patterns for the formation of the head area. A high dose is assigned afterward in the middle section to create the T-gate foot. However, the different PMMA layers do not have a high contrast between them and the resulting

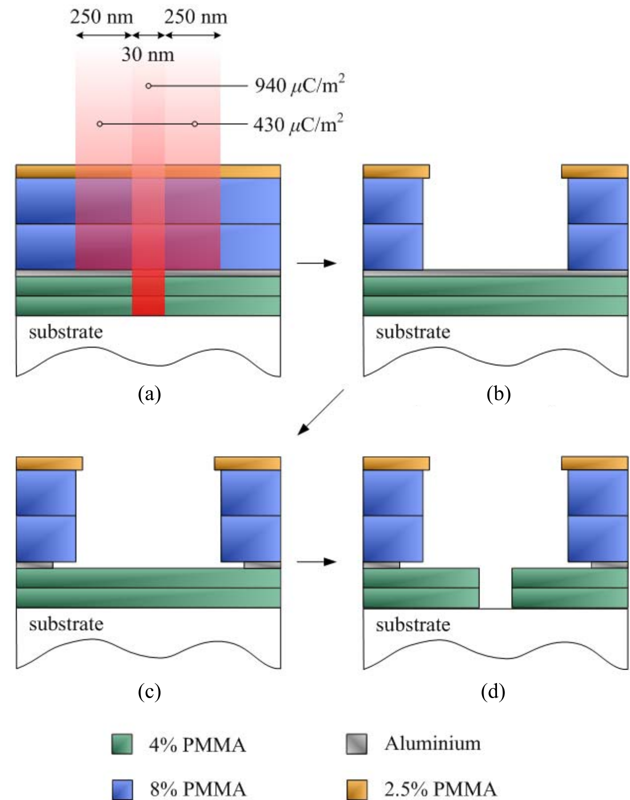

Fig. 2. Schematic diagram of the PMMA/Al/PMMA T-gate technology. (a) Exposure. (b) Head development. (c) Aluminium etching. (d) Foot development.

depth of the head area varied due to temperature and timing variations in the development process [16]. The sharp profile between the top and the bottom PMMA layers was created after the introduction of an intermediate aluminium layer with 10-nm thickness. The Al layer creates a threshold since the electron beam with a relatively low dose of 430 μC/m^2 is sufficiently back-scattered so that the layers underneath are underexposed. Therefore, the low-dose exposure is used for the formation of the head pattern on the top 8% PMMA layers. On the other hand, the high dose equal to 940 μC/m^2 assigned in the middle of the design adequately penetrates the Al layer, exposing the resist stack down to the substrate. Therefore, the foot pattern is created at the bottom 4% PMMA layers. The top 2.5% PMMA layer has a higher molecular weight compared with the 8% PMMA layer underneath, creating the required undercut profile for the liftoff process. A 70-nm foot window resulted from the 30-nm line design due to the increased forward scattering caused by the multiple PMMA/Al layers. However, the current technique is simple to implement since only one registration job is required.

The opening of the T-gate window is performed in three steps. Initially, a 2.5:1 IPA:MIBK developer solution kept at 23 °C is applied for 40 s, removing the top three PMMA layers. The MF-CD-26 (Microposit) solution is applied for 100 s afterward, etching the Al layer sufficiently for the exposure of the bottom layers. Finally, a second treatment with the MIBK solution is applied for 40 s for the development of the foot pattern.

Following the creation of the T-shaped resist profile, the recess etching procedure was performed for the removal of the highly doped cap layer using a succinic acid solution. The pH of the solution was adjusted to 5.9 and the samples were processed for 16 s. Afterward, a deoxidizing process was applied using a 10:1 H_2O:ammonia solution for 20 s and the gate area was metallised using a conventional 15/15-nm Pt/400-nm Au metal alloy.

Finally, the areas between the drain and the source were passivated using a Si_3N_4 film. Prior to the dielectric deposition, a bilayer of PMMA was spun and the windows were opened around the gates. An ICP-CVD process was used in the next, for the deposition of the Si_3N_4 film. This process was executed at room temperature preventing the diffusion of the gate metal in the semiconductor and any melting of the PMMA. In the end, the unwanted dielectric was removed following a liftoff process.

The coplanar waveguide pads of both devices were deposited afterward using a metal stack of 20-nm Ti/500-nm Au, presenting 50 Ω of characteristic impedance. The fabrication process continued with the removal of the cap layer between the anode and the cathode of the diode. Similarly to the recess etching process of the HEMT, the same succinic acid solution was applied for the selective removal of $In_{0.53}Ga_{0.47}As$ between the diode electrodes. A target current level of 60 mA was set for 120-μm wide Gunn diodes, according to [12], indicating the end point of the process. The corresponding current density, which is equal to 500 mA/mm, is in agreement with the current density of the HEMT as presented in Section III. Finally, the areas between the anode and the cathode of the diode were deoxidized using a 4:1 H_2O:HCl solution and passivated with Si_3N_4 following the same process described for the transistor.

The most significant advantage of the procedure described above is the common execution of the majority of the fabrication steps for both the Gunn diode and the HEMT. Only the passivation procedure is executed individually due to the different deoxidizing solutions required for the exposed InAlAs barrier layer of the HEMT and the InGaAs cap layer of the Gunn diode. The complete Gunn diode and HEMT are shown in Fig. 3 and a more detailed image of the HEMT before the deposition of the passivation layer is shown in Fig. 4.

III. Results and Discussion

An Agilent technologies B1500A semiconductor analyzer was used for the dc characterization of the devices. Fig. 5 shows the drain current of the fabricated transistors versus the drain voltage for different biasing voltages applied at the gate. The measurements correspond to HEMTs with two-finger 70-nm T-gates and 25-μm width. The devices present a maximum current density of 560 mA/mm for 1 and 0.8 V V_{DS} where a V_{GS} of −0.6 V is required for the pinchoff of the transistor. The transconductance performance is shown in Fig. 6 showing a maximum value of 520 mS/mm for 0.6 V V_{DS} and −0.15 V V_{GS} biasing conditions.

Two Agilent vector analyzers were used for the small-signal characterization of the HEMTs for the frequency range between 10 MHz–110 GHz and 140–220 GHz. Following the characterization of the HEMTs, the tapers performing the CPW transition from 40–60–40 to 15–20–15-μm ground-signal-ground configuration (Fig. 3), were de-embedded. The Ansoft HFSS electromagnetic modeling tool was used for the simulation of the small signal characteristics up to 110 GHz. For the frequency range between 140 and 220 GHz,

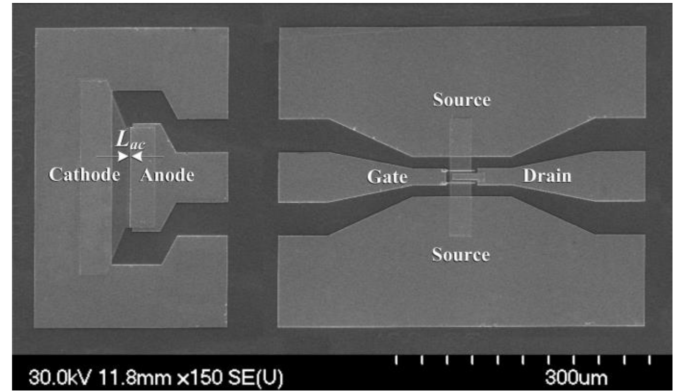

Fig. 3. Scanning electron microscope picture of the fabricated 120-μm wide Gunn diode with 1-μm L_{ac} (left) and the 25-μm wide HEMT with 2 × 70-nm T-gates (right).

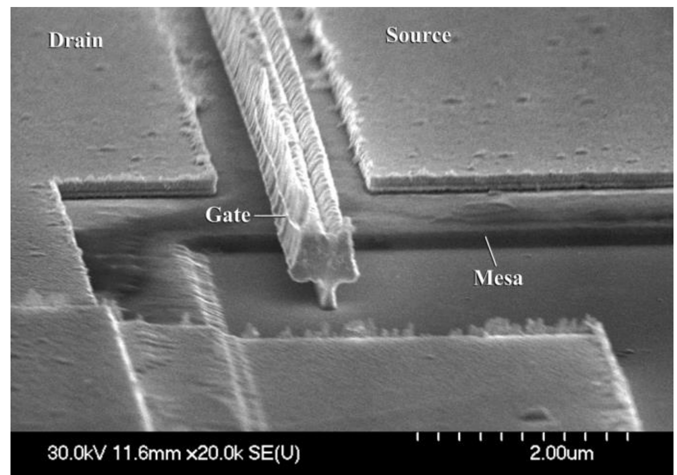

Fig. 4. Detailed scanning electron microscope picture of the fabricated HEMT structure. The drain-to-source separation is equal to 1.5 μm.

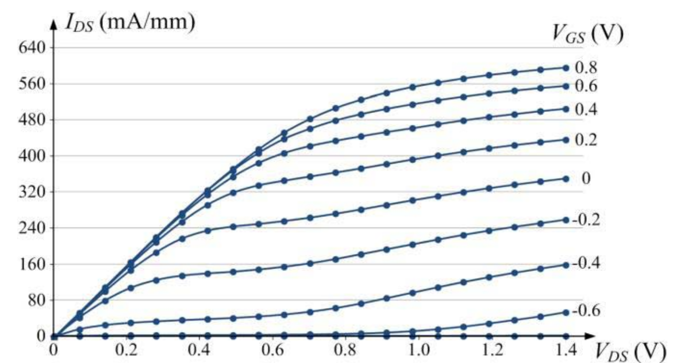

Fig. 5. Current–voltage (I_{DS}–V_{DS}) characteristics of the 2-nm × 70-nm T-gate HEMT with 25-μm width for variable V_{GS}.

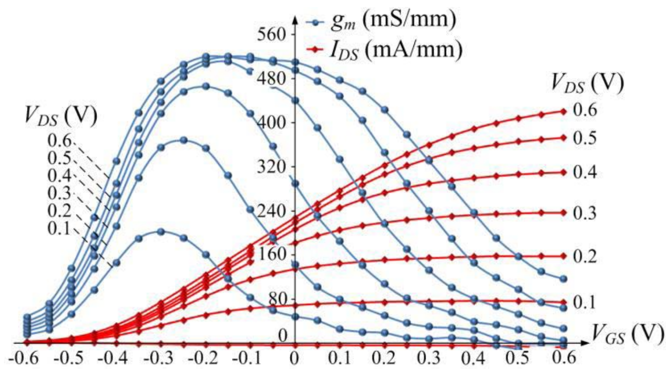

Fig. 6. Transconductance-voltage ($g_m - V_{GS}$) characteristics (blue curves) and current–voltage (I_{DS}–V_{GS}) characteristics (red curves) for variable V_{DS}.

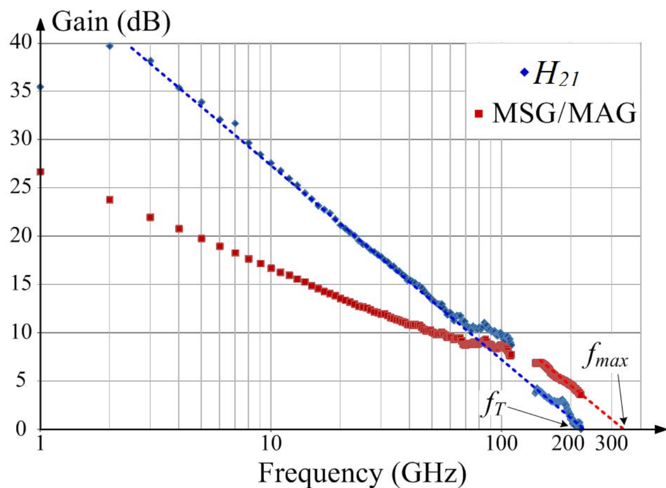

Fig. 7. Current gain H_{21} and MSG/MAG as a function of the operation frequency for the 2-μm × 25-μm wide HEMT. The f_{max} and the f_T after de-embedding the transition pads are 330 and 220 GHz, respectively.

the transition pads were characterized using two Picoprobe GSG probes with 100- and 50-μm pitch. The maximum stable/available gain (MSG/MAG) and the current gain H_{21} of the 2×25 μm devices are shown in Fig. 7 after de-embedding the transition pads. The devices biased at −0.15 V V_{GS} and 1.0 V V_{DS} demonstrate an f_T of 220 GHz and f_{max} equal to 330 GHz.

An E4448A Agilent technologies spectrum analyzer was used for the investigation of the Gunn diode oscillations, as shown in Fig. 8. An ACP 110–100 GSG CascadeMicrotech probe and a WHMP-10 Faran technology mixer were used for the detection of oscillations in the W-band. A Picoprobe GSG probe with 100-μm pitch and a WR-05 Faran technology mixer were used for the investigation of the frequency range between 140 and 220 GHz. After the identification of the oscillation frequencies, the mixers were replaced by a PM4 Ericson power meter for the accurate measurement of the generated power (Fig. 8). The losses introduced by the probes were also subtracted from the power measurements.

Devices with 60- and 120-μm width and various L_{ac} designs were fabricated, where the 120-μm wide diodes presented superior power performance over the 60-μm devices. Fig. 9 shows the measured spectrum of a Gunn diode with

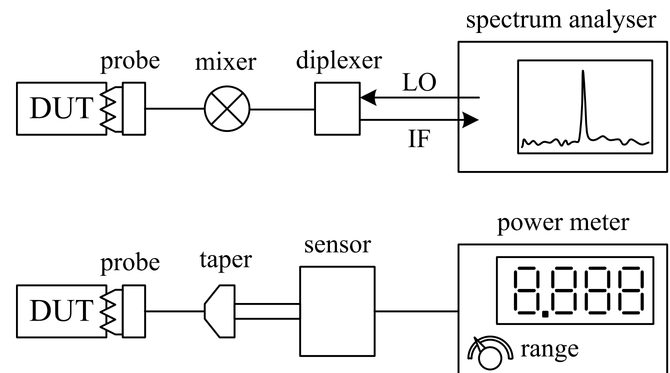

Fig. 8. Experimental setup for frequency and power characterization.

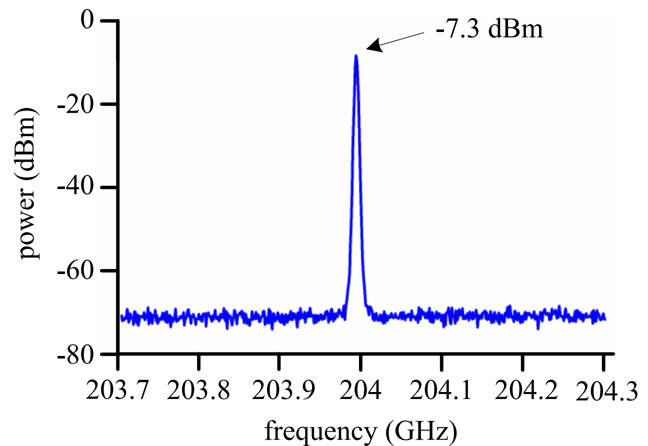

Fig. 9. Measured spectrum of the 120-μm wide Gunn diode with 1-μm L_{ac} biased at 3.2 V.

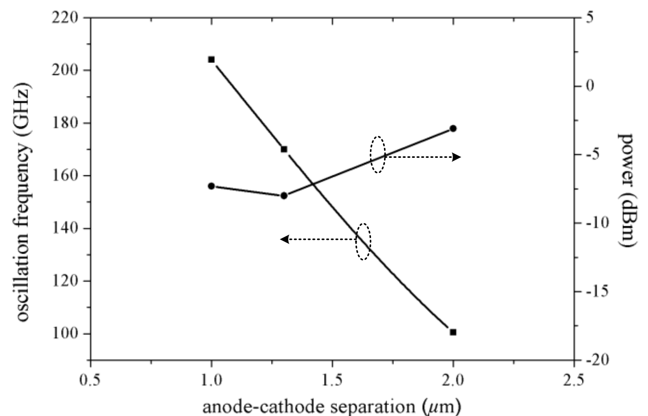

Fig. 10. Dependence of the oscillation frequency and the generated power for 120-μm wide devices with various L_{ac}.

1-μm L_{ac} and 120-μm width biased at 3.2 V. The device generates oscillations at 204 GHz with −7.3-dBm maximum output power. The oscillation frequency and the generated power for devices with various L_{ac} are shown in Fig. 10. The frequency dependence follows the same rule as reported in [12] for devices with $In_{0.53}Ga_{0.47}As$ channel. The generated power was found to be unrelated to the L_{ac}, remaining as approximately −6 dBm for all the devices. These new devices therefore produce similar power levels to those devices

presented in [12] (−10 dBm), where the layer structure was exclusively designed for the fabrication of planar Gunn diodes The maximum measured power in this paper was equal to −3.1 dBm for devices with 2-μm L_{ac} at 130 GHz.

The presented results show a great potential for the implementation of high-power high-frequency oscillators consisting of planar Gunn diodes and HEMTs. The diode itself demonstrates excellent characteristics and the future integration with a transistor amplifier is expected to enhance significantly the output power. In addition, a possible implementation of a HEMT-based mixer circuit could boost the generated frequencies in the terahertz regime.

The new 70-nm T-gate technology was used for the demonstration of HEMT devices with very good high-frequency performance, compared with similar geometries [13], [17]. However, the reduction of the T-gate length in the range of 30–50 nm is required for the enhancement of the gain performance in the D-band (110–140 GHz) and above. In a future development of the T-gate technology, the foot area could be exposed after the removal of the head area. Thus, a shorter gate length would result from the reduced forward scattering of the e-beam. Since no rapid thermal annealing process is required in this process, a self-aligned technique can also be applied, providing significant advantages as demonstrated in [15]. The current and transconductance of the HEMTs could be increased by the addition of a second δ-doping layer in future implementations [17]. The addition of an extra doping layer is also expected to introduce additional offers for the power performance of the Gunn diode [8].

IV. Conclusion

The integration of planar Gunn diodes and HEMTs on an InP substrate has been presented for the first time in this paper. The maximum frequency of oscillation equal to 204 GHz for planar Gunn diodes has been demonstrated from devices with 1-μm L_{ac} and 120-μm width. The power levels of the diodes are also very promising where −3.1-dBm maximum generated power has been measured for 2-μm devices The HEMTs present f_T of 220 GHz and $f_{\max}$ of 330 GHz and the performance of the devices is expected to improve significantly after the reduction of the gate length and the use of a self-aligned technique. The technology presented demonstrates excellent characteristics for the implementation of high-power, high-frequency MMIC oscillators.

Acknowledgment

The authors would like to thank the staff of the James Watt Nanofabrication Center at the University of Glasgow for helping fabricating the devices reported in this paper.

References

[1] J. B. Gunn, “Microwave oscillation of current in III-V semiconductors,” *Solid State Commun.*, vol. 1, no. 4, p. 4, 1963.

[2] D. L. Woolard, E. R. Brown, M. Pepper, and M. Kemp, “Terahertz frequency sensing and imaging: A time of reckoning future applications?” *Proc. IEEE*, vol. 93, no. 10, pp. 1722–1743, Oct. 2005.

[3] A. Föster, J. Stock, S. Montanari, M. I. Lepsa, and H. Lüth, “Fabrication and characterisation of GaAs Gunn diode chips for applications at 77 GHz in automotive industry,” *Sensors*, vol. 6, no. 4, pp. 350–360, 2006.

[4] S. Montanari, *Fabrication and Characterization of Planar Gunn Diodes for Monolithic Microwave Integrated Circuits*. Jülich, Germany: Forschungszentrum, 2005, p. 158.

[5] G. M. Dunn, A. Phillips, and P. J. Topham, “Gunn instabilities in power HEMTs,” *Electron. Lett.*, vol. 37, no. 8, pp. 530–531, Apr. 2001.

[6] A. L. Springer, C. G. Diskus, K. Lubke, A. Stelzer, and H. W. Thim, “Transferred electron effect in AlGaAs/GaAs multi-quantum-well structures,” in *Proc. 27th Eur. Solid-State Device Res. Rec. Conf.*, Sep. 1997, pp. 296–299.

[7] A. Khalid *et al.*, “A planar Gunn diode operating above 100 GHz,” *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 849–851, Oct. 2007.

[8] C. Li *et al.*, “Enhancement of power and frequency in HEMT-like planar Gunn diodes by introducing extra delta-doping layers,” *Microw. Opt. Compon. Lett.*, vol. 53, no. 7, pp. 1624–1626, Jul. 2011.

[9] C. Li *et al.*, “Design, fabrication and characterization of $In_{0.23}Ga_{0.77}$ as-channel planar Gunn diodes for millimeter wave applications,” *Solid State Electron.*, vol. 64, no. 1, pp. 67–72, Oct. 2011.

[10] A. Khalid, C. Li, V. Papageorgiou, N. J. Pilgrim, G. M. Dunn, and D. R. S. Cumming, “A 218-GHz second-harmonic multiquantum well GaAs-based planar Gunn diodes,” *Microw. Opt. Technol. Lett.*, vol. 55, no. 3, pp. 686–688, Mar. 2013.

[11] V. Papageorgiou, A. Khalid, M. J. Steer, C. Li, and D. R. S. Cumming, “Monolithic fabrication of a planar Gunn diode and a pHEMT side-by-side,” in *Proc. 43rd Eur. Solid-State Device Res. Conf.*, Bucharest, Romania, Sep. 2013, pp. 111–114.

[12] A. Khalid *et al.*, “$In_{0.53}Ga_{0.47}As$ planar Gunn diodes operating at a fundamental frequency of 164 GHz,” *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 39–41, Jan. 2013.

[13] Y. Chen *et al.*, “First demonstration of InAlAs/InGaAs HEMTs using T-gates fabricated by a bilayer of UVIII and PMMA resists,” in *Proc. 8th IEEE Int. Symp. High Perform. Electron Devices Microw. Optoelectron. Appl.*, Nov. 2000, pp. 202–205.

[14] Y. Chen *et al.*, “Fabrication of ultrashort T gates using a PMMA/LOR/UVIII resist stack,” *J. Vac. Sci. Technol. B*, vol. 21, no. 6, pp. 3012–3016, Nov./Dec. 2003.

[15] D. A. J. Moran, H. McLelland, K. Elgaid, G. Whyte, C. R. Stanley, and I. Thayne, “50-nm self-aligned and ‘standard’ T-gate InP pHEMT comparison: The influence of parasitics on performance at the 50-nm node,” *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2920–2925, Dec. 2006.

[16] A. Schleunitz, V. A. Guzenko, A. Schander, V. Marko, and S. Helmut, “Selective profile transformation of electron-beam exposed multilevel resist structures based on a molecular weight dependent thermal reflow,” *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 29, no. 6, pp. 06F302-1–06F302-4, Nov./Dec. 2011.

[17] D. A. J. Moran *et al.*, “Self-aligned T-gate InP HEMT realisation through double delta doping and a non-annealed ohmic process,” *Microelectron. Eng.*, vols. 73–74, no. 1, pp. 814–817, Jun. 2004.

Vasileios Papageorgiou received the degree in physics and the M.Sc. (Diploma) degree in electronics and computers from the Department of Physics, University of Patras, Patras, Greece, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the University of Glasgow, Glasgow, U.K., focusing on the integration of planar Gunn diodes and HEMTs for the implementation of high-power MMIC oscillators.

Ata Khalid received the Ph.D. degree in electronic device engineering from King’s College London, London, U.K., in 2000.

He was with King’s College London for several years to develop MMIC design and fabrication processes, development of HBTs, and HEMTs. He joined the School of Engineering at the University of Glasgow, Glasgow, U.K., in 2004, to develop solid-state terahertz radiation source technology based on planar Gunn diodes.

Chong Li received the M.Sc. (Hons.) degree from the University of Manchester, Manchester, U.K., in 2007, and the Ph.D. degree from the University of Glasgow, Glasgow, U.K., in 2011.

He has held a post-doctoral position with the University of Glasgow since 2011, where he joined the National Physical Laboratory in 2014. His current research interests include antenna metrology and wireless sensor networks.

David R. S. Cumming received the B.Eng. degree from the University of Glasgow, Glasgow, U.K., and the Ph.D. degree from the University of Cambridge, Cambridge, U.K.

He is a Professor of Electronic Systems with the University of Glasgow, where he is the Research Dean and leads the Microsystem Technology Group. He is involved in sensor systems and technologies for biomedical and imaging.