Characterization of Negative-Bias Temperature Instability of Ge MOSFETs With GeO_2/Al_2O_3 Stack

Jigang Ma, Jian Fu Zhang, Zhigang Ji, Brahim Benbakhti, Wei Dong Zhang, Xue Feng Zheng, Jerome Mitard, Ben Kaczer, Guido Groeseneken, *Fellow, IEEE*, Steve Hall, *Senior Member, IEEE*, John Robertson, and Paul R. Chalker

***Abstract*— Ge is a candidate for replacing Si, especially for pMOSFETs, because of its high hole mobility. For Si-pMOSFETs, negative-bias temperature instabilities (NBTI) limit their lifetime. There is little information available for the NBTI of Ge-pMOSFETs with $Ge/GeO_2/Al_2O_3$ stack. The objective of this paper is to provide this information and compare the NBTI of Ge- and Si-pMOSFETs. New findings include: 1) the time exponent varies with stress biases/field when measured by either the conventional slow dc or pulse I–V technique, making the conventional V_g-accelerated method for predicting the lifetime of Si-pMOSFETs inapplicable to Ge-pMOSFETs used in this paper; 2) the NBTI is dominated by positive charges (PCs) in dielectric, rather than generated interface states; 3) the PC in $Ge/GeO_2/Al_2O_3$ can be fully annealed at 150 °C; and 4) the defect losses reported for Si sample were not observed. For the first time, we report that the PCs in oxides on Ge and Si behave differently, and to explain the difference, an energy-switching model is proposed for hole traps in Ge-MOSEFTs: their energy levels have a spread below the edge of valence band, i.e., E_V, when neutral, lift well above E_V after charging, and return below E_V following neutralization.**

***Index Terms*— Al_2O_3, degradations, Ge MOSFETs, Ge/GeO_2, high-k on Ge, hole traps, lifetime, negative-bias temperature instability (NBTI), positive charges (PCs).**

I. Introduction

THE successful downscaling of Si MOSFETs has enabled a continuous increase of devices per chip and the operation speed since 1960s, but it is approaching its end since the device is running out of atoms, and its leakage and variability is becoming intolerable [1]–[6]. To continue improving device speed, much effort has been made to replace Si by high-mobility semiconductors [1]–[4]. Ge is a strong candidate, especially for pMOSFETs because its intrinsic hole mobility is about four times of that for Si.

Promising results have already been demonstrated for Ge pMOSFETs through two approaches. One is to use a Si-cap of several monolayers [1], [2], [4]. This offers good compatibility with existing Si processes, and the gate dielectric stack used is often the same as that for Si. However, the interface states are relatively high, the Si-cap increases the separation between gate and channel, and there are difficulties in making Ge nMOSFETs of good performance [7]. The other approach is preparing GeO_2/high-k stack directly on Ge [2], [3], [8]–[10]. By controlling the interaction of GeO_2 with Ge and suppressing the evaporation of GeO, it has been reported that the interface states can be as low as that for SiO_2/Si [8], [9], [11]. This approach offers the potential for fabricating Ge nMOSFETs [8], [12], [13].

The process for fabricating Ge MOSFETs is becoming sufficiently mature and reproducible to warrant research into their reliability, and some encouraging results have been reported [7], [14], [15]. Good TDDB data were obtained [14], but electron trapping is high [16], similar to that in the early stage of developing high-k/SiON stack for Si [17]–[20]. For Si-based CMOS technologies, the negative-bias temperature instability (NBTI) is the most severe reliability issue, since it results in a lifetime of pMOSFETs shorter than that of nMOSFETs [21], [22]. With Si-capped Ge MOSFETs, it has been reported that NBTI can be lower than its Si counterpart [2], [14], [15], [23]. For the Ge pMOSFETs without an Si-cap layer, however, there is little information available on the NBTI.

The central objective of this paper is to provide the information on the NBTI of Ge pMOSFETs with a $Ge/GeO_2/Al_2O_3$ structure. The results will be compared with both Si/SiON, Si/SiON/high-k stacks, and Si-capped Ge MOSFETs, and similarities and differences will be highlighted. The dependence of NBTI on both stress field and temperature is investigated. Attention will be paid to the defects responsible for NBTI, and the relative contribution from generated interface states will

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J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, and W. D. Zhang are with the School of Engineering, John Moores University, Liverpool L3 3AF, U.K. (e-mail: j.ma@2011.ljmu.ac.uk; j.f.zhang@ljmu.ac.uk; z.ji@ljmu.ac.uk; b.benbakhti@ljmu.ac.uk; w.zhang@ljmu.ac.uk).

X. F. Zheng is with Xidian University, Xi'an 710071, China (e-mail: xfzheng@mail.xidian.edu.cn).

J. Mitard and B. Kaczer are with imec, Leuven B-3001, Belgium (e-mail: mitard@imec.be; kaczer@imec.be).

G. Groeseneken is with imec, Leuven B-3001, Belgium, and also with Katholieke Universitet Leuven, Leuven 3001, Belgium (e-mail: groes@imec.be).

S. Hall and P. R. Chalker are with the University of Liverpool, Liverpool L69 3GJ, U.K. (e-mail: s.hall@liverpool.ac.uk; pchalker@liverpool.ac.uk).

J. Robertson is with the University of Cambridge, Cambridge CB2 1TN, U.K. (e-mail: jr214@hermes.cam.ac.uk).

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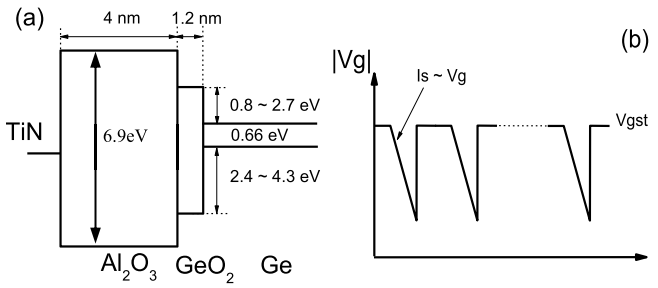

Fig. 1. (a) Schematic energy band diagram and structure of the used sample. (b) Gate bias waveform used in tests. V_{gst} is the stress bias.

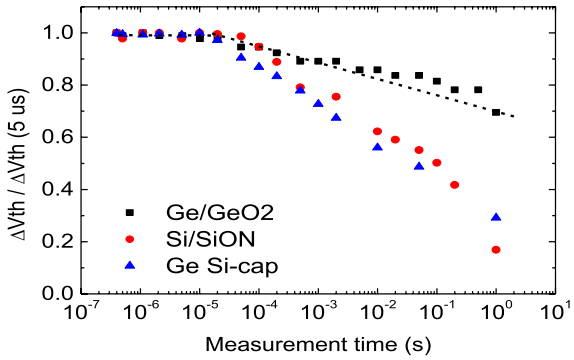

Fig. 2. Dependence of ΔV_{th} on the measurement time for different samples. The stress field over the interfacial layer is 6.5 MV/cm for Ge/GeO_2 and 10 MV/cm for both Si/SiON and Si-capped Ge sample. The stress time is 1 ks and temperature is 20 °C. During the measurement period, V_g was kept negative and did not reach zero, as shown in Fig. 1(b).

be estimated. It is found that the positive charges (PCs) in the oxides on Ge and Si behave differently, and when measured by either the conventional slow dc or pulse I–V technique, the conventional lifetime prediction method developed for Si based on the constant power exponent is not applicable to Ge pMOSFETs used in this paper. A defect energy switching model is proposed to explain the differences.

II. Devices and Experiments

The gate dielectric stack used for the majority of tests in this paper is shown in Fig. 1(a). The Ge layer is 700 nm and grown directly on Cz–Si wafers. To minimize interface states, a 1.2-nm GeO_2 was prepared by exposing clean Ge surface to an atomic oxygen flux at a low temperature of 150 °C for 20 min. A 4-nm Al_2O_3 was then produced by molecular beam deposition in the same chamber [24], resulting in an SiO_2 equivalent oxide thickness of 2.35 nm for the stack. Although Al_2O_3 only has a modest dielectric constant, it can suppress the evaporation of GeO and, in turn, the deterioration of GeO_2/Ge interface [25]. The device was annealed postmetallization in forming gas at 350 °C for 20 min. The channel length used in this paper is typically 1 μm and the width is 50 μm. The pMOSFETs have a 10-nm physical vapour deposition TiN metal gate. For the purpose of comparison, other structures used include Ge/Si-cap/SiO_2/HfO_2, Si/SiON/high-k, and Si/SiON, and their details will be given in figure captions or legends.

The test follows the standard stress-and-sense procedure [26], [27], and a typical V_g waveform is shown in Fig. 1(b). To monitor the threshold voltage shift, i.e., ΔV_{th}, the stress was periodically interrupted, and the source current, i.e., I_s, instead of I_d, versus V_g was recorded under a drain bias of $V_d = -100$ mV using a V_g ramp to minimize the impact of junction leakage. ΔV_{th} was extracted from the V_g shift at a constant $I_s = 100 \times W/L$ nA [28].

The temperature used is in the range of 20 °C–125 °C, and the stress and measurement were performed at the same temperature, unless otherwise specified. The electric field over the interfacial GeO_2 layer was calculated from $E_{ox} = (V_g - V_{th}) \times 3.9/(6\times \text{ EOT})$, where EOT is the SiO_2 equivalent thickness, and the GeO_2 has a dielectric constant of six [29].

The measurement time, t_m, can be defined as the time for sweeping V_g from the stress level V_{gst} to the measurement V_g for $I_s = 100 \times W/L$ nA [see the ramp in Fig. 1(b)]. Reliable measurements were obtained only for $t_m > 0.4$ μs, and the recovery for shorter time could not be assessed. Fig. 2 shows that the recovery is negligible when t_m increases from ~0.4 to ~10 μs, and $t_m = 5$ μs is used here to minimize recovery. When $t_m = 1$ s, recovery lowers ΔV_{th} by 70%–80% for Si/SiON and the Si-capped Ge sample, but only ~30% for $Ge/GeO_2/Al_2O_3$, so that ΔV_{th} is relatively stable for the latter.

In this paper, both $t_m = 5$ μs [27], [30] and $t_m = 1$ s [31]–[33] were used. Although $t_m = 5$ μs minimizes recovery, agreement has not been reached on the NBTI kinetics even for Si/SiON [34]–[36]. Under the conventional slow dc measurement of $t_m = 1$ s, however, it is widely accepted that ΔV_{th} follows a power law and the V_g-accelerated lifetime prediction method is established [37], and some industrial researchers preferred $t_m = 1$ s [38]. It is of importance to find out whether this method is applicable for $Ge/GeO_2/Al_2O_3$.

III. Results and Discussion

A. NBTI Under Different Stress Fields

The V_g-accelerated lifetime prediction method for Si/SiON requires the time exponent of ΔV_{th} to be independent of the stress V_g [27], [37]. When using this method, the stress bias, i.e., V_{gst}, typically does not change with time, and t_m is approximately seconds. We applied these test conditions first to the $Ge/GeO_2/Al_2O_3$, and Fig. 3(a) shows that ΔV_{th} was substantial even under an operational bias level of −1.2 V ($E_{ox} = -2$ MV/cm) and it is V_g-accelerated. The defect density in the current $Ge/GeO_2/Al_2O_3$ is clearly too high to meet the lifetime required for commercial application. It is of interest, however, to study their properties and dynamics, since the past experiences from high-k/SiON stack on Si show that the nature of the defects does not change when their density reduces substantially through process optimization [39], [40].

Although Fig. 3(a) appears similar to the conventional Si/SiON, where ΔV_{th} follows a power law against stress time [27], $\log|\Delta V_{th}|$ versus log(time), however, is not a parallel shift for different V_{gst} and the time exponent, n, reduces from 0.33 at $V_{gst} = -0.8$ V to 0.13 at $V_{gst} = -2.2$ V in Fig. 3(b), despite that the $|E_{ox}| \leq 4.5$ MV/cm used here is well within

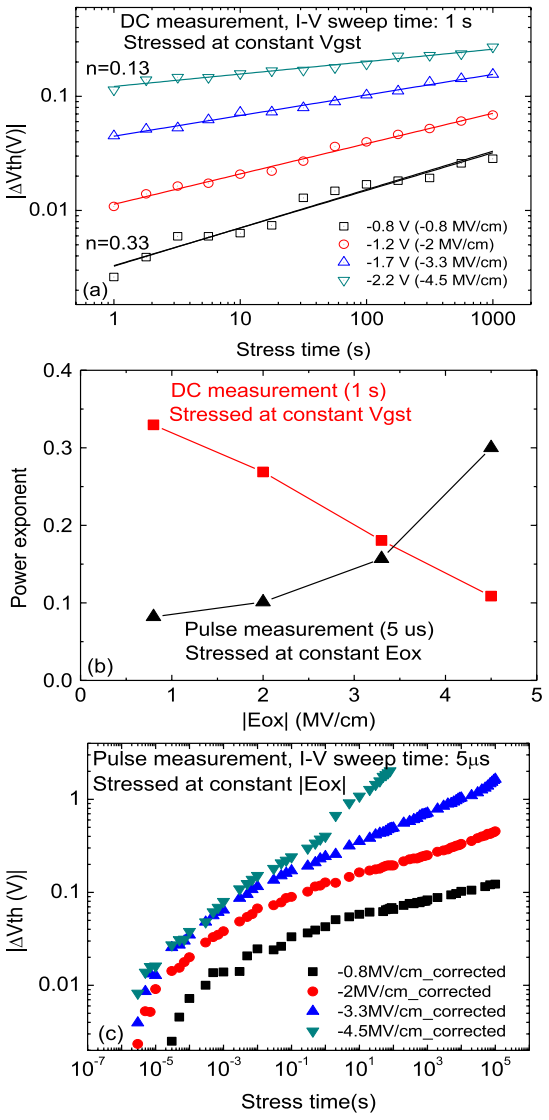

Fig. 3. (a) NBTI degradation kinetics under different stress biases at 20 °C measured by slow dc I–V of t_m = 1 s. The solid lines were fitted with a power law. The stress V_g does not change with time, and E_{ox} in the legend is the field strength over GeO_2 at the start of stress. (b) Time exponent at different V_{gst} for dc and E_{ox} for pulse measurement extracted within the time range 1–1000 s. (c) NBTI kinetics under constant stress E_{ox} at 20 °C measured by pulse I–V of t_m = 5 μs. The stress $|V_g|$ was corrected and increased with time to maintain a constant E_{ox}, here.

the range typically used for Si MOSFETs when observing a constant time exponent [27], [41].

A possible explanation for the lower n at higher V_{gst} is that, when the stress was carried out under constant bias V_{gst}, the formation of PCs lowers the $|E_{ox}|$ near the Ge/dielectric interface. At higher V_{gst}, there are more PCs, leading a larger reduction in $|E_{ox}|$ near Ge, lowering $|\Delta V_{th}|$ and in turn n. This PCs-induced $|E_{ox}|$ reduction can be corrected by increasing V_{gsti} for a stress step i from the V_{gst} at the start of stress by ΔV_{thi-1}, so that the effective stress bias, $(V_{gst}-V_{th})$, and E_{ox} are kept constant. To suppress the recovery during measurement and the consequent underestimation of ΔV_{th}, t_m = 5 μs was used, and Fig. 3(c) shows the result under constant stress E_{ox}. The degradation does not follow a power law with a single exponent over the whole range of test time in

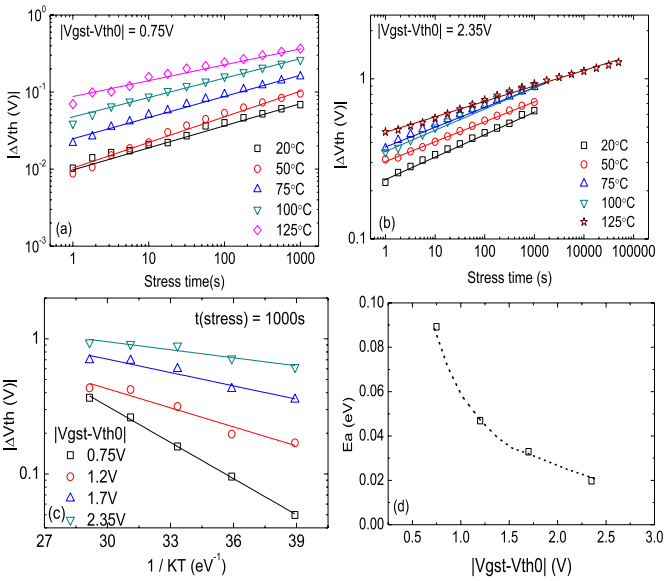

Fig. 4. NBTI kinetics under different stress temperatures, t_m = 1 s, and (a) $|V_{gst}-V_{th}0|$ = 0.75 and (b) 2.35 V. (c) Arrhenius plot at 1000 s. (d) Extracted apparent activation energy from (c) at different $|V_{gst}-V_{th}0|$.

Fig. 3(c), although data between 1 and 1000 s can be fitted with a power law. The time exponent extracted between 1 and 1000 s is shown in Fig. 3(b), which increases for higher $|E_{ox}|$. As a result, suppressing recovery during measurements and stressing under constant E_{ox} do not lead to a constant time exponent, and the conventional lifetime prediction method cannot be used for the $Ge/GeO_2/Al_2O_3$ used here.

B. Effects of Stress Temperature and Anneal

Fig. 4(a) shows the ΔV_{th} under $|V_{gst}-V_{th}0|$ = 0.75 V for different stress temperatures with t_m = 1 s. As expected, the NBTI is thermally activated. Under a higher $|V_{gst}-V_{th}0|$ = 2.35 V, however, Fig. 4(b) shows that ΔV_{th} tends to become insensitive to temperature as it rises. This leads to a reduction of the activation energy, E_a, for higher V_{gst}, as shown in Fig. 4(c) and (d). E_a was extracted from the Arrhenius plot at 1000 s in Fig. 4(c). It is an apparent activation energy with the measurement made at the stress temperature [42]. The insensitivity of ΔV_{th} to temperature over 75 °C at $|V_{gst}-V_{th}0|$ = 2.35 V in Fig. 4(b) is not caused by running out of defects, since the longer stress clearly shows that the degradation can be higher.

The temperature insensitivity of ΔV_{th} at a stress time of 1000 s has not been observed for Si/SiO_2 [43] and Si/SiON/high-k [44] and is worth of further exploring. One possibility is that the recovery during the 1-s measurement delay is also a thermally activated process, compensating the degradation. Fig. 5(a)–(d) shows the results measured with t_m = 5 μs that minimized the recovery. The ΔV_{th} appears insensitive to temperature initially (e.g., <1 ms), and the reason is not known at present. For longer stress time, however, it is clearly thermally enhanced and the apparent E_a taken at 1000 s is insensitive to E_{ox} in Fig. 5(d).

To study the anneal of PCs, a device was exposed to 150 °C after stressing at 20 °C. Fig. 6(a) shows that nearly all PCs can

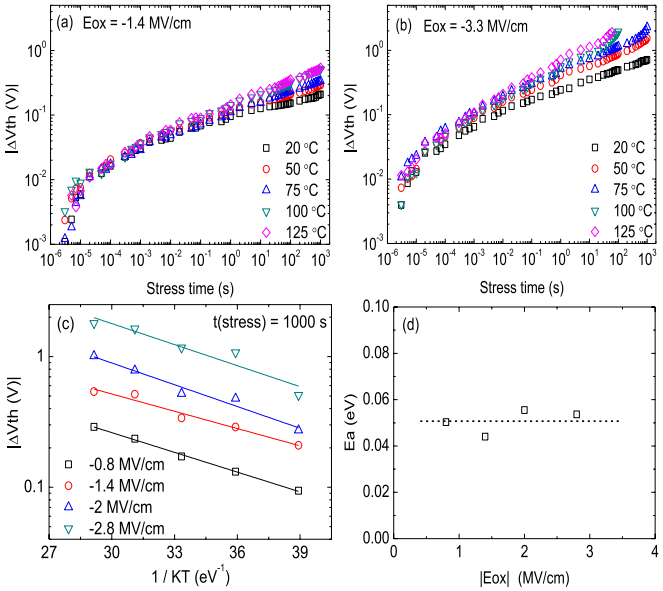

Fig. 5. NBTI kinetics under different stress temperatures with $t_m = 5\ \mu s$. The E_{ox} during stress was kept at a constant of (a) -1.4 MV/cm and (b) -3.3 MV/cm. (c) Arrhenius plot at 1000 s. (d) Extracted apparent activation energy from (c) at different E_{ox}.

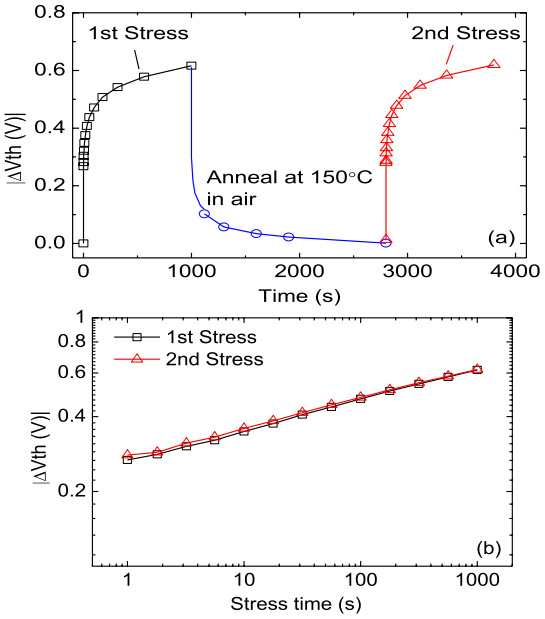

Fig. 6. (a) First stress was under $V_g = -2.8$ V, 20 °C for 1000 s. The device was then annealed for 20 min at 150 °C in air with all terminals floating. The second stress was under the same conditions as the first one. (b) ΔV_{th} for these two stresses by resetting the stress time to zero at the start of the second stress is compared. $t_m = 1$s.

be neutralized in 1800 s. In comparison, the neutralization is less than half for Si/SiON under similar anneal conditions [45]. The following speculation is made to explain this difference.

It has been reported that the PCs in SiO_2 can have energy levels above the bottom edge of the Si conduction band, i.e., E_c, making them difficult to reach by free electrons from Si substrate [17], [31]–[33]. The E_c offset between SiO_2 and Si is around 3.2 eV, so that these traps can be located well above the Si E_c. The E_c offset between GeO_2 and Ge, however, has been reported to be as low as 0.8 eV [46], so that the PC in GeO_2 should be closer to Ge E_c, making them relatively easier to neutralize at elevated temperature.

It is worth pointing out that the PCs in SiO_2 can only be fully neutralized when the anneal temperature reached 400 °C [45], [47]. After the anneal, the ΔV_{th} in the subsequent stress becomes smaller than that before anneal, because of defect losses and slowdown in SiON [45], [47]. To test if this is also the case for $Ge/GeO_2/Al_2O_3$, the device was restressed after anneal, and Fig. 6(b) clearly shows that ΔV_{th} has not been reduced for the restress, so that the defect losses and slowdown were not observed here.

C. Contribution of Generated Interface States

The PCs responsible for NBTI can originate from both the bulk of gate oxide and the oxide/substrate interface [22], [39], [43], [48]. When NBTI was reported for thick SiO_2 (e.g., 95 nm) in early years, the stress E_{ox} was relatively low, and it was observed that PCs from the oxide and the interface were equally important [43]. For thin (<3 nm) oxides, however, the stress E_{ox} used is typically higher (e.g., 10 MV/cm) and hole injection occurs [22], [27]. The charging of hole traps leads to a larger contribution of PCs from oxides to ΔV_{th} than that from generated interface states [22], [30], [49]. Nitridation introduces additional hole traps, further enhancing the contribution of PC from oxides to ΔV_{th} [50], [51]. We now assess the relative importance of PCs from interface states for Ge pMOSFETs of a GeO_2/Al_2O_3 stack.

Fig. 7(a) shows a typical result of charge pumping measurements before and after a stress. The generation of interface states clearly can be seen from the raised peak after stress, resulting in an increase of interface state density of $\Delta D_{it} = 1.88 \times 10^{11}\ cm^{-2}eV^{-1}$. As a first-order estimation of the contribution from ΔD_{it} to ΔV_{th}, we assume a uniform energy distribution of interface states. It has been reported that the charge neutrality level is in the lower half of the bandgap for Ge [52]; but, for simplicity, we assume that all states between the midband and E_v are donor-like and contribute to PCs. This gives rise to a PC of $\Delta N_{it} = 0.33 \times \Delta D_{it} = 6.20 \times 10^{10}\ cm^{-2}$ and a corresponding threshold voltage shift of $\Delta V_{it} = \Delta N_{it} \times q/C_{ox}$ [53]. Fig. 7(b) compares the ΔV_{it} with the measured ΔV_{th}, showing that ΔV_{it} is one order of magnitude smaller.

The ΔD_{it} measured by CP is the average value over an energy range of ± 0.22 eV centered at midgap in our case [54]. It has been reported that the interface state density rises substantially toward the band edge, so that an assumption of uniform energy distribution can underestimate the contribution of ΔD_{it}. As a second-order approximation, we use the energy profile reported in [29] for D_{it}. As shown in Fig. 7(c), the solid curve was fitted with the test data using an expression, $D_{it} = A \times \exp[-(E - Ev)/Eo] + C$, where A, E_o, and C are constants. This function was then normalized to the measured ΔD_{it} over the energy range from midgap to 0.22 eV below it, resulting

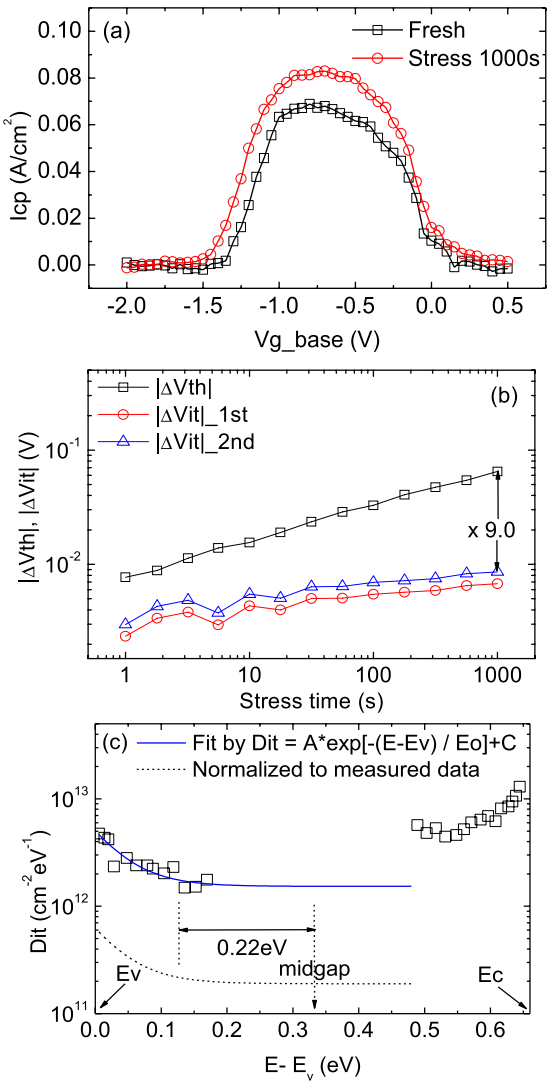

Fig. 7. (a) Charge pumping current, I_{cp}, before and after a stress under $V_{gst} = -1.2$ V at 20 °C. (b) Comparison of the first- and second-order estimated contribution of generated interface states to the threshold voltage shift with the measured ΔV_{th}. (c) Energy distribution reported in [29]. The dashed line is obtained by normalizing the solid line to the measured 1.88×10^{11} $cm^{-2}eV^{-1}$ in the range of 0.22 eV from midgap. The charge pumping amplitude is 1 V, frequency is 1 MHz, and the rise and fall time is 20 ns.

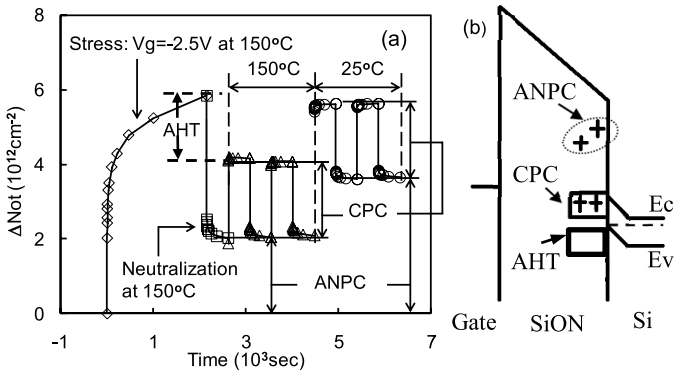

Fig. 8. (a) Three types of PCs in Si/SiON/HfO_2: AHTs, CPCs, and ANPC. After stress and neutralization, $E_{ox} = \pm 5$ MV/cm were applied with alternating polarity first at 150 °C and then 25 °C [39]. $V_g > 0V$ neutralizes CPCs, and $V_g < 0$ V recharges them. (b) Energy level differences for the three types of PCs. ΔN_{ot} was measured from the I_d–V_g shift at midgap, where interface states are neutral for Si MOSFETs.

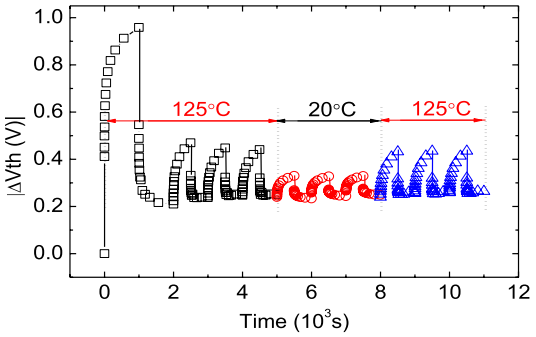

Fig. 9. PCs in Ge/GeO_2/Al_2O_3 device. The stress was at $V_{gst} = -2.6$ V and 125 °C. After a neutralization step at +4.2 MV/cm at 125 °C, $E_{ox} = \pm 3.3$ MV/cm were applied with alternating gate polarity in a temperature sequence of 125 °C, 20 °C, and 125 °C. The time for switching temperature is 40 min with gate floating, and this time was not included in the time axis.

in the dotted line in Fig. 7(c). The PCs were estimated by integrating the dotted line between midgap and E_v, resulting in $\Delta N_{it} = 7.89 \times 10^{10}$ cm^{-2}. The corresponding ΔV_{it} is also shown in Fig. 7(b), and its contribution remains insignificant. The stress in Fig. 7 was at 20 °C. At 125 °C, the measured ΔV_{it} (not shown) can be twice as high as that at 20 °C, but it is still only about 1/8th of the total ΔV_{th}. We conclude that the NBTI of Ge/GeO_2/Al_2O_3 is dominated by PCs in the dielectric.

D. PCs in Dielectric: Energy Switching Model

It has been shown in Sections III-A and B that NBTI in the Ge sample behaves differently from that in Si samples. In this section, the cause for these differences will be investigated at the defect level. For Si pMOSFETs, the PCs in gate oxides have a complex behavior, and have been explained differently by different groups [27], [30], [36], [54]–[57]. Fig. 8(a) and (b) shows their typical behavior, and one framework for characterizing them is to separate them into three types according to their energy ranges: as-grown hole traps (AHTs) below the Si E_v, cyclic positive charges (CPCs) around Si E_c, and antineutralization positive charges (ANPCs) above Si E_c [17], [22], [31]–[33], [44]. After building up PCs during stress at high $|E_{ox}|$, substantial recovery occurs under $V_g > 0$ at a relatively low $E_{ox} = +5$ MV/cm due to the neutralization of AHT and CPC. By alternating the polarity of $E_{ox} = \pm 5$ MV/cm, CPC around Si E_c can be repeatedly charged and neutralized, but the ANPCs well above E_c remain charged and are not neutralized. Most AHTs below Si E_v cannot be recharged under $E_{ox} = -5$ MV/cm. In the following, we will show that PCs in GeO_2/Al_2O_3 on Ge are different.

Fig. 9 shows a typical result for GeO_2/Al_2O_3 on Ge. Although the first impression is that the PCs behave similarly to those in Si samples, a close inspection, however, reveals several important differences.

1) The charge and neutralization of CPC around E_c by alternating V_g polarity for Si samples in Fig. 8(a) is

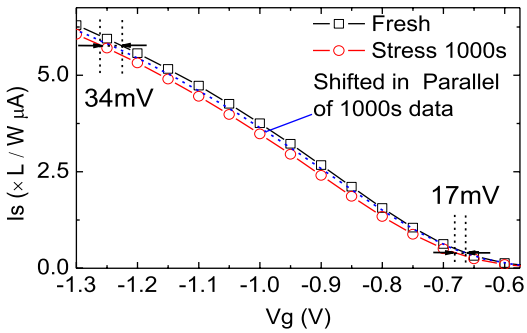

Fig. 10. I_s–V_g before and after stress under $E_{ox} = -6.5$ MV/cm for 1000 s on an Si/SiON/HfO/AlO device. The dotted line is a parallel shift of the line for 1000-s data until it reaches the fresh I_s–V_g at low $|V_g|$. It shows the stressed I_s–V_g is not in parallel with the fresh I_s–V_g.

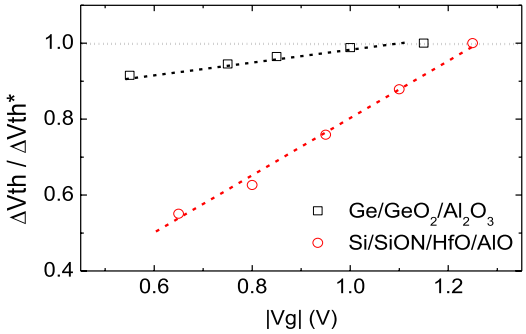

Fig. 11. Dependence of ΔV_{th} on the sensing V_g. ΔV_{th}* is the ΔV_{th} measured at the highest sensing $|V_g|$ for a sample. Devices were stressed under an initial $E_{ox} = -6.5$ MV/cm for 1000 s at 20 °C.

insensitive to measurement temperature, i.e., T, since it has an energy level accessible even at room temperature, and the charge and neutralization are through carrier tunneling here that is a process insensitive to T. In contrast, Fig. 9 shows that the charge/neutralization cycling in Ge sample reduces for lower T.

2) The density of ANPCs above E_c in Si samples in Fig. 8(a) clearly increases at lower T. After being neutralized at a higher T, the defect energy level remains above E_c. As soon as T is reduced, electrons leave the defects, tunnel back into the Si conduction band, recharge the defects, and result in the higher ANPC. For the Ge sample, however, Fig. 9 shows that the remaining PCs hardly increase when the temperature lowers from 125 °C to 20 °C.
3) When V_g sweeps from the stress level in the positive direction to a sensing V_g, some traps in Si samples fall below the Fermi level and are neutralized [22], [27], [30]. It results in the non-parallel I_s–V_g shift shown in Fig. 10 for Si sample. Fig. 11 shows that $|\Delta V_{th}|$ nearly halved when V_g moves from −1.2 to −0.6 V. In contrast, the change of ΔV_{th} with V_g is much smaller for Ge samples (Fig. 11), indicating detrapping from traps below E_v for Ge is less important than that in Si.

The above differences indicate that the PCs in Ge samples are different from those in Si samples, so that a different model is needed. We propose an energy switching model to explain these differences. The first principle calculations show that

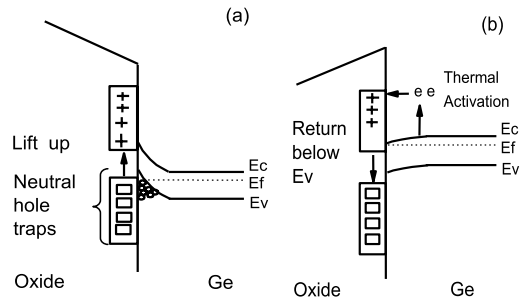

Fig. 12. Energy-switching model for PCs in Ge/GeO_2/Al_2O_3. (a) Charging under $V_g < 0$ and the lifeup of energy level after charging. (b) Neutralization under $V_g > 0$ and the lowering of energy level after neutralization. □ represents neutral hole traps and + represents charged hole traps.

energy levels of a defect in dielectric can strongly depend on its charge states [58], [59]. The energy switching here means that the energy level of a defect switches from one value to another, when its charge state changes. As shown in Fig. 12(a), neutral hole traps have a spread of energy levels below Ge E_v. Application of higher $|E_{ox}|$ allows charging the traps further below E_v, leading to the field activation of NBTI in Fig. 3(a). Application of higher temperature also charges the hole traps further below E_v, resulting in the higher ΔV_{th} at higher temperatures in Figs. 4 and 5.

After being charged, instead of staying at the same energy level, the defects are lifted to energy levels well above Ge E_v. This allows most hole traps holding their PCs when V_g is swept from stress toward threshold levels, giving rise to the smaller reduction in Fig. 11, when compared with that in Si/SiON

If the energy levels of the lifted PCs were near E_c, their neutralization should be insensitive to temperature, similar to the CPC in Si samples in Fig. 8. However, Fig. 9 shows that this is not the case for Ge samples. On the other hand, if the lifted PCs are above E_c, their neutralization should be thermally enhanced, as shown in Fig. 12(b), similar to the ANPC above Si E_c in Fig. 8(b) [17], [31], [44]. This is confirmed below.

Fig. 13 shows that an increase of T clearly lowers ΔV_{th} for both Si [Fig. 13(a)] and Ge [Fig. 13(b)] samples. The thermal activation of neutralization supports the proposition that there are PCs above the Ge E_c. However, when T reduces subsequently, ΔV_{th} rises back for Si, but remains the same for Ge samples. This supports the view that, unlike the case of Si samples, the energy level of defects drops back below E_v after neutralization at high T to prevent recharge at the subsequent low T for Ge sample without restress, as shown in Fig. 12(b). Because the energy level was switched below E_v after neutralization at 125 °C, lowering temperature to 20 °C did not recharge them, unlike the Si sample in Fig. 13(b).

For Ge sample at a time $t*$, a signature of the energy switch after neutralization is that the number of un-neutralized PC is determined by the highest temperature a sample was exposed prior to $t*$, rather than the temperature at $t*$. In contrast, for Si sample, the lack of energy level switching means that the number of un-neutralized PC at $t*$ is determined by the temperature at $t*$. In another word, one may say that Ge/GeO_2/Al_2O_3 can remember its temperature history,

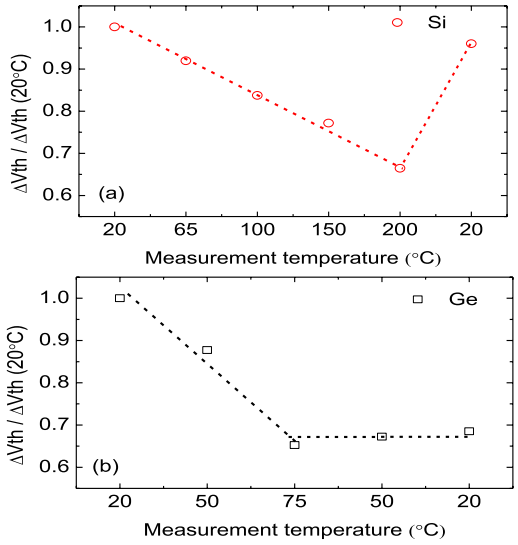

Fig. 13. Impact of measurement temperature on $\Delta V_{\rm th}$ for (a) Si/SiON and (b) Ge/GeO_2/Al_2O_3. The lines are a guide for the eye. $t_{\rm m} = 1$s.

but Si/SiON cannot. The underlying physical mechanism for the energy switching is not known. One speculation is the field-assisted multiphonon emission during hole trapping [55], and further evidences are needed to support it.

IV. Conclusion

This paper characterizes the NBTI for Ge/GeO_2/Al_2O_3 and compares it with Si samples. Similar to Si samples, NBTI is activated both electrically and thermally for Ge/GeO_2/Al_2O_3. There are a number of important differences with Si samples, and the new findings include: 1) the time exponent is not constant for different stress biases/fields when measured with either slow dc or pulse technique, which makes the conventional $V_{\rm g}$ acceleration lifetime prediction technique of Si samples inapplicable to the Ge/GeO_2/Al_2O_3; 2) $\Delta V_{\rm th}$ is substantially less sensitive to measurement time; 3) the neutralization can be nearly 100% under a temperature as low as 150 °C, in contrast with the 400 °C needed by Si sample; and 4) defect losses were not observed for Ge/GeO_2/Al_2O_3.

On defects, the PCs in GeO_2/Al_2O_3 on Ge dominate the NBTI. They do not follow the same framework as that for PCs in SiON/Si, and an energy-switching model has been proposed: the energy levels have a spread for neutral hole traps below $E_{\rm v}$, lift up after charging, and return below $E_{\rm v}$ following neutralization. Finally, we point out that these conclusions are drawn based on the samples used in this paper and their generic applicability awaits further tests.

References

[1] M. Caymax *et al.*, "Germanium for advanced CMOS anno 2009: A SWOT analysis," in *Proc. IEEE IEDM*, Dec. 2009, pp. 428–431.

[2] C. Le Royer, "Interfaces and performance: What future for nanoscale Ge and SiGe based CMOS?" *Microelectron. Eng.*, vol. 88, no. 7, pp. 1541–1548, 2011.

[3] P. C. McIntyre, Y. Oshima, E. Kim, and K. C. Saraswat, "Interface studies of ALD-grown metal oxide insulators on Ge and III–V semiconductors," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1536–1539, 2009.

[4] J. Mitard *et al.*, "Record I(ON)/I(OFF) performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *Proc. IEEE IEDM*, Dec. 2008, pp. 1–4.

[5] A. Asenov *et al.*, "Modeling and simulation of transistor and circuit variability and reliability," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–8.

[6] M. Duan *et al.*, "New analysis method for time-dependent device-to-device variation accounting for within-device fluctuation," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2505–2511, Aug. 2013.

[7] J. Mitard *et al.*, "Impact of Epi-Si growth temperature on Ge-pFET performance," in *Proc. ESSDERC*, Aug. 2009, pp. 411–414.

[8] A. Toriumi, T. Tabata, C. H. Lee, T. Nishimura, K. Kita, and K. Nagashio, "Opportunities and challenges for Ge CMOS-control of interfacing field on Ge is a key," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1571–1576, 2009.

[9] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "High-mobility Ge pMOSFET with 1-nm EOT Al_2O_3/GeO_x/Ge gate stack fabricated by plasma post oxidation," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 335–341, Feb. 2012.

[10] L. Nyns *et al.*, "Interface and border traps in Ge-based gate stacks," *ECS Trans.*, vol. 35, no. 3, pp. 465–480, 2011.

[11] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "Al_2O_3/GeO_x/Ge gate stacks with low interface trap density fabricated by electron cyclotron resonance plasma postoxidation," *Appl. Phys. Lett.*, vol. 98, no. 11, pp. 112902-1–112902-3, 2011.

[12] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High-performance GeO_2/Ge nMOSFETs with source/drain junctions formed by gas-phase doping," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1092–1094, Oct. 2010.

[13] C. H. Lee, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, "High-electron-mobility Ge/GeO_2 n-MOSFETs with two-step oxidation," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1295–1301, May 2011.

[14] B. Kaczer *et al.*, "Electrical and reliability characterization of metal-gate/HfO_2/Ge FET's with Si passivation," *Microelectron. Eng.*, vol. 84, nos. 9–10, pp. 2067–2070, 2007.

[15] J. Franco *et al.*, "SiGe channel technology: Superior reliability toward ultrathin EOT devices—Part I: NBTI," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 396–404, Jan. 2013.

[16] B. Benbakhti *et al.*, "Characterization of electron traps in Si-capped Ge MOSFETs with HfO_2/SiO_2 gate stack," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1681–1683, Dec. 2012.

[17] J. F. Zhang, "Defects and instabilities in Hf-dielectric/SiON stacks (Invited Paper)," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1883–1887, 2009.

[18] J. F. Zhang, C. Z. Zhao, M. B. Zahid, G. Groeseneken, R. Degraeve, and S. De Gendt, "An assessment of the location of as-grown electron traps in HfO_2/HfSiO stacks," *IEEE Electron Device Lett.*, vol. 27, no. 10, pp. 817–820, Oct. 2006.

[19] C. Z. Zhao and J. F. Zhang, "Effects of hydrogen on positive charges in gate oxides," *J. Appl. Phys.*, vol. 97, no. 7, pp. 073703–073708, 2005.

[20] C. Z. Zhao, J. F. Zhang, M. B. Zahid, B. Govoreanu, G. Groeseneken, and S. De Gendt, "Determination of capture cross sections for as-grown electron traps in HfO_2/HfSiO stacks," *J. Appl. Phys.*, vol. 100, no. 9, pp. 093716-1–093716-10, 2006.

[21] N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai, and T. Horiuchi, "The impact of bias temperature instability for direct-tunneling ultra-thin gate oxide on MOSFET scaling," in *Symp. VLSI Technol. Tech. Dig.*, Jun. 1999, pp. 73–74.

[22] J. F. Zhang, Z. Ji, M. H. Chang, B. Kaczer, and G. Groeseneken, "Real Vth instability of pMOSFETs under practical operation conditions," in *Proc. IEEE IEDM*, Dec. 2007, pp. 817–820.

[23] B. Kaczer, J. Franco, J. Mitard, P. J. Roussel, A. Veloso, and G. Groeseneken, "Improvement in NBTI reliability of Si-passivated Ge/high-k/metal-gate pFETs," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1582–1584, 2009.

[24] F. Bellenger *et al.*, "High FET performance for a future CMOS GeO_2-based technology," *IEEE Electron Device Lett.*, vol. 31, no. 5, pp. 402–404, May 2010.

[25] K. Kita *et al.*, "Comprehensive study of GeO_2 oxidation, GeO desorption and GeO_2-metal interaction-understanding of Ge processing kinetics for perfect interface control," in *Proc. IEEE IEDM*, Dec. 2009, pp. 1–4.

[26] J. F. Zhang, I. S. Al-Kofahi, and G. Groeseneken, "Behavior of hot hole stressed SiO_2/Si interface at elevated temperature," *J. Appl. Phys.*, vol. 83, no. 2, pp. 843–850, 1998.

[27] Z. Ji, L. Lin, J. F. Zhang, B. Kaczer, and G. Groeseneken, "NBTI lifetime prediction and kinetics at operation bias based on ultrafast pulse measurement," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 228–237, Jan. 2010.
[28] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI degradation- and recovery-behavior based on ultra fast VT-measurements," in *Proc. IEEE 44th Annu. IRPS*, Mar. 2006, pp. 448–453.
[29] J. Mitard *et al.*, "Investigation of the electrical properties of Ge/high-k gate stack: GeO_2 VS Si-cap," in *Proc. ICSSDM*, 2011.
[30] Z. Ji, J. F. Zhang, M. H. Chang, B. Kaczer, and G. Groeseneken, "An analysis of the NBTI-induced threshold voltage shift evaluated by different techniques," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1086–1093, May 2009.
[31] J. F. Zhang, C. Z. Zhao, A. H. Chen, G. Groeseneken, and R. Degraeve, "Hole traps in silicon dioxides. Part I. Properties," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1267–1273, Aug. 2004.
[32] C. Z. Zhao, J. F. Zhang, G. Groeseneken, and R. Degraeve, "Hole-traps in silicon dioxides. Part II. Generation mechanism," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1274–1280, Aug. 2004.
[33] J. F. Zhang, M. H. Chang, and G. Groeseneken, "Effects of measurement temperature on NBTI," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 298–300, Apr. 2007.
[34] T. Grasser *et al.*, "The paradigm shift in understanding the bias temperature instability: From reaction-diffusion to switching oxide traps," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3652–3666, Nov. 2011.
[35] S. Mahapatra *et al.*, "A comparative study of different physics-based NBTI models," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 901–916, Mar. 2013.
[36] Y. Gao, D. S. Ang, C. D. Young, and G. Bersuker, "Evidence for the transformation of switching hole traps into permanent bulk traps under negative-bias temperature stressing of high-k P-MOSFETs," in *Proc. IEEE IRPS*, Apr. 2012, pp. 5A.5.1–5A.5.5.
[37] *Failure Mechanisms and Models for Semiconductor Devices*, JEDEC, Alexandria, VA, USA, 2011.
[38] S. Pae, J. Maiz, C. Prasad, and B. Woolery, "Effect of BTI degradation on transistor variability in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 3, pp. 519–525, Sep. 2008.
[39] C. Z. Zhao *et al.*, "Stress-induced positive charge in Hf-based gate dielectrics: Impact on device performance and a framework for the defect," *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1647–1656, Jul. 2008.
[40] J. F. Zhang *et al.*, "Dominant layer for stress-induced positive charges in Hf-based gate stacks," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1360–1363, Dec. 2008.
[41] V. D. Maheta, E. N. Kumar, S. Purawat, C. Olsen, K. Ahmed, and S. Mahapatra, "Development of an ultrafast on-the-fly I_{DLIN} technique to study NBTI in plasma and thermal oxynitride p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2614–2622, Oct. 2008.
[42] W. Muth and W. Walter, "Bias temperature instability assessment of n- and p-channel MOS transistors using a polysilicon resistive heated scribe lane test structure," *Microelectron. Rel.*, vol. 44, no. 8, pp. 1251–1262, 2004.
[43] K. O. Jeppson and C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, 1977.
[44] J. F. Zhang *et al.*, "Impact of different defects on the kinetics of negative bias temperature instability of hafnium stacks," *Appl. Phys. Lett.*, vol. 92, no. 1, p. 013501, 2008.
[45] M. Duan *et al.*, "New insights into defect loss, slowdown, and device lifetime enhancement," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 413–419, Jan. 2013.
[46] L. Lin, K. Xiong, and J. Robertson, "Atomic structure, electronic structure, and band offsets at Ge:GeO:GeO_2 interfaces," *Appl. Phys. Lett.*, vol. 97, no. 24, pp. 242902-1–242902-3, 2010.
[47] M. Duan *et al.*, "Defect loss: A new concept for reliability of MOSFETs," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 480–482, Apr. 2012.
[48] S. S. Tan, T. P. Chen, J. M. Soon, K. P. Loh, C. H. Ang, and L. Chan, "Nitrogen-enhanced negative bias temperature instability: An insight by experiment and first-principle calculations," *Appl. Phys. Lett.*, vol. 82, no. 12, pp. 1881–1883, 2003.
[49] M. H. Chang and J. F. Zhang, "On positive charge formed under negative bias temperature stress," *J. Appl. Phys.*, vol. 101, no. 2, pp. 024516-1–024516-7, Jan. 2007.
[50] V. Huard, "Two independent components modeling for negative bias temperature instability," in *Proc. IEEE IRPS*, May 2010, pp. 33–42.
[51] S. W. M. Hatta *et al.*, "Energy distribution of positive charges in gate dielectric: Probing technique and impacts of different defects," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1745–1753, May 2013.
[52] A. Dimoulas and P. Tsipas, "Germanium surface and interfaces (Invited Paper)," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1577–1581, 2009.
[53] T. Aichinger, M. Nelhiebel, and T. Grasser, "Refined NBTI characterization of arbitrarily stressed PMOS devices at ultra-low and unique temperatures," *Microelectron. Rel.*, vol. 53, no. 7, pp. 937–946, 2013.
[54] L. Lin *et al.*, "A single pulse charge pumping technique for fast measurements of interface states," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1490–1498, May 2011.
[55] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "A two-stage model for negative bias temperature instability," in *Proc. IEEE IRPS*, Apr. 2009, pp. 33–44.
[56] Z. Y. Liu *et al.*, "Comprehensive studies of BTI effects in CMOSFETs with SiON by new measurement techniques," in *Proc. IEEE IRPS*, May 2008, pp. 733–734.
[57] T. Grasser, H. Reisinger, P. J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *Proc. IEEE IRPS*, May 2010, pp. 16–25.
[58] D. Liu, Y. Guo, L. Lin, and J. Robertson, "First-principles calculations of the electronic structure and defects of Al_2O_3," *J. Appl. Phys.*, vol. 114, no. 8, p. 083704, 2013.
[59] J. R. Weber, A. Janotti, and C. G. Van de Walle, "Native defects in Al_2O_3 and their impact on III–V/Al_2O_3 metal-oxide-semiconductor-based devices," *J. Appl. Phys.*, vol. 109, no. 3, p. 033715, 2011.

Jigang Ma received the B.Eng. and M.Eng. degrees from Xidian University, Xi'an, China, in 2009 and 2012, respectively. He is currently pursuing the Ph.D. degree in microelectronics with Liverpool John Moores University, Liverpool, U.K.

Jian Fu Zhang received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, and the Ph.D. degree from the University of Liverpool, Liverpool, U.K., in 1982 and 1987, respectively.

He has been a Professor of Microelectronics with Liverpool John Moores University, Liverpool, since 2001. His current research interests include the aging, variability, characterization, and modeling of nanometer-size devices.

Zhigang Ji received the Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2010.

He has been a Lecturer at LJMU since 2011. His current research interests include modeling and defect characterization of MOS devices.

Brahim Benbakhti received the Ing. degree in electronics and the M.Sc. degree in signals and systems from Tlemcen University, Tlemcen, Algeria, and the M.Sc. and Ph.D. degrees in microwave and microtechnology from the University of Lille I, Lille, France, in 1999, 2002, 2003, and 2007, respectively.

He has been a member of the Microelectronics Group, School of Engineering, Liverpool John Moores University, Liverpool, since 2012.

Wei Dong Zhang received Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2003.

He has been a Reader in Microelectronics at LJMU since 2010. His current research interests include reliability assessment of CMOS and memory devices.

Xue Feng Zheng received the B.Eng. and M.Sc. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, and the Ph.D. degree in microelectronics from Liverpool John Moores University, Liverpool, U.K., in 2001, 2004, and 2010, respectively.

He joined the School of Microelectronics, Xidian University, in 2003, where he has been an Associate Professor since 2010.

Jerome Mitard received the Ph.D. degree in microelectronics from the Laboratory of Electronic Information Technology, Grenoble, France, and STMicroelectronics, Grenoble.

He joined imec, Leuven, Belgium, in 2007, as a Device Researcher. He is currently in charge of the sub-10-nm node FINFET.

Ben Kaczer received the M.S. degree in physical electronics from Charles University, Prague, Czech Republic, and the M.S. and Ph.D. degrees in physics from the Ohio State University, Columbus, OH, USA, in 1992, 1996, and 1998, respectively.

He joined the Reliability Group of IMEC, Leuven, Belgium, in 1998, where he is a Principal Scientist.

Dr. Kaczer is currently serving on the IEEE TRANSACTIONS ON ELECTRON DEVICES Editorial Board.

Guido Groeseneken (F'05) received the Ph.D. degree in applied sciences from Katholieke Universiteit Leuven (KU Leuven), Leuven, Belgium, in 1986.

He has been at IMEC, Leuven, since 1987, and a Professor at KU Leuven, since 2001.

Steve Hall (SM'08) received the Ph.D. degree from the University of Liverpool, Liverpool, U.K., in 1987.

He has interests spanning materials characterization, device physics and innovative device design, and gate level circuits.

Dr. Hall sits on the Editorial Advisory Committee of Solid-State Electronics and the Editorial Board of IEEE ELECTRON DEVICE LETTERS.

John Robertson, photograph and biography not available at the time of publication.

Paul R. Chalker received the Ph.D. degree from Cardiff University, Cardiff, U.K.

He is currently a Professor of Materials Science with the School of Engineering, University of Liverpool, Liverpool, U.K.