Comments and Corrections

Corrections to "Suppression of Drain-Induced Barrier Lowering in Silicon-on-Insulator MOSFETs Through Source/Drain Engineering for Low-Operating-Power System-on-Chip Applications"

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Due to an oversight in [1], Figs. 4–9 appeared in black and white in print. They should have printed in color, as shown below:

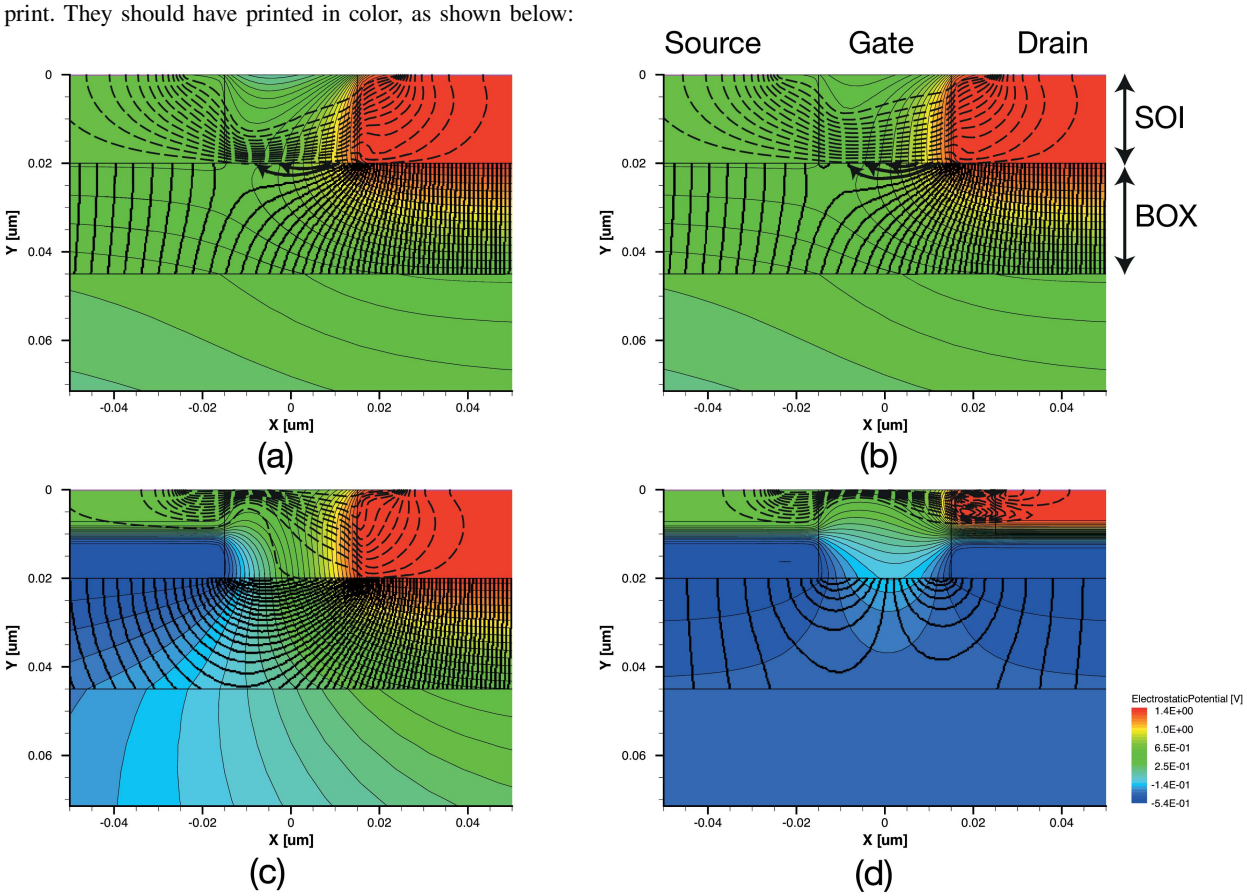

Fig. 4. Cross-sectional views of potential distribution, electric force, and current flow when a threshold voltage is applied to the gate with values of $L_G = 30$ nm and $V_D = 0.9$ V for (a) SOI, (b) retrograde SOI, (c) LCS, and (d) LCSD MOSFETs. Potential is indicated by colors, electrical force is shown by solid lines in BOX regions, and current flow is indicated by broken lines in the SOI layer.

Manuscript received August 30, 2011; revised August 31, 2012 and October 5, 2012; accepted October 9, 2012. Date of publication November 4, 2013; date of current version November 20, 2013. This work was supported in part by a grant for High-Tech Research Centers from the Japan's Ministry of Education, Culture, Sports, Science and Technology (MEXT) from 2008 to 2010, by a grant for the Strategic Development of Advanced Science and Technology from MEXT from 2011 onward, by the VLSI Design and Education Center at The University of Tokyo, and by Synopsys, Inc. The review of this paper was arranged by Editor H. Jaouen.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2286957

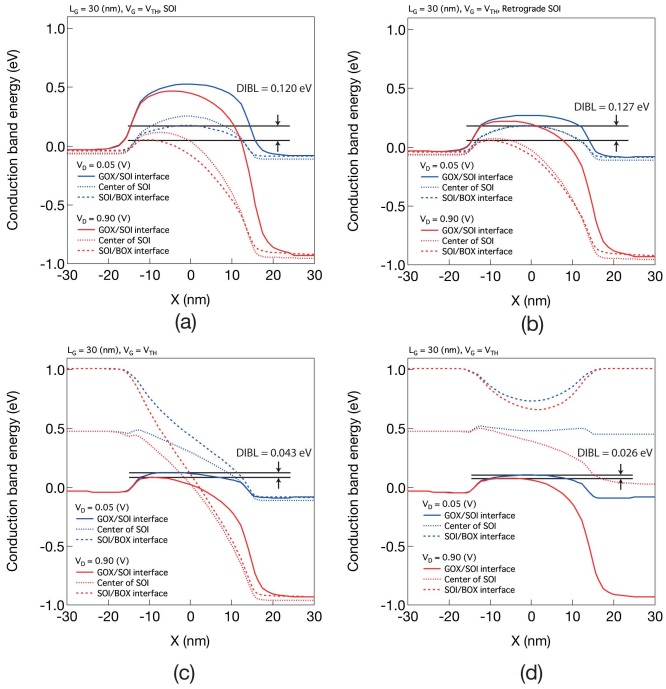

Fig. 5. Cross-sectional distribution of conduction band edge energy in the GOX/SOI interface and at the center of the SOI and SOI/BOX interface when a threshold voltage is applied to the gate with values of $V_{DS} = 0.05$ and 0.90 V for (a) SOI, (b) retrograde SOI, (c) LCS, and (d) LCSD MOSFETs. The differences in maximum conduction band edge energy between $V_{DS} = 0.05$ and 0.90 V in the lowest profile of the body region are shown as DIBL.

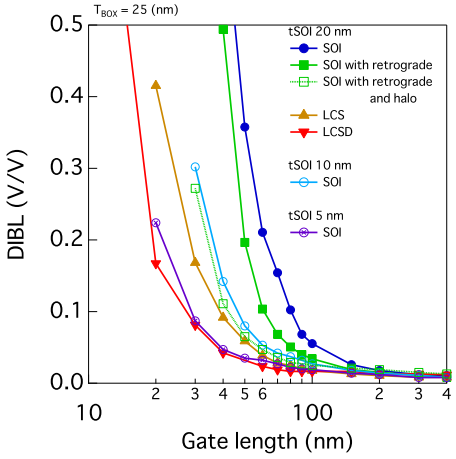

Fig. 6. Gate length dependence of DIBL for SOI, retrograde SOI, LCS, and LCSD MOSFETs.

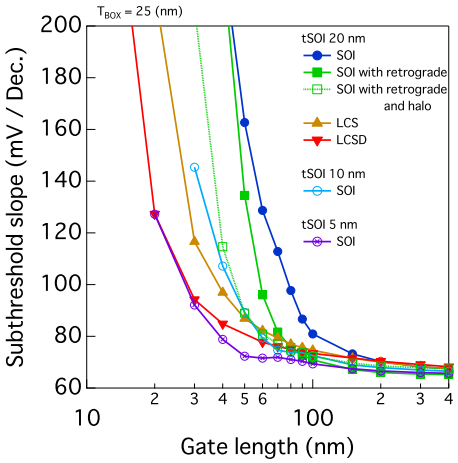

Fig. 7. Gate length dependence of SS for SOI, retrograde SOI, LCS, and LCSD MOSFETs.

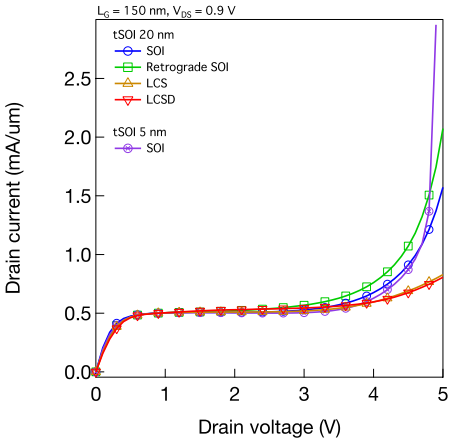

Fig. 8. Drain voltage V_{DS} dependence of drain current I_{DS}.

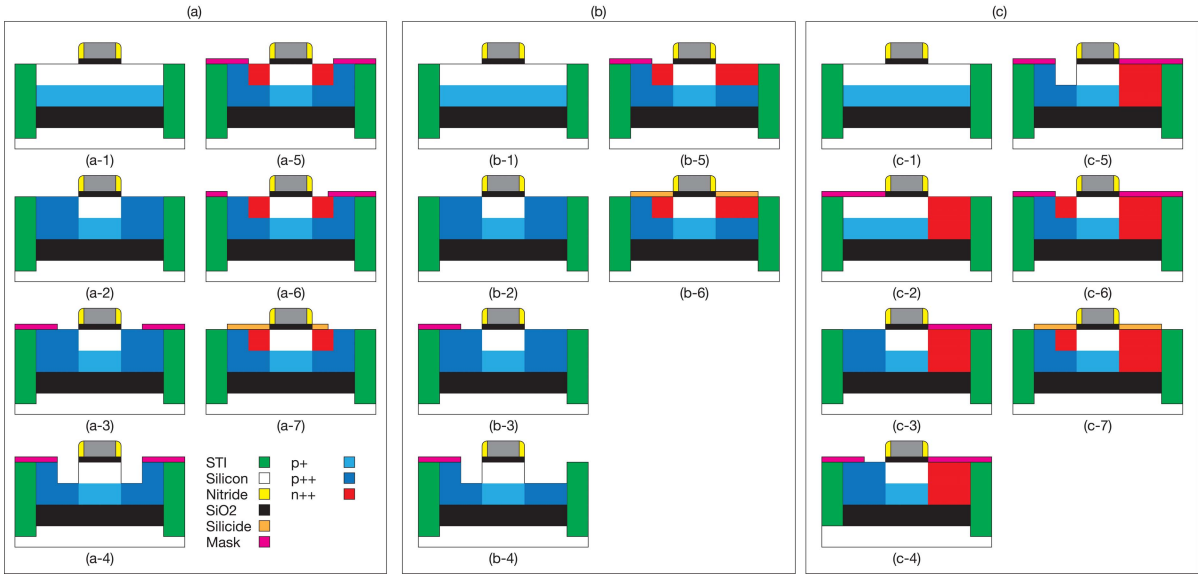

Fig. 9. LCS and LCSD MOSFET process flows.

REFERENCES

[1] T. Yamada, Y. Nakajima, T. Hanajiri, and T. Sugano, "Suppression of drain-induced barrier lowering in silicon-on-insulator MOSFETs through source/drain engineering for low-operating-power system-on-chip applications," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 260–267, Jan. 2013.