Performance Dependence on Width-to-Length Ratio of Si Cap/SiGe Channel MOSFETs

Wen-Teng Chang, *Member, IEEE*, and Yu-Seng Lin

Abstract—This paper measures the *n*- and *p*-MOSFETs fabricated through 65-nm high-*k*/metal gate CMOSFET process flow. The [110] channels of the Si cap on SiGe with different width (*W*) and length (*L*) ratios were compared with Si-only channels. The results show that a high *W–L* ratio in the [110] *n*-channel can alleviate the degradation of biaxial compressive stress. Meanwhile, a low *W–L* ratio in the *p*-channel can improve the performance; however, the ratio should at least be below two in this paper. The dominance of the longitudinal or transverse configurations successfully explains this phenomenon because of the reliance of the different levels of piezoresistance coefficient on the channel orientation. The threshold voltage shifts versus the *W–L* ratio in the *p*-channel is in agreement with the result. The result is verified by a quantitative current comparison at a high bias in the *n*-/*p*-channels between the strained SiGe and Si-only channels, which shows that an extreme *W–L* ratio in the original biaxially strained SiGe channel can result in longitudinal or transverse strain, thereby leading to different levels of performance degradation/improvement.

Index Terms—MOSFET, piezoresistance coefficient, strained SiGe, threshold voltage, transconductance.

I. INTRODUCTION

STRAIN engineering has been used to enhance the electron and hole mobility with uniaxial, biaxial, and combined uniaxial and biaxial strain [1]–[23]. Although local strain uniaxiality has been reported to exhibit high performance with minimum cost [21], researchers have found that anisotropic strain can be channel width dependent and can thus enhance hole mobility when the stress is along the channel length [24]. Many studies have reported that strain is unequally distributed along the channel induced by a uniaxial or biaxial stressor [1]–[6]. The electrical properties related to strain structure have also been reported to be channel length dependent [8]–[12], [16]–[20]. However, only a few studies have focused on the relationship between channel width and length in terms of comparing the impacts of unstrained and strained devices, particularly with decreasing size. Considering that biaxial stress has a longitudinal and transverse orientation, the enhanced or degraded stress level depends
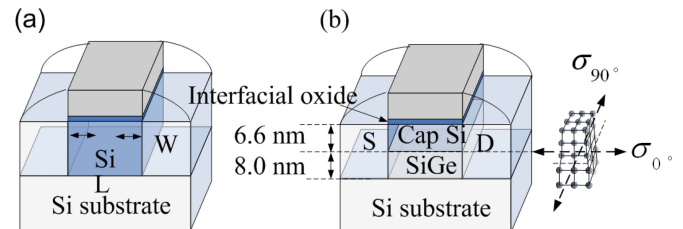
Fig. 1. (a) Silicon-only as a basis for evaluating the performance of (b) silicon cap on strained SiGe channel.

on which configuration is dominant. This inference implies that the dimensional width related to length is critical; the strained channel can produce opposite effective carried mass (mobilities) in the two configurations [15]–[18], [25], [26]. Alatise *et al.* [20] have reported that drain current is enhanced in strained SiGe *p*-MOSFETs when the gate channel is 1 μm, but is degraded when the gate channel is 100 nm. However, the relationship of channel orientation to channel dimension has not been considered in their study. This paper considers various channel dimensions to evaluate the longitudinal or transverse dominance in strained SiGe MOS related to channel dimension. This result implies that an extreme *W–L* ratio in a biaxially strained SiGe channel can result in either longitudinal or transverse strain, which leads to different levels of performance degradation or improvement. This paper could provide useful information when a biaxially strained film is used to enhance MOSFET performance.

II. EXPERIMENTS

The strained $Si_{0.75}Ge_{0.25}$ channel was grown on an Si substrate. The Si-only channel in the MOS was used as a basis for comparison [Fig. 1(a)]. The devices were fabricated with 65-nm high-*k*/metal gate CMOSFET process flow. The selective epitaxial growth significantly improves *p*-MOS [9], [13]. The strained SiGe layer did not only enhance the channel mobility of *p*-MOS, but is also compatible with current CMOS process [22], [23]. However, the postthermal-induced Ge diffusion can induce substantial interface states, wherein one of the solutions is to use a layer of Si cap between SiGe and gate oxide to prevent Ge diffusion. Biaxially compressive strain can enhance the performance of [110] *p*-channel, but can degrade that of *n*-channel; hence, both *n*-/*p*-channels of the strained SiGe and Si-only are useful in studying the tendency of piezoresistance coefficients related to the *W–L* ratio. The SiGe layer is a biaxial compressive strain [Fig. 1(b)] because of the large lattice

constant of SiGe compared with Si, which causes longitudinal ($\sigma_{0°}$) and transverse ($\sigma_{90°}$) stress on the [110] channel. The Hf-based dielectric atomic layer was deposited after interfacial oxide, with a thickness of approximately 1 nm. The thickness of the strained SiGe and Si caps were 8 and 6.6 nm, respectively. The channel width and length ranged from 10 μm to 32 nm. This paper compares the performance of MOS with Si-only and strained SiGe channel by selecting the identical width-to-length (W–L) dimensions. The dc measurements were performed using an Agilent HP4156 semiconductor parameter analyzer with grounded source and body ($V_S = V_B = 0$ V).

III. RESULTS AND DISCUSSION

A. Dependence of n- and p-MOS Enhancement or Degradation on Channel Dimension

Considering that this experiment used the Si-only channel as the basis for comparison, the unstrained and biaxial strained channels with identical dimensions were compared. The normalized transconductance shift ratio or enhancement (degradation) rate (ε_{gm}) of the MOS with capped Si/SiGe channel compared with the Si-only channel is defined as follows:

$$\varepsilon_{gm} = \frac{g_{m,w/SiGe} - g_{m,Si\,only}}{g_{m,Si\,only}}. \tag{1}$$

Ignoring the dimension deformation, this ratio was used to calculate the normalized mobility shifting induced by strained SiGe compared with the mobility of the Si-only channel (μ), that is

$$\varepsilon_{gm} \approx \frac{\mu_{strained} - \mu}{\mu} = \frac{\Delta\mu}{\mu} \tag{2}$$

where $\Delta\mu$ is the mobility shift caused by the biaxial stress of the capped Si/SiGe. Fig. 2(a)–(c) shows the transconductance (g_m) of Si-only (empty marks) and strained SiGe (solid marks) n-channel MOSFETs with channel width of 10, 1, and 0.08 μm, respectively. These figures show that all the g_m values of the Si-only n-channel are higher than those of capped Si/SiGe n-MOSFETs. ε_{gm} deteriorates as the W–L ratio becomes smaller (W decreases or L increases). This result can be explained by the tendency of the strain to have a longitudinal or transverse strained configuration, and can be quantified using the piezoresistance coefficients of the [110] channel. Although the piezoresistance coefficients of $Si_{0.75}Ge_{0.25}$ are unclear, the longitudinal and transverse configurations of Si and SiGe were measured in a similar range (Table I) [26], [27]. Table I shows that the coefficients are negative for the n-channel in both longitudinal ($\pi_{0°}$) and transverse ($\pi_{90°}$) configurations under compressive stress. Nevertheless, the n-channel in the longitudinal configuration has higher (more negative) piezoresistance coefficients ($\pi_{0°}$) compared with that of the transverse configuration ($\pi_{90°}$). The piezoresistance coefficient (π) is defined as the normalized resistivity change ($\Delta\rho/\rho$) over applied stress as follows:

$$\pi = \left|\frac{\Delta\rho/\rho}{\Delta T}\right| \approx \left|\frac{\Delta\mu/\mu}{\Delta T}\right|_{Fixed\,Dim.} = \frac{\Delta g_m/g_m}{\Delta T} = \frac{\varepsilon_{gm}}{\Delta T} \tag{3}$$

where the absolute value of $\Delta\rho/\rho$ is approximate to ε_{gm} because resistivity varies only slightly. The stress (ΔT) of the
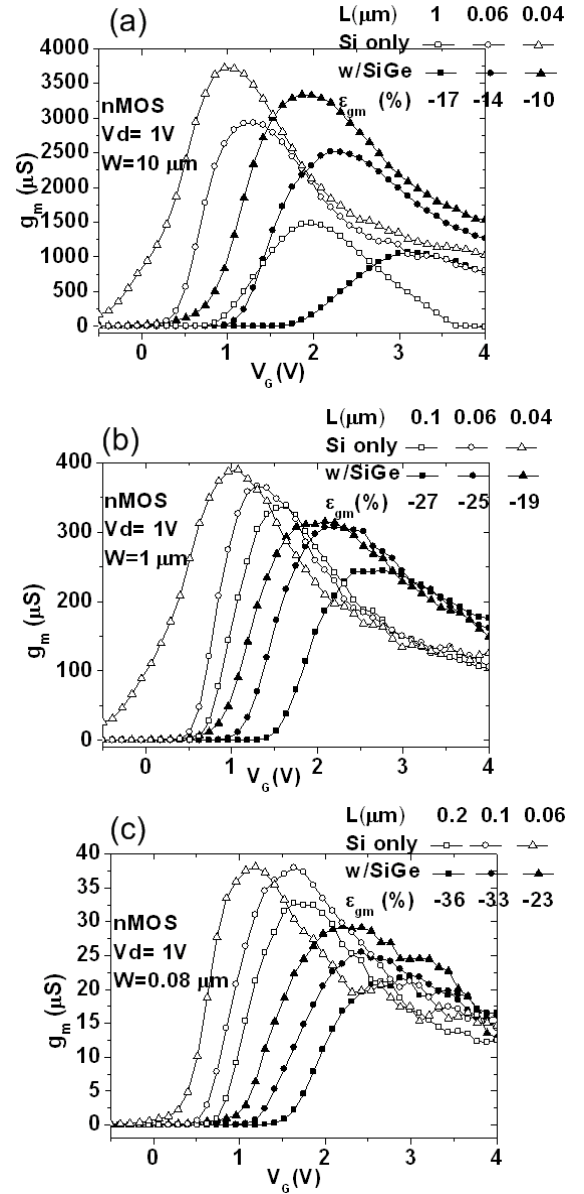

Fig. 2. Transconductance of Si-only and capped Si/SiGe nMOSFETs with channel width of (a) 10, (b) 1, and (c) 0.08 μm.

TABLE I

PIEZORESISTANCE COEFFICIENTS (π) OF [110] Si- AND SiGe-BASED MOS LONGITUDINAL AND TRANSVERSE TO THE CHANNEL [26], [27]

Si / SiGe ($\times 10^{-11}$Pa)	n-channel	p-channel
$\pi_{0°}$	-52– -32 / -52	41.5– 90 / 125
$\pi_{90°}$	-35 – -14.5 / -20	-56.3 – -38.5 / -52

biaxially strained SiGe can be decomposed into longitudinal ($\Delta T_{0°}$) and transverse ($\Delta T_{90°}$) stress as follows:

$$\Delta T = \alpha\,\Delta T_{0°} + \beta\,\Delta T_{90°} \tag{4}$$

where α and β are the coefficients dependent on the W–L ratio. The stress in the longitudinal configuration becomes dominant (high α/β) when n-MOS has a small W–L ratio. This finding agrees with the results in Figs. 2(a)–(c), which
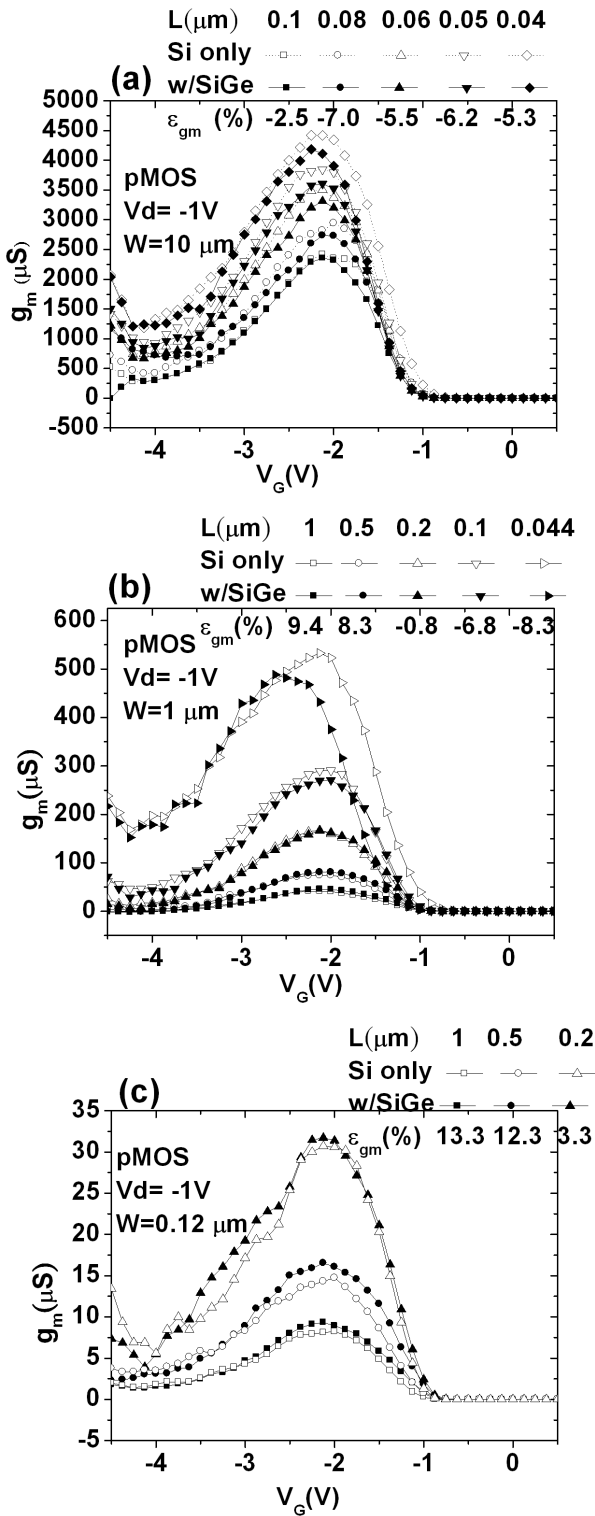
Fig. 3. Transconductance of Si-only and capped Si/SiGe pMOSFETs with channel width of (a) 10, (b) 1, and (c) 0.12 μm.
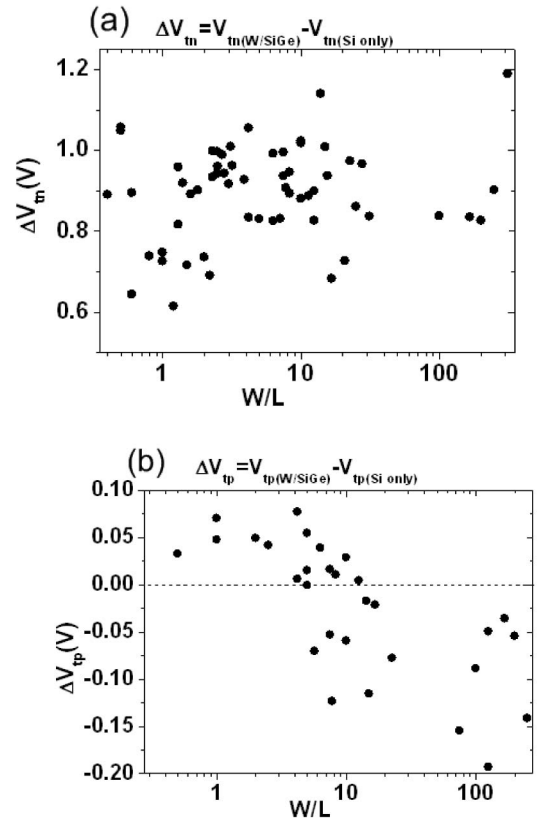

Fig. 4. Threshold voltage shifts as a function of W/L ratio in (a) nMOS and (b) pMOS.

degradation rather than enhancement when strained SiGe is applied. Fig. 3(b) shows a medium W–L ratio from 1 (1/1) to 22 (1/0.044). The result shows that ε_{gm} shifts from negative to positive when the W–L ratio is approximately two to five (W–L = 1/0.5 and 1/0.2). Fig. 3(c) shows the minimum W/L ratio, which shows that strained SiGe is effective in enhancing g_m. These results show that the strained SiGe p-channel only enhances g_m with a small W–L ratio. ε_{gm} can reach up to 13% when the W–L ratio is 0.12. This phenomenon is well explained by the orientation–dominance approach. A high W–L ratio results in $\alpha \ll \beta$, leading to a dominant transverse configuration with negative piezoresistance coefficients ($\pi_{90°}$) of Si and SiGe, as shown in Table I. On the contrary, for a small W–L ratio, as in Fig. 3(c), $\alpha \gg \beta$, the piezoresistance coefficients ($\pi_{0°}$) of Si and SiGe are positive for this longitudinal configuration. Therefore, a high W–L ratio leads to degradation, whereas a small W–L ratio leads to enhancement in the p-channel.

B. Threshold Voltage Shifts Related to Dimension

Fig. 4(a) and (b) shows the threshold voltage shifts as a function of the W–L ratio in n- and p-MOS, respectively. The shifting threshold voltage in n-MOS exhibits a slightly positive trend in relation to the W–L ratio, whereas that in p-MOS exhibits a significant negative trend in relation to the W–L ratio. ΔV_{tp} becomes positive when the W–L ratio decreases to the values in the range of four and 10. Studies have reported that a negative ΔV_{tp} in the p-channel shows that V_{tp} increases by increasing the strain and vice

shows that a low W–L ratio causes ε_{gm} to deteriorate. The extreme example in Fig. 2(a) shows that a W–L ratio of 250 (W/L = 10/0.04 μm) may lead to $\sigma_{90°}$ dominance, which shows an inclination toward uniaxial stress.

Fig. 3(a)–(c) shows the transconductance (g_m) of Si-only and strained SiGe p-channel MOSFETs with channel width of 10, 1, and 0.12 μm, respectively. Fig. 3(a) shows a large ratio of W–L at W =10 μm. Surprisingly, ε_{gm} shows g_m

Fig. 5. Log (ID) versus $(V_G - V_t)$ plot for the n-channel. (a) $L = 1$ μm for various W. (b) $W = 0.25$ μm for various L. (c) $I_D - V_D$ curves for the n-channel with Si only and cap Si/SiGe.
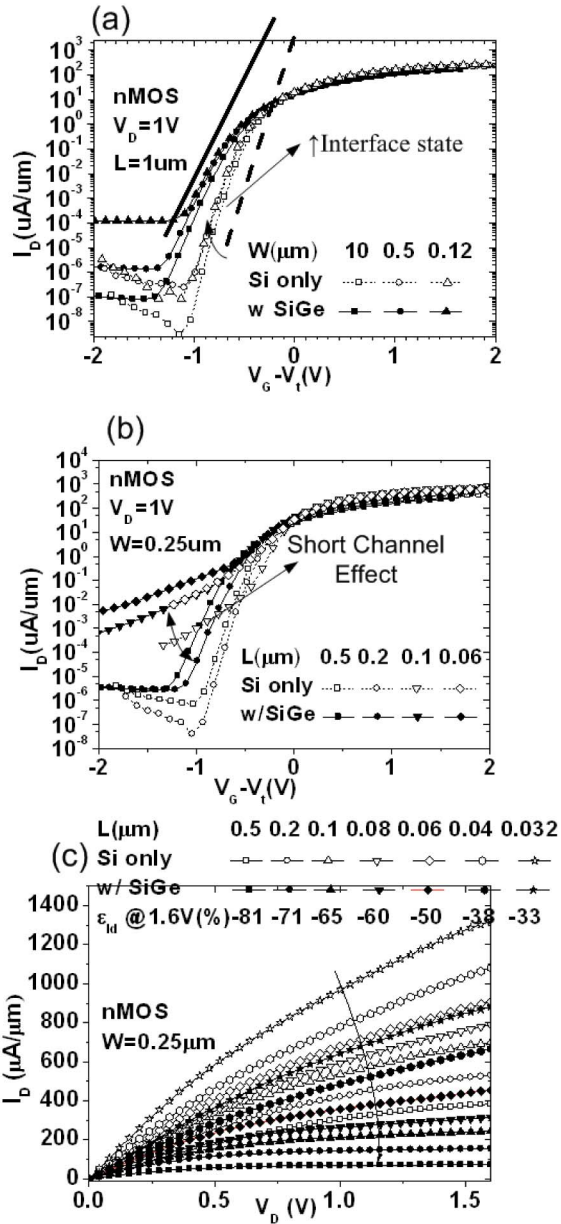

Fig. 6. Log (I_D) versus $(V_G - V_t)$ plot for the p-channel. (a) $L = 0.1$ μm for various W. (b) $W = 0.25$ μm for various L. (c) $I_D - V_D$ plot and W/L ratio of ID enhancement quantification in strained SiGe for $W = 0.5$, 0.25 and 0.14 μm at $L = 0.1$ μm.

versa [10], [11]. This result agrees with the result the g_m enhancement/degradation reversion shown in Fig. 3(a)–(c), in which the position of the V_G apex in the Si-only and capped Si/SiGe channels (i.e., ΔV_t) reverses.

C. Drain Current Behavior Related to Dimension

Fig. 5(a) and (b) shows the log (I_D) versus $(V_G - V_t)$ plot for the n-channel at $L = 1$ μm for various W and $L = 0.25$ μm for various L, respectively. Fig. 5(a) and (b) shows that the subthreshold slopes in the cap Si/ SiGe n-channel are lower than those in the Si-only n-channel, which shows that the strained SiGe in MOS has higher interface states than in the Si-only [28]. The drain-induced barrier lowering effect causes V_t to decrease with the decrease in L, as shown in Fig. 5(b). Similarly, the normalized current shift ratio (ε_{ID})
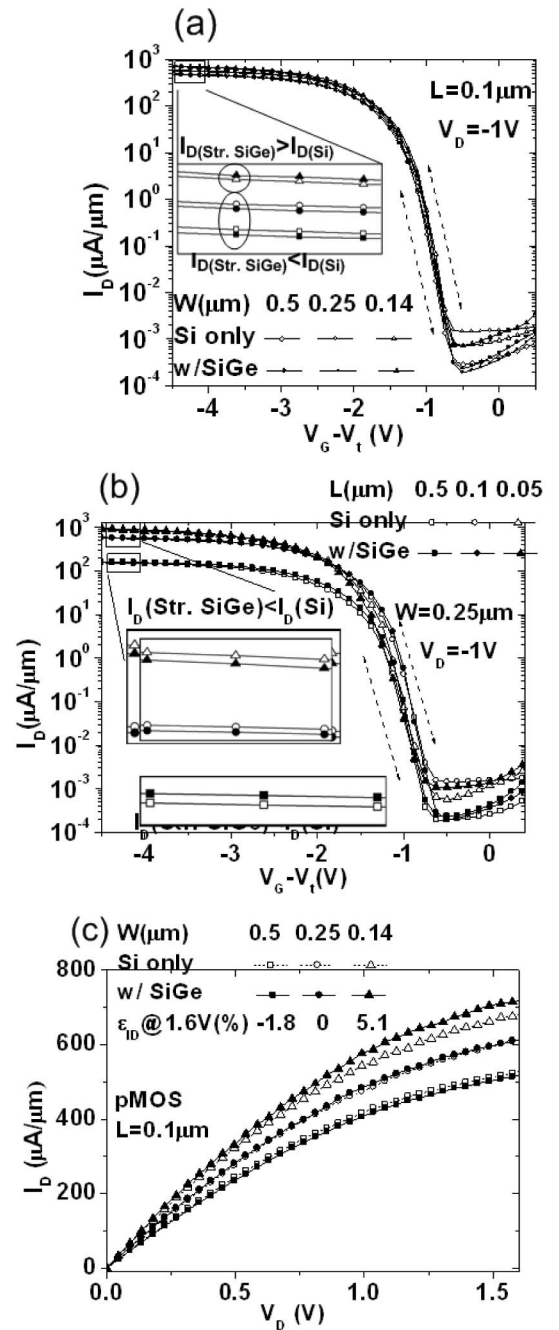
of the strained SiGe channel $(I_{D(\text{Str.SiGe})})$ compared with the Si-only channel $(I_{D(\text{Si})})$ is defined as follows:

$$\varepsilon_{ID} = \frac{I_{D(\text{Str.SiGe})} - I_{D(\text{Si})}}{I_{D(\text{Si})}}. \tag{5}$$

The result shows that ε_{ID} becomes more negative with decreasing W/L ratio in MOS (c), which agrees with the findings obtained using transconductance.

Fig. 6(a) and (b) shows the log (I_D) versus $(V_G - V_t)$ plot for the p-channel at $L = 0.1$ μm for various W and $W = 0.25$ μm for various L, respectively. The local saturation

area magnified in the insets shows that the current difference in the strained SiGe ($I_{D(Str.SiGe)}$) and Si-only ($I_{D(Si)}$) of p-MOS can change with dimension. Fig. 6(b) shows that the drain current density of the strained p-channel becomes higher than that of the unstrained p-channel when the W–L ratio is less than 2.5 (W–L = 0.25/0.1). This finding agrees with the finding in Fig. 3. The insignificant difference in the subthreshold slopes of the strained and unstrained channels shows small ΔV_t. Fig. 6(c) shows the I_D–V_D plot around the critical W–L ratio for the strained SiGe of W = 0.5, 0.25, and 0.14 μm at L = 0.1 μm. The quantification shows that the threshold ratio to enhance I_D is W/L = 2.5.

IV. CONCLUSION

This paper employed 65-nm high-k/metal gate CMOSFET process flow to fabricate a capped Si/SiGe channel, which was then compared with an Si-only channel. The results show that a high W–L ratio in the [110] n-channel can alleviate the degradation of biaxial compressive stress. Meanwhile, a low W–L ratio in the p-channel can improve performance, but the threshold ratio should at least be below two. Nevertheless, this threshold ratio could be varied with reduction of dimensions of a MOS because the strain is unequally distributed along the channel. Aside from the scaling effect, the thickness of Si cap and SiGe is critical to determine the performance of the p-MOSFETs. A thick Si cap reduces the total hole mobility by inducing a parasitic channel in the Si cap with lower hole mobility, whereas a thin Si cap increases the interface state, which degrades the transistor performance. A tensile strain within the Si capping can also depend on its thickness [29]. An optimal Si cap/SiGe thickness ratio of 0.9 was thus found from [5].

The channel dimension W–L ratio can determine the dominance of the longitudinal or transverse configurations. These configurations further determine the amount of enhancement or degradation because of the different piezoresistance coefficients of the channel orientation. This result implies that an extreme W–L ratio in a biaxially strained SiGe channel can result in either longitudinal or transverse strain, which leads to different levels of performance degradation or improvement. Therefore, we believe that this paper can be further applied to tensile strained layers, such as silicon carbide channels.

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