Guest Editorial
Special Issue on GaN Electronic Devices

WITH the continuous demanding of performance in the wireless communication market and the need of more efficient power conversion systems, microwave and power transistors are playing critical roles in many aspects of human activities. In mobile communication applications, next-generation cellphones and basestations require wider bandwidth and improved efficiency. In parallel, the power electronics market is looking at new devices with enhanced performances to further reduce power conversion losses for a more efficient energy usage at silicon cost levels.

Over the last decade, GaN-based high electron mobility transistors (HEMTs) have emerged as excellent devices for a number of applications. Devices with f_T in excess of 300 GHz at $L_g = 30$ nm, a power-added efficiency (PAE) of 73% at 4 GHz frequency and 45 V drain bias, and output power density in excess of 40 W/mm have been demonstrated, thus clearing the way for the adoption of HEMTs in high power/frequency systems. In addition, GaN technology now offers transistor, diode and even IC's compatible with power electronic expectations, at least in the 0−600 V range.

Most of the commercial applications of III-N electronics today are in the field of solid-state radar and mobile communication base stations. The intrinsic advantage to form compact and simple broadband power amplifiers has introduced this technology much faster than anybody anticipated. Further, there are strong hopes in the power business to use the simplicity of compact converters to save energy in the field of power conversion. Last but not least, III-N devices offer the chance to close the solid-state millimeter-wave power gap to achieve watt-level operation per chip in the frequency range of 100 GHz and beyond.

However, GaN electronic devices still face great challenges related to the development of new device architectures, techniques for normally-off operation with large threshold voltage, gate scaling, substrate costs, thermal management, packaging, degradation modes and mechanisms not yet fully understood, that today are limiting the market penetration of GaN-based devices.

Due to the rapid advances taking place in the development and application of GaN electronics, there is an immediate need to take cognizance of the recent technological improvements and bring the potential and opportunities that exist in the area to a wider device community. The primary goal of this special issue is, therefore, to put together works in different aspects, including modeling, design, technology, characterization and applications so that this special issue will not only be of great archival value but also attract new researchers into this area for further accelerating the application of III-N devices in building reliable, cheaper, and high-performance electronic systems.

The papers collected in this special issue have been grouped into six topics.

1) Fabrication and characterization of GaN-based devices.
2) High power GaN HEMTs for power switching applications.
3) High speed GaN HEMTs for RF applications.
4) Reliability and parasitic issues in GaN HEMTs.
5) Simulation-based development of GaN HEMTs devices.
6) GaN-based low noise amplifiers and gate drive circuits.

I. Fabrication and Characterization of GaN-Based Devices

The first invited paper in this section "Scaling of GaN HEMTs and Schottky Diodes For Sub-Millimeter-Wave MMIC Applications" by Shinohara *et al.* from HRL Laboratories, reports the state-of-the-art high frequency performance of GaN-based HEMTs and Schottky diodes. Ultrahigh f_T, exceeding 450 GHz and f_{max} close to 600 GHz were obtained in deeply-scaled GaN HEMTs while maintaining superior Johnson figure of merit (*JFoM*). Excellent low-power noise performance and DCFL ring oscillator circuits are demonstrated.

In the second invited paper "Current Stability in Multi-mesa-Channel AlGaN/GaN HEMTs" by Ohi *et al.* from Hokkaido University, Sapporo, and CREST (Japan Science and Technology Agency) multimesa-channel (MMC) AlGaN/GaN HEMTs are fabricated and characterized. The advantageous properties with respect to device scaling are discussed.

The third paper "p-Channel Enhancement and Depletion Mode GaN-based HFETs with Quaternary Backbarriers" by Hahn *et al.* from RWTH Aachen, Germany provides a comprehensive study of enhancement and depletion mode p-channel GaN/AlInGaN heterostructure field effect transistors.

Two research groups from South Korea (Kyungpook National University and Samsung Electronics Co., Ltd) and France (University of Montpellier II and IMEP-MINATEC) present in the paper "High-Performance GaN-based Nanochannel FinFETs With/Without AlGaN/GaN Heterostructure" by Im *et al.* two types of fin-shaped field-effect transistors (FinFETs), one with AlGaN/GaN heterojunction and the other with heavily doped heterojunction-free GaN layer operating in junctionless mode, and provides a performance comparison.

The group from the Hong Kong University of Science and Technology reports in "DC and RF Performance of Gate-last

Digital Object Identifier 10.1109/TED.2013.2278653

0018-9383 © 2013 IEEE

AlN/GaN MOSHEMTs on Si with Regrown Source/Drain" by Huang *et al*., on the fabrication and characteristics of self-aligned gate-last AlN/GaN metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs). They feature regrown source/drain for low on-state resistance (R_{on}).

The sixth paper "Sidewall Dominated Characteristics on Fin-Gate AlGaN/GaN MOS-Channel-HEMTs" by Takashima *et al*. from Fuji Electric and Rensselaer Polytechnic Institute concerns fin-gate structures. They were fabricated onto AlGaN/GaN MOS channel-high electron mobility transistors (MOSC-HEMTs), and the fin sidewall contribution to the MOS channel characteristics was investigated. The results demonstrate sidewall-dominated characteristics of these FIN-MOSC-HEMTs.

In the next paper "AlGaN/GaN-Based Lateral-Type Schottky Barrier Diode with Very Low Reverse Recovery Charge at High Temperature" by Lee *et al*. from Samsung Electronics and Kyungpook National University (South Korea), lateral multifinger type Schottky barrier diode (SBD) are discussed with bonding pad over active (BPOA) structure fabricated on the AlGaN/GaN heterostructure prepared on sapphire substrate. They exhibited excellent device characteristics such as forward current and reverse recovery in comparison to silicon devices.

The paper "Fabrication and Characterization of Enhancement-Mode High-κ $LaLuO_3$-AlGaN/GaN MIS-HEMTs" by Yang *et al*. from the Hong Kong University of Science and Technology, the Chinese Academy of Sciences and Peter Grünberg Institute (Germany), proposes enhancement-mode (E-mode) $LaLuO_3$-AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) fabricated using fluorine (F) plasma ion implantation.

Finally, the paper entitled "AlGaN/GaN Three Terminal Junction Devices for Rectification and Transistor Applications on 3C-SiC/Si Pseudosubstrates" by Hiller *et al.* from Technische Universität Ilmenau, Germany, describes three terminal junction devices featuring an in-plane side gate that is capable of modulating current flow at a nanoscale junction fabricated on AlGaN/GaN heterojunctions. The process techniques and mechanisms for rectification and transistor operations are discussed.

II. High Power GaN HEMTs for Power Switching Applications

This section starts with two invited papers describing advanced technology for next-generation GaN power switching applications.

The first paper "GaN on Si Technologies for Power Switching Devices" by Ishida *et al.,* from Panasonic, Japan, the device technology for fabricating normally-off GaN-based gate injection transistors (GITs) on 200 mm Si substrates is described. GaN-based GIT's are further implemented in a three-phase inverter for motor drive applications, delivering a high efficiency of 99.3% at a high output power of 1500 W.

The second paper entitled "Lateral and Vertical Transistors Using the AlGaN/GaN Heterostructure" by Chowdhury *et al.* from Arizona State University and Transphorm, USA, provides a comprehensive overview on the latest development in lateral and vertical power switching devices featuring AlGaN/GaN heterostructures. The application-specific benefits and challenges of the lateral and vertical device structures and technology are discussed.

Utilizing pseudo-bulk GaN substrates, the third paper entitled "High Voltage Vertical GaN PN Diodes with Avalanche Capability" by Kizilyalli *et al.* from Avogy Inc., San Jose, USA reports on vertical GaN PN diodes with breakdown voltages of 2600 V and a differential specific on-resistance of 2 mΩ-cm^2. A positive temperature coefficient of the breakdown voltage is observed, indicating that the breakdown is due to impact ionization and avalanche.

The next two papers in this section focus on the technology of MIS-HEMTs that possess desirable features for power switching applications, but also face challenging issues regarding to the gate dielectric.

The paper entitled "Fabrication and Performance of Au-free AlGaN/GaN-on-Silicon Power Devices with Al_2O_3 and Si_3N_4/Al_2O_3 Gate Dielectrics" by Van Hove *et al.* from IMEC, Belgium, presents GaN-based MIS-HEMTs fabricated on 150-mm Si substrates using an Au-free process. Both single-layer Al_2O_3 and bilayer (with *in situ* Si_3N_4 and *ex situ* Al_2O_3) gate dielectrics are investigated with the latter showing robust performance and a breakdown voltage over 600 V.

The paper entitled "High Drain Current Density E-mode Al2O3/AlGaN/GaN MOS-HEMT on Si with Enhanced Power Device Figure-of-Merit (4×10^8 V^2 $W^{-1}cm^{-2}$)" by Freedsman *et al.* from Nagoya Institute of Technology reports on the enhancement-mode (E-mode) Al_2O_3/AlGaN/GaN MIS-HEMTs. The E-mode operation is obtained by utilizing the negative charges in the Al_2O_3 gate dielectric deposited by atomic layer deposition.

The last paper entitled "Improved Vertical Isolation for Normally-off High Voltage GaN-HFETs on n-SiC Substrates" by Hilt *et al.* from Ferdinand-Braun-Institut, Berlin, Germany, presents an argon implantation technique for improving the vertical isolation in lateral normally-off high voltage AlGaN/GaN heterojunction FET's on n-SiC substrates. Vertical leakage reduction and breakdown voltage improvement are achieved.

III. High Speed GaN HEMTs for RF Applications

Each one of the four papers in this section pushes the state-of-the-art in GaN-based transistors for RF applications.

The first invited paper "AlInN-Based HEMTs for Large-Signal Operation at 40 GHz," by Tirelli *et al.* from ETH-Zürich, Switzerland, studies the impact of GaN and AlN capping layers on the performance of AlInN/GaN HEMTs. It is found that while AlN-capped epilayers have higher current levels and reduced dispersion, the GaN-cap improves channel control. A maximum power density of 5.8 W/mm is achieved on GaN-capped InAlN/GaN transistors.

In a second invited paper "InAlN Barrier Scaled Devices for Very High f_T and for Low-Voltage RF Applications" by

Saunier *et al*. from TriQuint Semiconductor, the microwave and mm-wave performance is studied of InAlN/AlN/GaN HEMTs with gate lengths in the 30 to 50 nm range. Both enhancement-mode and depletion-mode devices are reported with frequency performance well in excess of 200 GHz. Excellent large signal performance at 30 GHz and a noise figure of 0.25 dB at 10 GHz are demonstrated.

The third paper, "Optimization of $Al_{0.29}Ga_{0.71}N$/GaN High Electron Mobility Heterostructures for High Power/Frequency Performances," by Rennesson *et al*. from CNRS-CRHEA and IEMN (Lille), France, studies the optimization of AlGaN/GaN transistor structures grown on a Silicon substrate to maximize their high power and frequency performance. A power density of 1.5 W/mm at 40 GHz is obtained after finding the best trade-off between barrier layer thickness and electrostatic channel control.

The RF Devices section concludes with the paper "High-gain Millimeter-Wave AlGaN/GaN Transistors" by Schwantuschke *et al*. from Fraunhofer Institute for Applied Solid State Physics, Freiburg, Germany, on high-gain mm-wave AlGaN/GaN transistors. The paper demonstrates dual-gate devices for substantial improvement in bandwidth and gain per stage at the circuit level.

IV. Reliability and Parasitic Issues in GaN HEMTs

This section start with an invited paper "AlGaN/GaN-Based HEMTs Failure Physics and Reliability: Mechanisms Affecting Gate Edge and Schottky Junction" by Zanoni *et al.* from the University of Padova, Italy, reporting a comprehensive review of AlGaN/GaN HEMT reliability related failure modes and mechanisms focusing on the well-known gate-drain edge degradation issue. Physical effects at the origin of device degradation (inverse piezoelectric effect, time dependent trap formation and percolative conductive paths formation, and electrochemical AlGaN and GaN degradation) are discussed.

In the second paper "Reliability Analysis of Permanent Degradations on AlGaN/GaN HEMTs" by Marcon *et al.* by IMEC, Belgium, and the University of Padova, Italy, a detailed report on the understandings on the two most common failure modes of GaN-based HEMTs is presented, namely, permanent gate leakage current increase and output current drop.

The following three papers of this section, presents electro-mechanical numerical simulations addressing both reliability issues and device performances.

In "AlGaN/GaN HEMT Degradation: An Electro-Thermo-Mechanical Simulation" by Auf der Maur *et al.* from the University of Rome Tor Vergata, Italy, fully self-consistent degradation simulation results are presented, based on an electro-thermo-mechanical model of a typical AlGaN/GaN HEMT structure. The mechanical stress state is analyzed under different DC operating conditions identifying possible dislocation formation and movement.

In the paper "Impact of Intrinsic Stress in Diamond Capping Layers on the Electrical Behavior of AlGaN/GaN HEMTs" by Wang *et al.* from Universidad Politécnica de Madrid, Spain, the Naval Research Laboratory, Washington, and the University of Bristol, Bristol, U.K., the impact of intrinsic stress in diamond capping layers is reported on the electrical behavior of AlGaN/GaN HEMTs.

Then, the paper "Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling" from Turuvekere *et al.* from IIT Madras and Tata Institute of Fundamental Research, Mumbai, India, reports on the gate leakage mechanisms in AlInN/GaN and AlGaN/GaN HEMTs; the reverse bias gate current has been decomposed it into three components: thermionic emission (TE), Poole-Frenkel (PF) emission and Fowler-Nordheim (FN) tunneling.

The second part of this reliability section deals with the very critical problem of charge trapping and traps identification in GaN-based HEMTs.

The sixth paper "Deep Levels Characterization in GaN HEMTs-Part I: Advantages and Limitations of Drain Current Transient Measurements" by Bisi *et al.* from the Universities of Padova and Modena & Reggio Emilia, Italy, and Fraunhofer Institute, Freiburg, Germany, investigates the advantages and limitations of the current-transient methods adopted for the study of the deep levels in GaN-based HEMTs; they also present a database of defects described in more than 60 papers on GaN technology which can be used to extract information on the nature and origin of the trap levels responsible for current collapse in AlGaN/GaN HEMTs.

The effects of device self-heating on the extraction of traps activation energy are investigated by means of experimental measurements and numerical simulations in the seventh paper, "Deep Levels Characterization in GaN HEMTs-Part II: Experimental and Numerical Evaluation of Self-Heating Effects on the Extraction of Traps Activation Energy" by Chini *et al.* from Universities of Padova and Modena & Reggio Emilia, Italy.

Then, the paper "Evaluation of Electron Trapping Speed of AlGaN/GaN HEMT with Real-Time Electro Luminescence and Pulsed I-V Measurements" by Wakejima *et al.* from Nagoya Institute of Technology, Japan, reports an experimental technique for the evaluation of electron trapping in AlGaN/GaN HEMT by means of a real-time electro luminescence and pulsed measurements.

In the ninth paper "Methodology for the Study of Dynamic ON-Resistance in GaN High-Voltage Field-Effect Transistors" by Jin *et al.* from MIT, a new methodology is developed for the investigation of the dynamic ON-resistance capable of spanning across 10 decades under a variety of bias conditions allowing a detailed characterization of charge trapping in power GaN HEMTs.

Finally, the charge trapping characteristics in dielectric-gated AlGaN/GaN HEMTs with atomic layer deposited HfO_2 is reported in the paper "Threshold Voltage Shift due to Charge Trapping in Dielectric-Gated AlGaN/GaN High Electron Mobility Transistors Examined in Au-Free Technology" by Johnson *et al.* from Texas A&M University, Texas State University and SEMATECH, Albany, USA. The paper also demonstrates and discusses the stability of the enhancement mode operation of HEMTs.

V. Simulation-Based Development of GaN HEMTs Devices

The first (invited) paper in this section "Theory of Carriers Transport in III-N Materials: State of the Art and Future Outlook" from Bellotti *et al*. from Boston University and Politecnico di Torino, Italy, describes the state of the art in the numerical simulation of the carrier transport properties of GaN and its ternary alloys, with a view to the application to a state of the art full-band Monte Carlo model including carrier-phonon interaction and a full quantum mechanical model for multiband transport, that is critical to modeling high-field transport.

The second paper "Robust Surface-Potential-Based Compact Model for GaN HEMT IC Design" by Khandelwal *et al*. from the Norwegian University of Science and Technology, the Indian Institute of Technology, Kanpur, IMS Bordeaux and IEMN, Lille, France, presents an accurate surface-potential-based compact model for the simulation of GaN HEMT based circuits; the presented model is robust according to benchmark tests like the DC and AC symmetry tests, reciprocity test and harmonic balance simulations test.

The third paper "Electric Field Distribution around Drain Side Gate Edge in AlGaN/GaN HEMTs: Analytical Approach" by Si *et al*. from the University of Electronic Science and Technology of China, proposes a conformal-mapping based analytical model for the surface electric field around the drain side gate edge in the AlGaN/GaN HEMT, to which the gate leakage, current collapse, etc. are highly related, and compare the model to numerical simulations.

The last paper "Design and Simulation of 5−20 kV GaN Enhancement-Mode Vertical Superjunction HEMT" Li *et al*. from Rensselaer Polytechnic, describes a systematic design process using numerical simulations of the novel GaN E-mode vertical superjunction HEMT with breakdown voltage in the range of 5−20 kV. The simulated on-state breakdown voltage of the GaN vertical superjunction HEMT shows 4.5% drop from the off-state breakdown voltage, and is only slightly higher than the 1.7% drop of the conventional GaN vertical HEMT.

VI. GaN-Based Low Noise Amplifiers and Gate Drive Circuits

Finally, two papers are devoted to low-noise and driver applications of GaN HEMTs. Although GaN devices are mainly intended as power (switching or RF) devices, they have a remarkable potential in other fields, paving the way, e.g., to robust multifunctional integrated circuits including RX and TX stages.

A first paper in this section "GaN-Based Robust Low-Noise Amplifiers" by Colangeli *et al*. from University of Rome Tor Vergata, Italy, reports an overview of GaN-based LNAs, highlighting their noise performance together with high linearity and robustness (over 40 dBm input power level without gain penalty).

The last paper "Capacitor-less Gate Drive Circuit Capable of High-Efficiency Operation for GaN FETs" by Hattori *et al*. from Shimane University, Matsue, Japan, proposes a capacitor-less gate drive circuit for power applications of GaN-based devices able to increase their efficiency. Drive loss analysis of an inverted gate drive circuit showing the lowest losses among capacitor-type gate drive circuits and a capacitor-less gate drive circuit was made to examine the differences between them; the results show that higher efficiency operation is obtained by applying a capacitor-less gate drive circuit to simple test circuits.

The six guest editors would like to sincerely thank the reviewers who carefully and meticulously reviewed each manuscript and the revised versions in a very timely manner. We would also like to thank the authors for their cooperation in submitting revised manuscripts in a shorter-than-normal time frame and in documenting important research results on GaN-based technology and devices, so that they are available to the wider research and user communities. We would also like to thank Jo Ann Marsh of the EDS publications office for the supporting work, that we greatly appreciated. Last but not least, a warm thanks goes to the ED Transactions EIC John Cressler for his continuous support and encouragement. We have greatly enjoyed putting together this Special Issue, and we hope that the readers will enjoy it as well.

Giovanni Ghione, *Guest Editor in Chief*
Politecnico di Torino, Italy
giovanni.ghione@polito.it

Kevin J. Chen, *Guest Editor*
Hong Kong University of Science and Technology, Hong Kong
eekjchen@ust.hk

Takashi Egawa, *Guest Editor*
Nagoya Institute of Technology, Nagoya, Japan
egawa.takashi@nitech.ac.jp

Gaudenzio Meneghesso, *Guest Editor*
University of Padova, Italy
gaudenzio.meneghesso@unipd.it

Tomas Palacios, *Guest Editor*
MIT, Boston, USA
tpalacios@MIT.EDU

Ruediger Quay, *Guest Editor*
Fraunhofer, IAF, Germany
ruediger.quay@iaf.fraunhofer.de

Giovanni Ghione (M'87–SM'94–F'07) received the Degree (*cum laude*) in electronic engineering with Politecnico di Torino, Torino, Italy, in 1981.

He has been an Assistant Professor of electromagnetic fields since 1983, Associate Professor of circuit theory with Politecnico di Milano, Milano, Italy, since 1987, and a Full Professor of electronics since 1990, first with University of Catania, Catania, Italy, and then with Politecnico di Torino. He has contributed to the numerical noise modeling in small- and large-signal regime, to the thermal modeling of devices and integrated circuits; to the modeling of passive elements, in particular of coplanar components. These activities were later extended to widegap semiconductors such as SiC and GaN and related alloys. He was actively engaged since 1985 in research on optoelectronic devices, with application to fast photodetector and to electrooptic and electroabsorption modulator modeling, but also to far infrared detectors on small-bandgap semiconductors and to organic solar cells. Since 2007, he has been the Head of the Department of Electronics and Telecommunications, Politecnico di Torino. He has authored or co-authored more than 300 research papers on the above subjects and five books. His current research interests include high-frequency electronics, with particular attention to the physics-based modeling of compound semiconductor materials and devices.

Prof. Ghione is reviewer for several international journals and member of the Editorial Board of the MTT Transactions. He has been a member of the QPC Subcommitee of IEDM from 1997 to 1998 and from 2006 to 2007 and a Chair in 2008. He was the EU Arrangement Chair of IEDM from 2009 to 2010. He has been a Chair of the ED Society Committee on Compound Semiconductor Devices and Circuits since 2010. Since September 2010, he has been an Associate Editor for Compound Semiconductors in IEEE TRANSACTIONS ON ELECTRON DEVICES. He has been a Chair of the GAAS2003 Conference and he has been a Subcommittee Chair in several SCs of the European Microwave Week.

Kevin Jing Chen (M'96–SM'06) received the B.S. degree from Peking University, Beijing, China, in 1988, and the Ph.D. degree from the University of Maryland, College Park, MD, USA, in 1993. His Ph.D. thesis was on the experimental realization and physics of resonant-tunneling transistors.

He is currently a Professor with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong. He was a Research Fellow with NTT LSI Laboratories, Japan, from 1994 to 1995, working on monolithic integration of resonant tunneling devices and III–V heterojunction FETs. From 1999 to 2000, he was a Technical Staff Member with the Wireless Semiconductor Division, Agilent Technologies, working on enhancement-mode P-HEMT technology for cellular handset applications. He has published more than 280 peer-reviewed papers. He has been granted five U.S. patents. His current research interests include fabrication technology and physics of wide-bandgap GaN devices for high-frequency, high-power and high-temperature applications.

Prof. Chen is a member of the Compound Semiconductor Device and IC Technology committee of the IEEE Electron Device Society and a Distinguished Lecturer of EDS. He has served as an Editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and the *Japanese Journal of Applied Physics*. He is currently an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES.

Takashi Egawa (M'12) received the B.E. and M.E. degrees in electronics and the D.E. degree in electrical and computer engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 1980, 1982, and 1991, respectively.

He was engaged in research on high-speed GaAs LSI, Oki Ltd., Tokyo, Japan, from 1982 to 1988. In 1991, he joined the Nagoya Institute of Technology as a Research Associate. He became an Associate Professor in 1993, a Professor with the Research Center for Micro-Structure Devices in 1999, and a Professor with the Research Center for Nano-Device and System in 2004, where he is currently a Professor and the Director. He has authored or co-authored more than 220 publications in international journals. His current research interests include heteroepitaxy of GaN and GaAs by MOCVD and its application to electronic and optical devices.

Prof. Egawa received the Kodaira Memorial Prize from IEE Japan in 1991 and from the Laser Society of Japan in 1996. He received awards from the Japanese Association for Crystal Growth, Minister of Education, Culture, Sports, Science and Technology in 2010, and Inoue Harushige Prize in 2013. He is a member of the Japan Society of Applied Physics, the IEE of Japan, and the IEEE EDS. He has been serving as an Editor of the IEEE ELECTRON DEVICE LETTERS for the compound semiconductor devices area since 2012.

Gaudenzio Meneghesso (S'95–M'97–SM'07–F'13) graduated in electronics engineering from the University of Padova, Padova, Italy, 1992, focused on the the failure mechanism induced by hot-electrons in MESFETs and HEMTs, and the Ph.D. degree in electrical and telecommunication engineering from the University of Padova, in 1997, focused on hot-electron characterization, effects and reliability of GaAs-based and InP-based HEMTs and pseudomorphic HEMTs.

He was with the University of Twente, Twente, The Netherland, in 1995, holding a human capital and mobility fellowship (within the SUSTAIN Network) on the dynamic behavior of protection structures against electrostatic discharge (ESD). Since 2011, he has been with the University of Padova as a Full Professor. He has published more than 500 technical papers and he has been invited to present his research activities in more than 60 international conferences. His current research interests include the electrical characterization, modeling and reliability of several semiconductors devices, including microwave and optoelectronics devices on III–V and III–N, RF-MEMS switches for reconfigurable antenna arrays, ESD protection structures for CMOS and smart power integrated circuits including electromagnetic interference issues, organic semiconductors devices, and photovoltaic solar cells based on various materials.

Prof. Meneghesso received the Italian Telecom Award for his thesis work in 1993. He is a reviewer of several international journals, including the IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE ELECTRON DEVICE LETTERS, *IEE Electronics Letters*, *Journal of Applied Physics*, *Applied Physics Letters*, and *Semiconductor Science and Technology*, *Microelectronics Reliability* (Elsevier). He has been a Guest Editor for the IEEE TED Special Issue on Light-Emitting Diodes in 2010 and the Microelectronics Reliability Special Issues in 2012 (papers presented at the 23rd European Symposium on the Reliability of Electron Devices, Failure Physics, and Analysis, ESREF in 2012). He has been serving for the IEEE International Reliability Physics (IRPS) Symposium since 2005, being TPC Chair of the Compound Semiconductor from 2008 to 2010, and he has been with the management committee since 2009. He served several years for the IEEE-International Electron Device Meeting. He was in the Quantum Electronics and Compound Semiconductors subcommittee as a member in 2003, as a Chair in 2004 and 2005, and he has been in the Executive Committee as an European Arrangements Chair in 2006 and 2007. He is on the Steering Committee of several European conferences: European Solid State Device Research Conference (ESSDERC) Heterostructures Technology Workshop (HETECH), Workshop on Compound Semiconductors Devices and Integrated Circuits (WOCSDICE). He was involved in the Technical Program Committee of several international conferences. He has been the General Chair of HETECH in 2001, WOCSDICE in 2007, HETECH in 2009, ESREF in 2012, WOCSEMMAD in 2013, and TWHM in 2013. In 2010, he entered in the IEEE EDS Adcom on different subcommittee. He was nominated to IEEE Fellow class in 2013, with the following citation: "for contributions to the reliability physics of compound semiconductors devices."

Tomas Palacios (S'02–M'06–SM'13) is the Emmanuel Landsman CD Associate Professor with the Department of Electrical Engineering and Computer Science, MIT, Cambridge, MA, USA. He has authored more than 200 contributions in international journals and conferences, 40 of them invited, three book chapters, and ten patents. His current research interests include the combination of new semiconductor materials and device concepts to advance the fields of information technology, biosensors, and energy conversion.

Prof. Palacios was the recipient of multiple awards, including the 2011 Presidential Early Career Award for Scientists and Engineers, the 2010 Young Investigator Award of the International Symposium on Compound Semiconductors, the 2009 National Science Foundation CAREER Award, the 2009 ONR Young Investigator Award, and the 2008 DARPA Young Faculty Award.

Rüdiger Quay (M'01–SM'10) received the Diploma degree in physics from Rheinisch-Westfälische Technische Hochschule (RWTH), Aachen, Germany, in 1997, a second Diploma in economics in 2003, the Doctoral (Hons.) degree in technical sciences from the Technische Universität Wien, Vienna, Austria, in 2001, and the Venia Legendi (Habilitation) degree in microelectronics from Technische Universität Wien in 2009.

He joined the Fraunhofer Institute of Applied Solid-State Physics, Freiburg, Germany, in 2001, as a Project Leader in the development of 100 Gbit/s ETDM circuits based on InP HBTs, later as a Group Leader of RF-devices and circuit characterisation group working on mm-wave RF-devices and high-power devices and ICs. Currently, he is the Deputy Head of the business field gallium nitride RF-power electronics with Fraunhofer. Since 2011, he has been a Lecturer with IMTEK, Albert-Ludwig University, Freiburg. He has authored or co-authored over 150 refereed publications and three monographs. He holds two patents.

Dr. Quay was a co-recipient of the Best Paper Awards of the European Microwave Integrated Circuit Conference in 2004, 2005, and 2006, and the European Microwave Prize in 2012. From 2003 to 2004, he was a member of the IEDM technical committee on compound semiconductors, which he chaired in 2005. Since 2009, he has been serving the TPRC of the MTT International Microwave Symposium and the TPC of the European Solid-State Circuits Conference. He is a Vice-Chairman of MTT-6, Microwave and Millimeter Wave Integrated Circuits, and he has been a member of the IEEE Electron Device Society Compound Semiconductor Subcommittee since 2012. Since 2011, he has been an Associate Editor of the *International Journal of Microwave and Wireless Technologies* and he has been an Associate Editor of the IEEE ELECTRON DEVICE LETTERS for compound semiconductors since 2012.