# GaN-Based Robust Low-Noise Amplifiers

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*Abstract***— In this paper, an overview of recently reported low-noise amplifiers (LNAs), designed, and fabricated in GaN technology is provided, highlighting their noise performance together with high-linearity and high-robustness capabilities. Several SELEX-ES GaN monolithic technologies are detailed, providing the results of the noise characterization and modeling on sample devices. An in-depth review of three LNAs based on the 0.25-***µ***m GaN HEMT process, marginally described in previous publications, is then presented. In particular, two robust and broadband 2–18-GHz monolithic microwave integrated circuit (MMIC) LNAs are designed, fabricated, and tested, exhibiting robustness to over 40-dBm input power levels; an X-band MMIC LNA, suitable for synthetic aperture radar systems, is also designed and realized, for which measurement results show a noise figure ∼2.2 dB with an associated gain >25 dB and robustness up to 41-dBm input power level.**

*Index Terms***— Broadband LNA, GaN MMIC, GaN technology, robust LNA, synthetic aperture radar (SAR), X-band LNA.**

## I. INTRODUCTION

**T**HE introduction of GaN HEMT devices, exhibiting high power densities associated to high breakdown voltages, and GaN monolithic technology, allowing for integrated circuit design, paved the way to compact, high-efficiency, high-power amplifiers (HPAs); since the late 90s several GaN-based power amplifiers have been developed, exploiting both hybrid and monolithic implementations and covering a wide range of applications from base stations for mobile communications to radar [1]. Although power amplification is the natural target for such devices, the power handling capability and the inherent linearity typical of GaN HEMTs can be exploited in other applications, such as transmit/receive  $(T/R)$  switches  $[2]$ – $[7]$  as an ultracompact alternative to ferrite circulators, duplexers [8], and broadband power combiners [9], [10].

Above all, GaN HEMTs and GaN monolithic technologies can represent a significant breakthrough in low-noise amplification; GaN-based low-noise amplifiers (LNAs) are one of the best candidates to realize receiving stages capable of surviving to extremely high input power levels without damage and without the need for protection by limiting circuits, that would lower the overall system noise figure. In addition, GaN HEMTs are superior to GaAs counterparts in terms of power handling and inherent linearity, allowing for the fabrication of

Manuscript received March 28, 2013; revised May 22, 2013; accepted May 23, 2013. Date of publication June 21, 2013; date of current version September 18, 2013. The review of this paper was arranged by Editor G. Ghione.

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Digital Object Identifier 10.1109/TED.2013.2265718

42  $-$  [25] (6.0 GHz)  $-$  [25] (14.0 GHz)  $-$  X-band LNA (9.6 GHz) Survivability [dBm] **for Survivability [dBm]** [28] (8.0 GHz) (<u>111</u> • • • • • • • • • • • • • • [27, 31] (4.5 GHz) 40  $[26]$   $(2.0 \text{ GHz})$  $[29]$   $(10.0$  GHz) 38 [23] (10.0 GHz) 36 ίð 34 [20] (9.6 GHz) Maximum P<sub>av</sub>  $[34] (10.0$  GHz) [22] (4.0 GHz) Maximum P 32 30 28  $[25]$   $(28.0 \text{ GHz})$ 0 5 10 15 20 25 30 35 Frequency [GHz]

Fig. 1. Results of robustness test for GaN LNAs.



Fig. 2. Cross-section SEM image of a device with  $L_G = 150$  nm and a Schottky FP metallization.

extremely linear LNAs. Finally, if GaN monolithic microwave integrated circuit (MMIC) LNAs are developed in the same technology of HPAs and T/R switches, a fully integrated T/R front end can be realized, providing low-noise and high-power amplification and operating-mode selection functionalities in a single, compact chip.

In this paper, an overview of recent contributions concerning GaN applied to low-noise amplification is provided in Section II. Subsequently, a number of GaN MMIC technologies supplied by SELEX-ES is presented in Section III,

together with the results of the characterization and modeling of representative devices. The above technologies are used to realize several robust LNAs for broadband and X-band applications. Design strategies and experimental validations of the three amplifiers are reported in Section IV, both in terms of small-signal and nonlinear performances. In particular, stresstest results on the X-band amplifier are here presented and discussed for the first time.

#### II. STATE-OF-THE-ART FOR GAN-BASED LNAS

In the last decade, a great effort has been spent by academic and industrial research to investigate the potential of GaNbased active devices to realize LNAs. The inherent highlinearity and power-handling capabilities of GaN HEMTs could represent a stunning advance toward the possibility of fabricating extremely robust and linear LNAs.

Several researches on GaN-based LNAs were reported in open literature, both in hybrid and monolithic technologies, showing that a high maturity level was reached for applications at least up to Ku-band. In particular, S-, C-, and X-bands are the most targeted frequency ranges because of their historical use for telecommunications, radar, and electronic warfare. As far as hybrid technology is concerned, operating frequencies are narrowed down to 3 GHz [11]–[13]. In [11], exploiting a GaN HEMT power bar, an extremely high output IP3 of 54 dBm at 2 GHz was demonstrated with 2 dB associated noise figure. Also in [12], the circuit was based on a GaN HEMT power bar, directly bonded into a hybrid microstrip circuit, and the LNA design was oriented toward obtaining an output IP3 over 49 dBm while achieving ∼ 15-dB gain and a noise figure not >2 dB at 1.8 GHz. The two-stage GaN HEMT hybrid LNA proposed in [13] was designed to operate up to 3 GHz and to achieve up to 42-dBm output IP3 together with over 12-dB gain and <1.6-dB noise figure.

Moving to monolithic technology, and focusing again on linearity as one of the main figures of merit for LNA design, [14] recorded over 51-dBm output IP3 and < 3-dB noise figure measured at 2 GHz for an MMIC cascode feedback LNA. Other interesting results were reported in [15], where two MMIC single-stage LNAs, operating at 7 GHz, are featured by over 43-dBm output IP3.

Nevertheless, the introduction of GaN-based LNAs is typically aimed at replacing the cascade of p-i-n diode limiter and GaAs LNA, which is commonly implemented to realize robust receivers to date, while assuring comparable noise performance. Table I summarizes some relevant recently reported results presenting GaN MMIC LNAs featuring low noise performance and operating up to 25 GHz [16]–[33]. In particular, several proposed GaN LNAs for X-band applications [15], [16], [26], [28], [29], [32], [33] exhibited similar maximum noise figures, aligned  $\sim$  2.5 dB, with the lower value of 2.0 dB reported in [15] for single-frequency operation. LNAs presented for C-band operation in [18] and [25] were featured by a noise figure <1.9 and 2.7 dB, respectively. Finally, in [25], one more LNA working at 14 GHz was detailed, showing a 1.9-dB noise figure.

Regarding broadband LNAs [17], [19]–[23], [27], [30], [31], the average maximum noise figure was 3.3 dB; in addition



Fig. 3. Minimum NF and associated available gain for single-gate (squares) and Schottky FP (triangles) devices with  $W_G = 4 \times 75 \mu m^2$  and  $L_G$  = 250 nm at 10 GHz.



Fig. 4. Microphotographs of three GaN/Si HEMTs.

to these realizations, [24] achieved a remarkably low 1-dB noise figure in 1–8-GHz bandwidth, although the single-stage amplifier is affected by over 12-dB gain roll-off.

A number of contributions actually provide results for specific tests on LNA robustness, to show the effectiveness of GaN technology for LNA survivability, avoiding the use of limiting circuitry. Such results are summarized in Fig. 1, where each LNA's operating bandwidth and the related test frequency for robustness are reported. As can be noticed, the maximum recorded input power level for amplifiers survivability was over 40 dBm [25]–[28], [31]. Notice that the dashed graph trace, related to the last two works [27], [31], represented the maximum power level in which the available instrumentation allowed to present to the DUTs; however, the LNAs did not report any damage after the stress test, hence a much higher maximum input power is expected, as discussed in Section IV. In [34], the test frequency for robustness was 10 GHz where the input reflection coefficient of the amplifier might be unmatched, as it was considerably outside the effective LNA operating bandwidth centered at 30 GHz. Nevertheless, it is noteworthy that such operating frequency was one of the highest reported to date for GaN LNAs; other remarkable demonstrations of GaN LNA effectiveness in the millimeterwave range can be found in [35] and [36], where LNAs were designed to operate at center frequencies of 44.5 and 76.5 GHz, exhibiting a 3.2- and 5-dB noise figure, respectively.

TABLE I NOISE PERFORMANCE OF RECENT WORKS ON GAN LNAS

Reference	Year	Frequency (GHz)	Maximum NF (dB)
$[15]$	2012	$\overline{7}$	2.0
$[33]$	2012	$7 - 12$	2.5
$[32]$	2012	8	2.0
$[30]$	2010	$1 - 25$	4.5
[28]	2009	$8 - 11$	2.5
$[25]$	2009	6 14	1.2 1.9
$[29]$	2009	$8 - 11$	2.3
[26]	2009	$8 - 11$	3.0
$[23]$	2007	$4 - 16$	2.7
$[24]$	2007	$1 - 8$	1.0
$[22]$	2007	$3 - 7$	2.3
$[21]$	2006	$1 - 10$	2.5
$[20]$	2005	$6 - 14$	2.0
[19]	2005	$2 - 12$	3.7
$[18]$	2005	6	2.7
$[17]$	2004	$5 - 18$	4.5
[16]	2004	$7 - 12$	3.0
X-band LNA	2012	$8.6 - 10.6$	2.3
$LNA$ 6-3-3[31]	2010	$2 - 18$	4.7
LNA 2-2-2 [27]	2009	$2 - 18$	5.7



Fig. 5. Minimum noise figure and noise resistance of three GaN/Si HEMTs.

Noise performances of most contributions in Table I are fully comparable with or better than commercial chipsets (p-i-n diode limiter plus GaAs LNA) currently available. As an example, one such chipset [37], produced by TriQuint [38] for applications in 4–20 GHz bandwidth, exhibited a noise figure of 3.5 dB, to which references in Table I involving similar frequency ranges [17], [20], [23], [27], [30], [31] compare well. On the other hand, GaN LNAs are typically featured by better characteristics in terms of maximum input power and linearity. The same TriQuint chipset exhibits a 36-dBm survival input power and a 18-dBm compression point, to be judged against over 40-dBm maximum input power and 20-dBm compression point of [27], [31]; the latter pair of amplifiers is also slightly better as far as gain is concerned (>20 dB versus 17 dB).



Fig. 6. Phases and magnitudes of the optimum noise match of three GaN/Si HEMTs.

# III. NOISE CHARACTERIZATION AND MODELING OF GAN HEMT DEVICES

Successful design of a low-noise stage involves the availability of accurate and consistent active device noise models. Such obvious consideration is particularly valid for GaN HEMT devices, given the relatively recent availability of uniform substrates and stabilized epitaxial growth techniques.

In this section, the noise characterization and modeling of several GaN-based technologies, provided by SELEX-ES, are presented. In particular, the performances of three technologies are described, differing in gate length (0.5 and 0.25  $\mu$ m) and substrate [silicon carbide (SiC) or silicon (Si)].

The characterization is performed by means of a custom, fully automated test bench, already described in [39], and able to implement the source-pull technique over 4–20-GHz bandwidth. The device characterization in terms of linear S-parameters is performed as a step of the noise measurement campaign. In addition, all small-signal and noise quantities of interest are measured on line by means of a complex RF switch matrix, avoiding manual connections or disconnections: only repeatable parts (i.e., RF paths including the switches) are precharacterized.

Details of the extraction algorithm and the assumed noise model can be found in [40]. In summary, the noise behavior of the active device as a linear two ports is described by the chain (ABCD) noise correlation matrix, whose terms are smooth functions of frequency and can therefore be represented as Taylor polynomials up to the maximum frequency of interest.

## *A. 0.5-*μ*m GaN/SiC HEMTs*

SELEX-ES  $0.5$ - $\mu$ m GaN/SiC microstrip technology, based on a  $70-\mu$ m substrate, is well established, and particularly suited for the fabrication of circuit components for high-power applications, including amplifiers and RF switches, at least up to X-band. It will be described in the following, representing the starting environment for two more advanced technologies, which will be detailed later.

Gate contacts are realized by optical stepper lithography in two steps, namely gate foot  $(L_{G, Foot})$  and gate head  $(L_{G, Head})$ .

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Fig. 7. Microphotograph of the 2−18-GHz distributed LNA in the 2-2-2 topology.



Fig. 8. Simulated (dashed lines) and measured (continuous lines) transducer gain and noise figures of the 2–18-GHz distributed LNA in the 2-2-2 topology.

The first one is obtained by an Ni/Pt metal evaporation, followed by a thermal treatment to recover the Schottky barrier characteristics after the inductive coupled plasma (ICP)  $F^+$  dry etch, which introduces a surface damage and a fluorine transient effect on device performance. The second step consists of an Au evaporation, to reduce the gate sheet resistance and to place, if needed, a field plate (FP) electrode.

Ohmic contacts are obtained by rapid thermal annealing on Ti/Al/Ni/Au metal stack, yielding an average contact resistance of  $R_{\rm C}$  = 0.43/0.5  $\Omega$ ·mm.

Front-side process is then completed by SiN layer gate passivation and electroplating to define interconnect metallization.

Fabrication process ends with backside wafer thinning to allow implementation of microstrip circuit topologies. ICP etch process, completed by a reactive-ion etching chlorine plasma is used to etch the final GaN buffer and thus to reach the front metal, from the via holes for the front-to-back interconnection. Finally, wafer process is completed with the backside metallization.



Fig. 9. Simulated (dashed lines) and measured (continuous lines) matchings of the 2-2-2 LNA at the input (squares) and output (triangles) section.

## *B. 0.25-*μ*m GaN/SiC HEMTs*

The  $0.5$ - $\mu$ m GaN/SiC technology naturally evolves through gate length downscaling to a quarter-micron and subquartermicron technologies, where the gate length  $L<sub>G</sub>$  can be set to 250, 150, or even reach 80 nm. To obtain such gate lengths, an electronic lithography is adopted instead of an optical one.

This technology is compatible with an innovative (patent pending) implementation of FP to mitigate short-channel effects. In particular, a Schottky plate is placed between the gate and drain electrodes (see Fig. 2), and biased at a zero or positive (1 V) voltage through a 1-k $\Omega$  resistor: further details can be found in [41] and [42].

Devices realized in GaN/SiC technologies are fully characterized and modeled for noise and small-signal performances.

As a result of the measurements campaign, Fig. 3 shows a comparison between a single gate and a Schottky FP HEMT concerning the minimum noise figure and the associated gain versus bias, with  $W_G = 4 \times 75 \text{--} \mu \text{m}^2$  periphery and  $L_G =$ 250-nm gate length at 10 GHz. A lower  $NF_{min}$  is achieved from single-gate devices with respect to the Schottky FP HEMTs (0.87 versus 1.5 dB at  $V_{DS} = 15$  V,  $I_D = 15\% I_{DSS}$ ), but with a lower associated gain (10.5 versus 13.5 dB at  $V_{DS} = 15$  V,  $I_D = 15\% I_{DSS}$ ; further, the measured differences tend to reduce at lower *V*<sub>DS</sub>. On the other hand, it must be considered that the inclusion of a Schottky FP provides an additional high input power robustness against high electric field and drain current overload at any *V*<sub>DS</sub> bias.

### *C. 0.5-*μ*m GaN/Si HEMTs*

The fabrication procedure optimized on the SiC-based technologies is applied to AlGaN/GaN heterojunctions on 4-in HR-Si (111) substrates, with a resistivity  $\rho = 7 \text{ k}\Omega \cdot \text{cm}$ ; targeted optimizations for the ohmic contact deposition and the backside process are introduced. The latter consists in lapping down to 50  $\mu$ m the Si substrate thickness by means of an abrasive 9- $\mu$ m alumina dust, followed by a polishing treatment to make easier the mask alignment for via holes lithography [43]. Such substrate thinning allows to reduce



Fig. 10. Measured nonlinear behavior of the distributed LNA in the 2-2-2 topology at 4 GHz.

Si contribution to device's thermal conductivities, resulting in a junction temperature under the gate contact, i.e., the hottest region,  $\langle 150 \degree C$ , if an operating temperature of 80  $\degree C$  is considered (a typical room temperature upper bound for many power applications) [44]. Because of the substrate thinning made necessary by power handling considerations, microstrip technology represents a better solution for power handling if compared with coplanar technology, as shown in [45]. For a discussion on the performance of passive components realized on such microstrip technology, refer to [46].

In addition, for such technology, an extensive RF characterization campaign is carried out on a representative set of HEMTs with different gate peripheries. Pulsed load-pull measurements show an output power density of 4 W/mm at 3 GHz with a pulsed drain bias of 25 V and drain current  $I_{DS} = 30\% I_{DSS}$ .

Scattering parameters are measured up to 40 GHz, at  $V_{DS}$  = 10 V,  $I_D = 20\% I_{DSS}$ . Measurements on a representative  $4 \times 75 \text{-} \mu \text{m}^2$  HEMT allow to compute a cut-off frequency >19 GHz and a maximum stable gain >17 dB at 3 GHz.

Noise characterization involves a set of four-finger devices, with finger lengths  $W_u$  equal to 25, 50, and 75  $\mu$ m (see Fig. 4), biased at  $V_{DS} = 10$  V,  $I_D = 20\% I_{DSS}$  (corresponding to 10.7, 21.3, and 32.0 mA, respectively).

The noise performances of the three devices, in terms of the four noise parameters, are reported in Figs. 5 and 6.

Although slightly worse, the resulting performance is similar to those of the GaN/SiC counterparts. Furthermore, the low-frequency behavior of all noise parameters as a function of device periphery agrees well with commonly observed noise scaling rules [47]. In particular, the increased slope in  $NF_{min}$ and the crushing of  $\Gamma_{opt}$  toward the real axis for increasing peripheries, as well as the inverse proportionality of  $R_n$  to gate width.

### IV. DESIGN AND VALIDATION OF ROBUST LNAS

In this section, the design of several GaN-based robust LNAs is presented; in particular, the  $0.25-\mu m$  technology described in Section III is adopted for all designs.



Fig. 11. Microphotograph of the 2–18-GHz distributed LNA.

Although high robustness is an inherent feature of wide bandgap semiconductors, it will be apparent that it can be further improved by specific architectural solutions: with reference to the latter aspect, two broadband LNAs exploiting a peculiar realization of distributed amplification are described in the following, which are able to withstand an input power >10 W [continuous wave (CW)].

A robust X-band LNA for synthetic aperture radar (SAR) systems is hence detailed, featured by 2.2-dB noise figure over the most part of X-band.

In addition, both semidistributed and single-ended LNAs take advantage of series resistors (10 k $\Omega$ ) along the gate paths, which are standard measures to increase ruggedness, as detailed in [22]. These resistors, providing a feedback voltage drop, oppose the rise of a forward gate current, which, according to [22], is the major degradation mechanism in GaN amplifiers. On the contrary, gate-source breakdown only occurs for very high input levels, whereas gate-drain breakdown, maximum drain current, and maximum dissipated power can be neglected for bias conditions here considered.

It is noteworthy that the analysis in [22] addressed degradation mechanisms in single-ended amplifiers, pointing out the strict correlation between LNA failure and dc component of gate current (because of self-bias), limited to the first stage. In particular, quite an abrupt drop of drain current and gain is the external indicator of this phenomenon, which precedes failure.

Therefore, gate currents of the X-band LNA are measured to precisely assess its robustness, as detailed in the following. Unfortunately, similar measurements are not straightforward for distributed amplifiers, as active devices cannot be accessed individually (of course each device's gate current may be approximated by half the total value for a two-FET cell). Nevertheless, distributed amplifiers are inherently more robust than single-ended ones, as, to a first-order approximation, all input power is delivered to the load resistor of the gate line: dc gate current is therefore the only concern for degradation, but it is limited by series resistors.



Fig. 12. Simulated (dashed lines) and measured (continuous lines) transducer gain of the 2–18 GHz distributed LNA in 6-3-3 topology.

Therefore, presented broadband amplifiers are expected to be at least more robust (in a worst-case scenario) than the X-band LNA: this is testified by measured  $P_{\text{av}}-P_{\text{out}}$  curves of the former, which do not show any sudden gain drop up to the maximum input power considered. The latter, on the other hand, shows as expected a simultaneous drop of gain and rise of dc gate current within the measurement range, further supporting the above considerations; in addition, unlike in [22], gate-source breakdown is believed to be reached in power stress measurements.

Performed stress tests allow to determine precise limitations of designed MMICs, as long as the previous mechanisms of failure are considered. On the other hand, a variety of other failure mechanisms, typically acting on the medium and long term, are evidenced for GaN technology [48], about which a complete understanding is not achieved yet.

Finally, no standard procedure is found in the literature for robustness tests; published results were quite nonuniform as to duty cycle and exposure time. In this case, a CW stress was following [22], where the most comprehensive analysis on survivability of GaN LNAs can be found (in addition, exposure time will be provided in the following to help performance comparisons in the future). In any case, CW measurements present inherent advantages: they are easy to take, implicitly contain duty cycle information, and prevent from overrating/misjudging the actual performance of a technology (as they represent a worst-case stress).

## *A. Broadband LNAs*

The design goal is to achieve a robust LNA operating in 2–18-GHz bandwidth, exhibiting noise and gain performance in line with the state-of-the-art and that could survive a CW input power in excess of 5 W.

To satisfy these requirements, a three-stage circuit configuration, with each stage consisting of a two-cell distributed amplifier (2-2-2 topology), is adopted [27]. This approach is quite unusual in a distributed LNA, where typically a large number of cells are considered for each traveling wave structure. Fig. 7 shows a microphotograph of the realized



Fig. 13. Simulated (dashed lines) and measured (continuous lines) matchings of the 6-3-3 LNA at the input (squares) and output (triangles) section.

LNA, whose size is  $3 \times 2.9$  mm<sup>2</sup>. Active devices have all the same  $4 \times 50$ - $\mu$ m<sup>2</sup> gate periphery.

The small-signal and noise performances of the MMIC are evaluated by means of on-wafer measurements and the results are shown in Fig. 8 and Fig. 9 together with simulated data. In particular, a gain slightly lower than expected—leading also to a higher noise figure–is obtained: the MMIC exhibits an average gain of 20 dB and a noise figure ∼ 5 dB. These differences are associated to a relatively low grade of technological maturity at the time of design and realization, which also lead, in conjunction with the high number of active devices per MMIC, to poor yield. Nevertheless, the maximum gain difference (3 dB) approximately corresponds, in average, to a 1-dB error on each two-FET cell's gain.

LNA robustness is evaluated with a Microwave Power Inc L0206-40 solid-state amplifier by exposing the MMIC, mounted in a connectorized test jig, to a swept CW RF power. The LNA input is driven with a power level up to 40 dBm for ∼ 5 min at *f* = 4 GHz. As shown in Fig. 10, *P*ldB is reached for an output power of 22 dBm (corresponding to 3-dBm input power). For higher input levels—up to 40 dBm—the LNA operates completely saturated, with an output power of  $\sim$  25 dBm.

To improve gain and noise performances, without sacrificing robustness, an optimized circuit configuration is devised. In particular, a smaller gate periphery is selected for the first distributed stage, together with a larger number of cells. As to the second and third stages, the number of cells are increased to flatten the gain response over frequency. A microphotograph of the fabricated LNA, with overall dimensions  $3.8 \times 2.9$  mm<sup>2</sup>, is shown in Fig. 11 [31].

This novel scheme (6-3-3 topology) is specifically developed to allow the fulfillment of the conflicting specifications of low noise, high gain, high maximum frequency, and robust operation. The device sizes are carefully selected to perform a noise/survivability tradeoff. A  $2 \times 50$ - $\mu$ m<sup>2</sup> gate periphery is selected for the six-cell input stage to provide adequate noise performance and a 4  $\times$  50- $\mu$ m<sup>2</sup> gate periphery is adopted for the subsequent three-cell stages to provide good RF survivability.



Fig. 14. Simulated (dashed line) and measured (continuous line) noise figures of the 2–18-GHz distributed LNA in the 6-3-3 topology.

A controlled impedance mismatch between the stages is allowed to redistribute gain among the stages in a way that the overall noise figure is lowered. In addition, drain line capacitive loading is adopted (mainly in the first stage) leading to a good synchronism between gate and drain line phase velocities.

Linear and nonlinear tests are performed following the same procedures as for the previous LNA. The measured gain, shown in Fig. 12, exhibits an average value of 23.3 dB with a ripple of  $\pm$  0.8 dB in the 1–20-GHz frequency range: such a flat gain response shows the effectiveness of the design approach. The measured input and output return losses of the amplifier, depicted in Fig. 13, are better than 8.5 dB in the operating bandwidth. A minimum noise figure of 3.3 dB results at 3 GHz, while the noise figure reaches 4.7 dB at 18 GHz, as shown in Fig. 14.

The  $P_{\text{av}}-P_{\text{out}}$  characteristic of this LNA is measured at  $f = 4.5$  GHz, where the input return loss is better than 15 dB. In this case, the realized LNA is driven with a CW input power up to 40 dBm for  $\sim$  5 min. As shown in Fig. 14, *P*<sub>ldB</sub> is reached for an output power of 22 dBm (corresponding to 1-dBm input power) while the typical third-order intercept is 29 dBm. For higher input levels, the output power saturates to 26 dBm.

It is noteworthy that both LNAs can withstand more than 10-W input drive with no signs of damage: indeed, the 40-dBm limitation is only due to the available instrumentation, not to experienced DUT failures. To the best of the authors' knowledge, such input power level is the highest reported of multioctave LNAs without performance degradation. Such remarkable result is the key feature of the presented LNAs as compared with their GaAs counterparts, which, typically requiring a p-i-n diode limiter as a protection, actually do not represent an effective solution in terms of achievable system noise figures.

# *B. X-Band LNA for SAR Applications*

The design goal is in this case to obtain a narrow-band LNA with performance appropriate to short- and mid-term evolution of X-band SAR systems, such as the Cosmo SkyMED system.



Fig. 15. Measured nonlinear behavior of the distributed LNA in 6-3-3 at 4.5 GHz.



Fig. 16. Microphotograph of the X-band LNA.

In particular, a noise figure  $<$ 2.5 dB is targeted as well as a linear gain >25 dB; more detailed specifications, as well as a general description of the first-run LNA, were reported in [49]. In the following, the results of the second-run LNA, shown in the microphotograph reported in Fig. 15, is presented.

Although the first-run LNA is designed following a specific approach for optimum noise performance [50], the secondrun realization is aimed at improving the overall performance based on test results. In particular, a fine tuning of the LNA output matching network is performed with the main goal of achieving a lower gain ripple over frequency. The second-run LNA shows a noise figure of  $\sim$  2.2 dB at the optimum drain voltage VDS  $= 10$  V, and a linear gain higher than 25 dB with an associated ripple of  $\pm$  0.5 dB, as shown in Figs. 17 and 18, respectively. MMIC size is  $3 \times 2.5$  mm<sup>2</sup>.

In this more recent MMIC, a final (RF) yield of 70% is achieved. In nominal voltage bias conditions (no current regulation), transducer gain of measured devices varies within  $a \pm 1.2$ -dB range, which is associated to a peak-to-peak noise figure variation of  $\sim$  0.25 dB.



Fig. 17. Measured noise figure of the X-band LNA.



Fig. 18. Measured input matching (squares), output matching (circles), and transducer gain (triangles) of the X-band LNA.

The LNA is designed including input and output bond wires (length 600  $\mu$ m and diameter 25  $\mu$ m), and therefore the actual noise figure is expected to be some tenths of dB less than measured on wafer and shown in Fig. 17. As to the transducer gain shown in Fig. 18, the effects of simulated bonding wires are added to the measured S-parameters.

In addition, the ruggedness of this LNA is investigated under input overdrive conditions. The applied test process consists in exposing biased MMICs to a calibrated CW input RF power at 9.6 GHz, with a duration of 1 s, and measuring postexposure performance (after the RF overdrive). Such measurement process is repeated increasing by 1 dB the input RF drive up to ∼ 43 dBm. Because of the limited dynamic range of the power sensor, the postexposure *P*out is not measured in linear region but for an available power of  $\sim$  13 dBm, corresponding to a compression level  $\sim$  17 dB.

Fig. 18 shows the output power under stress condition. A detail of the curve is in the top of Fig. 19, while in the bottom of the same figure the dc components of gate currents are reported; because of setup limitations, the gate currents of the second and third stages are measured together  $(I_{G,23})$ , while that of the first  $(I_{G,1})$  is measured separately.

Fig. 20 shows the poststress  $P_{\text{out}}$ , plus associated dc gate currents, for  $P_{\text{av}} = 13$  dBm, versus increasing stress power



Fig. 19. Measured nonlinear behavior of the X-band LNA.



Fig. 20. Detail of P*out* (top) and associated gate currents (bottom) of the X-band LNA, versus actual  $P_{ap}$ .  $I_G$ , 1 is marked by squares,  $I_G$ , 23 by circles.

levels, as described. LNA circuits show no poststress gain degradation with an input RF overdrive up to 41 dBm. After so high input power levels, also poststress gate currents show irreversible changes.

More insight on the dynamics taking place in this case, however, can be obtained by inspecting the strong correlation, well visible in Fig. 19, between gain drop and gate current rises, which was already observed in [22]; similarly, this phenomenon affects primarily the first stage, whereas the second and third stages show a remarkably lower total gate current. Unlike in [22], however, sudden kinks are observed both in the  $P_{\text{out}}$  curve and in gate currents, showing that gate-source breakdown is reached, although the MMIC can still recover for  $P_{\text{av}}$  values up to 41 dBm; while gate current issues mainly affect the first stage, gate-source breakdown is first reached by the subsequent stages.

In conclusion, also in this narrow-band LNA, a remarkable result in terms of power handling capability is achieved. In addition, these measurements confirm that the survivability of the broadband LNAs presented in Section IV-A may achieve higher values than the available instrumentation allowed to measure.



Fig. 21. Poststress P<sub>out</sub> (top) and gate currents (bottom) of the X-band LNA, versus stress Pav (actual Pav is 13 dBm). I*G*,1 is marked by squares, I*G* ,23 by circles.

## V. CONCLUSION

This contribution focused on GaN HEMT and GaN monolithic technology for the development of high-robustness and high-linearity LNAs, leading to the design and realization of GaN LNAs featured by performance suitable for several applications, such as communications, radar, and electronic warfare. In this framework, several GaN monolithic processes were developed, both on SiC and Si substrates, with HEMT gate scaling capabilities down to 80 nm, by SELEX-ES. Extensive characterization and modeling campaigns were carried out on each of these technologies, as mandatory steps for design and fabrication of GaN MMIC LNAs.

Finally, broadband and narrowband LNA designs and relevant test results were presented. In particular, two different 2–18-GHz robust LNAs were reported, showing survivability to over 40-dBm input power levels in CW mode; to the best of the authors' knowledge, this was the best result in the literature for multioctave MMIC LNAs. Further, a narrowband LNA with performance appropriate to short- and mid-term evolution of X-band SAR systems was demonstrated: <2.3 dB noise figure with an associated gain >25 dB were reported, together with a 41-dBm maximum input power level before device failure.

#### ACKNOWLEDGMENT

The authors would like to thank the support of SELEX-ES, represented by Dr. C. Lanzieri and Dr. A. Pantellini, and Prof. P. Colantonio of the University of Rome Tor Vergata, responsible for the Italian Space Agency project Tile II.

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