Dielectric Permittivity of Porous Si for Use as Substrate Material in Si-Integrated RF Devices

Panagiotis Sarafis, Emmanouel Hourdakis, and Androula G. Nassiopoulou

***Abstract*— Dielectric permittivity of porous Si (PSi) layers formed on a low-resistivity p-type Si (0.001–0.005 Ω.cm) is thoroughly investigated using analytical expressions within the frame of broadband transmission line characterization method in the frequency range 1–40 GHz. It is demonstrated that the value of Si resistivity is critical for the resulting PSi layer permittivity even within the above limited resistivity range. The real part of PSi dielectric permittivity changes monotonically between 1.8 and 4 by changing the Si resistivity between 0.001 and 0.005 Ω.cm. The above study was made for porosities between 70% and 84%. The quality factor and attenuation loss of the investigated coplanar waveguide transmission lines were found to be Q = 26 and a = 0.19 dB/mm, respectively, at 40 GHz. These values are competitive to those obtained on quartz, which is one of the off-chip RF substrates with the lowest losses. This confirms the superiority of the PSi material, mentioned above, for use as a local substrate for the on-chip RF device integration.**

***Index Terms*— Dielectric characterization, dielectric permittivity, porous silicon, RF devices, RF substrate materials.**

I. Introduction

ON-CHIP RF devices show many advantages compared with off-chip ones, including low cost, high density, small volume, and increased reliability. A limiting factor toward the on-chip integration of RF devices is the lossy Si substrate. High-resistivity Si and silicon-on-insulator (SOI) were demonstrated as low-loss substrates at RF [1]–[3], however, these substrates are not compatible with the standard CMOS technology that is implemented on low-resistivity Si. A material that can be locally formed on the low-resistivity Si wafer to provide the necessary electromagnetic (EM) shielding and reduce crosstalk via the substrate is of paramount importance toward the on-chip integration of RF devices. An excellent material for this application is porous Si (PSi) [4]–[13]. This material can be locally formed on the Si wafer [14] by electrochemical dissolution of bulk crystalline Si. Its properties depend strongly on the electrochemical conditions used for its formation and the Si substrate resistivity [15]. By choosing the appropriate conditions, high resistivity combined with low dielectric constant and low loss tangent can be obtained. In previous works, coplanar waveguide transmission lines (CPW TLines) were successfully integrated and measured on PSi layers formed on p-type [7], [16]–[17] and p^+-type Si substrates [8], [11]. A comparison between the transmission properties of CPW TLines on a local PSi substrate and state-of-the-art RF integration technologies was made in [11] and demonstrated the superiority of PSi for this application.

The material properties of PSi for its use as a low-loss RF substrate were investigated by a few groups. More specifically, characterization of the dielectric properties of PSi has been reported for frequencies ranging from direct current (DC) up to frequencies of a few hundreds of megahertz using capacitor and inductor structures integrated on PSi layers [9], [10], and [18]. DC conductivity measurements of PSi layers fabricated on p^+-Si substrates were reported in former works [19], [20]. Broadband transmission line measurements in the frequency range from DC to 20 GHz were also reported for PSi formed on both p- and p^+-type Si [5]–[8]. In [5] and [6], the relative dielectric constant and loss tangent of PSi of three different porosities in the range of 20%–80% on p^+-Si substrates were reported. These publications depict a decrease in both the relative dielectric constant and the loss tangent, with increasing porosity. However, the above study was limited to three samples and, to our knowledge, this result was not further verified by others.

In this paper, we report on the determination of the dielectric permittivity of PSi formed on a p^+-type Si substrate with resistivity in the range of 1–5 mΩ.cm, using the broadband transmission line method, as in [5]–[8]. The reason for choosing the above Si resistivity range is that the PSi layers formed on this type of substrate within this resistivity range show excellent mechanical stability [21] even at very high porosity, as well as excellent RF shielding properties, as demonstrated previously [8], [11]. Our results show that the relative permittivity of PSi depends on the resistivity of the Si wafer on which PSi is formed. At 40 GHz, it shows a linear increase with the increase of the Si wafer resistivity even in the small resistivity range used. This is attributed to differences in the porosity and the morphology of the fabricated PSi when the starting Si wafer resistivity changes. This result is important since it explains the dispersion of the S-parameters of CPW TLines from one sample to another in the above frequency range. By accurately choosing the Si wafer resistivity, reproducible results are obtained. Moreover, we investigated the dielectric properties of PSi as a function of porosity for three different porosities in the range between 70% and 84%, with the aim to extend previous studies by our

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TABLE I
SAMPLE SERIES 1: PSi LAYERS FROM DIFFERENT RESISTIVITY Si WAFERS

Sample Name	Si Wafer Resistivity (mΩ.cm)	Etch Rate (μm/min)	PSi Layer Thickness (μm)
PSi1	2.0 ± 0.1	0.700	140
PSi2	2.3 ± 0.1	0.695	139
PSi3	2.7 ± 0.1	0.806	145
PSi4	2.8 ± 0.1	0.750	135
PSi5	3.1 ± 0.1	0.746	150
PSi6	4.6 ± 0.1	0.852	155
PSi7	5.0 ± 0.1	0.933	168

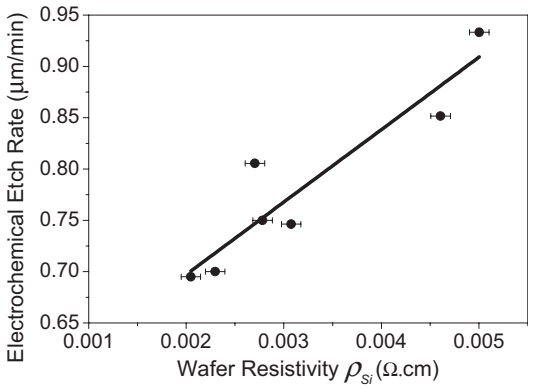

Fig. 1. Etch rate of seven PSi samples as a function of the initial Si wafer resistivity.

group related to the broadband characterization of 70% PSi layers [11]. Finally, in this paper, we demonstrate the state-of-the-art results of the attenuation constant and the quality factor of the CPW TLines integrated on the studied PSi layers.

II. MATERIAL AND DEVICE FABRICATION

A. Fabrication and Properties of the PSi Layers

PSi is fabricated on preselected areas on the Si wafer (maximum area used in this paper is 0.5 cm^2) by electrochemical etching of bulk crystalline Si in an HF:EtOH solution under constant current density. Depending on the Si wafer resistivity and the current density used, the material morphology differs. In general, PSi layers fabricated from low-resistivity (p^+-type) Si present a columnar porous morphology with vertical pores showing some branching along their length. For this substrate resistivity, uniform porosity is achieved in the whole layer thickness [22].

Two different experiments were carried out in this paper using two different series of samples with thick PSi layers on p^+-Si substrates. The first series of samples was dedicated to calibrating the etch rate and the resulting PSi layer thickness and to investigating the relative permittivity ($\varepsilon_{r,\mathrm{PSi}}$) of PSi as a function of the Si wafer resistivity (ρ_{Si}). The second series of samples was used to determine the PSi layer relative permittivity and loss tangent as a function of porosity, using the same value of ρ_{Si}.

The first series of PSi samples was fabricated using a 2HF(50%):3EtOH(99.9%) electrochemical solution, a current density of 20 mA/cm^2 and Si wafers with different resistivities in the range of 1–5 mΩ.cm, as depicted in Table I. For each sample the ρ_{Si} was measured using a four-point probe method on the specific area that would be anodized. The PSi layer thickness for each sample was measured by SEM. The etch rate was thus accurately determined. The objective was to correlate the resulting PSi layer thickness with the etching time and establish the corresponding calibration curve. It was found that the etch rate changes significantly with the Si resistivity even in the limited resistivity range used. This is due to differences in porosity correlated with the difference in resistivity [23]. The corresponding results are depicted in Table I and Fig. 1. For quite thick PSi layers, the etch rate difference introduces a large difference in the PSi layer thickness (several micrometers for the 150-μm-thick layers) for the same anodization conditions in wafers of different resistivities. In the following, we examine the variation of the PSi complex dielectric permittivity with the change of the initial Si wafer resistivity, taking into account the thickness difference. The corresponding results are presented in Section IV of this paper.

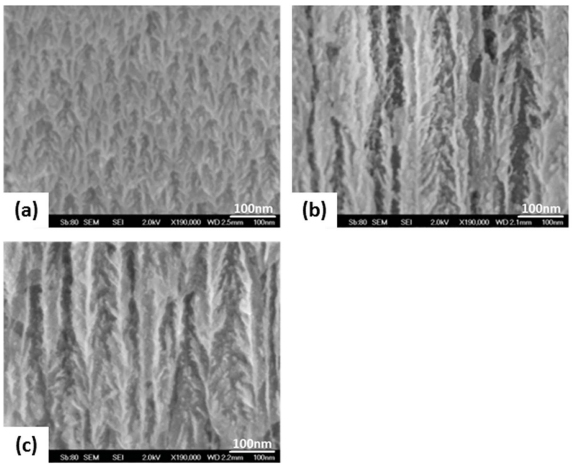

Fig. 2. Representative SEM micrographs of PSi layers fabricated at current densities (a) $J = 20$ mA/cm^2, porosity 70%. (b) $J = 40$ mA/cm^2, porosity 76%. (c) $J = 60$ mA/cm^2, porosity 84%.

The second series of samples was a set of three different samples with different porosities as in Table II and the same starting Si wafer resistivity (4.6 mΩ.cm). Their morphology was investigated by SEM, and representative images are depicted in Fig. 2. Pore size increases with porosity, while the nanostructured branching of the pores is smoothed out when porosity increases. The samples with higher porosity (76% and 84%) have larger pores with columnar morphology and relatively smooth pore walls compared with the lower porosity (70%) samples that show more pronounced dendrite nanostructured morphology (more randomly oriented pores).

The porosity of the layers was determined by using the three-weight measurement method by which the porosity P is calculated [12]

$$P = \frac{m_1 - m_2}{m_1 - m_3} \tag{1}$$

where m_1 is the initial mass of the sample, m_2 is the mass after anodization, and m_3 is the mass of the sample after removing the formed PSi layer. The corresponding error can be seen in Table II.

TABLE II
SAMPLE SERIES 2: SAMPLES WITH PSi LAYERS OF DIFFERENT POROSITIES

Sample Name	J (mA/cm^2)	Solution	P (%)	PSi Layer Thickness (μm)
PSi70	20	2HF:3EtOH	70 ± 5	155
PSi76	40	2HF:3EtOH	76 ± 3	138
PSi84	60	2HF:3EtOH	84 ± 3	145

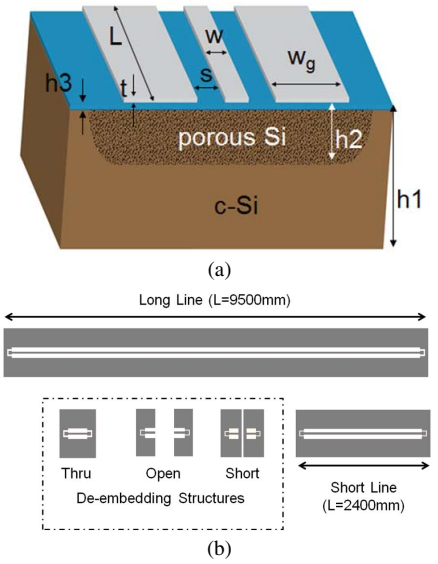

Fig. 3. (a) Schematic 3-D representation of a CPW TLine integrated on a local porous Si layer on the Si wafer and (b) its plane view representation together with corresponding de-embedding structures used in this paper. The different sizes depicted in the schematic are defined as follows: W = 20 μm is the TLine width, L the TLine length, s = 100 μm is the distance between the signal line and the ground line, Wg = 350 μm is the width of the ground plane, and t is the metal thickness. h_1 is the thickness (380 μm) of the wafer plus the SiO_2 layer (0.5 μm). h_2 is the thickness (variable, see Tables I and II for details) of the PSi layer plus the capping layer. h_3 is the thickness of the capping layer (0.5 m).

B. Fabrication of Test Devices (CPW TLines) for Measuring the Broadband Complex Permittivity of PSi

For the broadband dielectric characterization of the different PSi samples, we used the broadband transmission line method [7], [8], [24]. In this respect, CPW TLines of two different lengths along with a full set of de-embedding structures were fabricated on top of the corresponding PSi layers. The metallization used was 1-μm-thick Al, commonly used as an upper metal in various CMOS technology nodes. A schematic of the device and the de-embedding structures are given in Fig. 3.

III. DESCRIPTION OF THE METHOD USED FOR POROUS SILICON DIELECTRIC CHARACTERIZATION

Broadband transmission line measurements were used to characterize the PSi layer dielectric characteristics. In this respect, the S-parameters of a CPW on top of a PSi layer are measured, from which the effective permittivity and the propagation constant are extracted. Using the conformal mapping approach, the extracted parameters are then correlated to the substrate properties. More specifically, the complex permittivity and the conductivity of the PSi layer are calculated.

A. Measurements

For the broadband EM measurements of CPW TLines, a vector network analyzer (Anritsu-37269D), in the frequency range of 40 MHz–40 GHz, was used. For the on-wafer probing, a Cascade Microtech probe with 100-μm-pitch GSG microprobes was used. The load-reflect-reflect-match calibration method was followed, using an impedance standard substrate from Cascade Microtech. The S-parameters of the CPW TLines were recorded and analyzed. The de-embedding of the measurements was based on the two different length lines that were used to extract the propagation constant (γ), the relative permittivity (ε_{eff}), and the quality factor (Q) [25]. This method removes contact, pad, and pad-line transition parasitics, providing very accurate results for the above parameters. However, through this method, it is not possible to acquire the de-embedded S-parameters. For this reason, we used a three-step de-embedding method [26] (open-thru-short) to isolate the transmission line S-parameters.

B. CPW Propagation Parameters

The main parameters that describe the performance of a TLine are the effective permittivity, the total attenuation loss (a_T), and the quality factor. These parameters are widely used to compare the response of different CPW technologies and also as design parameters in order to integrate the model of a CPW line in the design flow of a complete RF circuit.

Total attenuation loss is the real part of the propagation constant and can be analyzed in conductor losses (a_C), substrate losses (a_S), and radiation losses [27], [28]. In the case of a lossy substrate, a_S can be further analyzed to dielectric polarization losses (a_D) and leakage losses (a_L). Due to the fact that radiation losses in a CPW can be neglected, we finally get

$$a_T = a_S + a_C = a_D + a_L + a_C. \tag{2}$$

The quality factor is calculated through

$$Q = \beta / 2a_T \tag{3}$$

where β is the phase constant.

C. Dielectric Properties of a Lossy Medium

In our analysis, we consider PSi as a lossy medium, characterized by its complex permittivity (ε_{PSi}) and its conductivity (σ_{PSi}). The complex permittivity can be written as

$$\varepsilon_{\text{PSi}} = \varepsilon_o \varepsilon_{r,\text{PSi}} = \varepsilon'_{\text{PSi}} - j\varepsilon''_{\text{PSi}} = \varepsilon_o \left(\varepsilon'_{r,\text{PSi}} - j\varepsilon''_{r,\text{PSi}}\right) \tag{4}$$

where ε_0 is the vacuum permittivity, $\varepsilon'_{\text{PSi}}$=$Re\{\varepsilon_{\text{PSi}}\}$, $\varepsilon''_{\text{PSi}} = \text{Im}\{\varepsilon_{\text{PSi}}\}$, $\varepsilon'_{r,\text{PSi}} = \text{Re}\{\varepsilon_{r,\text{PSi}}\}$, and $\varepsilon''_{r,\text{PSi}} = \text{Im}\{\varepsilon_{r,\text{PSi}}\}$. In a lossy dielectric medium, the dielectric loss tangent should incorporate both intrinsic polarization losses and leakage losses and can be written as [3]

$$\tan\delta_{\text{PSi}} = \frac{\omega \cdot \varepsilon''_{\text{PSi}} + \sigma_{\text{PSi}}}{\omega \cdot \varepsilon'_{\text{PSi}}} = \tan\delta_{D,\text{PSi}} + \tan\delta_{L,\text{PSi}} \tag{5}$$

where ω is the angular frequency, σ_{PSi} is the effective conductivity of PSi, $\tan\delta_{D,\mathrm{PSi}} = \omega\cdot\varepsilon''_{\mathrm{PSi}}/\omega\cdot\varepsilon'_{\mathrm{PSi}}$ stands for the intrinsic polarization losses of PSi, and $\tan\delta_{L,\mathrm{PSi}} = \sigma_{\mathrm{PSi}}/\omega\cdot\varepsilon'_{\mathrm{PSi}}$ stands for the leakage losses of PSi.

D. Conformal Mapping Approach for the CPW Analysis

The conformal mapping (CM) approach can provide closed-form formulas for calculating the effective permittivity ($\varepsilon_{\mathrm{eff}}$) of a CPW as a function of its physical characteristics and the electrical properties of the substrate stack on which the CPW is integrated. At this point, it has to be mentioned that the CM method is based on a quasistatic TEM approximation which is valid when the spacing between the two ground planes is smaller than the half-wavelength of the device [29], [30]. In our case, this means that we can use this approximation up to 400 GHz.

Using the CM method, we calculate the effective permittivity of the CPW on the three-layer stack (SiO_2/PSi/Si, see Fig. 3) as a function of the relative permittivity of SiO_2 ($\varepsilon_{r,\mathrm{cap}}\sim 3.9$), PSi ($\varepsilon_{r,\mathrm{PSi}}$), and Si ($\varepsilon_{r,Si}\sim 11.9$). For a finite-ground CPW on a three-layer dielectric stack, as in our case, the function is [28]

$$\varepsilon_{\mathrm{eff}} = 1+q_1(\varepsilon_{r,\mathrm{Si}}-1)+q_2(\varepsilon_{r,\mathrm{PSi}}-\varepsilon_{r,\mathrm{Si}})+q_2(\varepsilon_{r,\mathrm{cap}}-\varepsilon_{r,\mathrm{PSi}}) \quad (6)$$

where q_1, q_2, and q_3 are the filling factors that depend only on the geometrical parameters of the device [28] and are given by

$$q_j = \frac{1}{2}\frac{K(k_j)}{K(k'_j)}\frac{K(k'_0)}{K(k_0)}, \quad j=1,2,3. \quad (7)$$

In this equation, $K(k)$ describes the complete elliptic integral of k. Its arguments for a finite-ground CPW are calculated by

$$k_j = \frac{\sinh\left(\pi c/2h_j\right)}{\sinh\left(\pi b/2h_j\right)}\cdot\sqrt{\frac{\sinh^2\left(\pi b/2h_j\right)-\sinh^2\left(\pi a/2h_j\right)}{\sinh^2\left(\pi c/2h_j\right)-\sinh^2\left(\pi a/2h_j\right)}} \quad j=1,2,3 \quad (8)$$

$$k_0 = \frac{c}{b}\sqrt{\frac{b^2-a^2}{c^2-a^2}} \quad (9)$$

and

$$k'_j = \sqrt{1-k_j^2}, \quad j=0,1,2,3 \quad (10)$$

where $a = w/2$, $b = s + w/2$, and $c = w_g + s + w/2$. The variable h_j stands for the distance between the far end of the substrate layer and the metallization. In our case, h_1–h_3 is the Si wafer thickness, h_2–h_3 is the PSi thickness, and h_3 is the SiO_2 capping layer thickness.

The CM method also provides a correlation between the substrate attenuation loss (α_{sub}) and substrate loss tangent ($\tan\delta_{\mathrm{sub}}$). In the case of a one-layer substrate, this is written as [3], [31]

$$a_{\mathrm{sub}} = \frac{q\cdot\varepsilon'_{r,sub}\cdot f\cdot\pi\cdot\tan\delta_{\mathrm{sub}}}{c\cdot\sqrt{\varepsilon_{\mathrm{eff}}}} \quad (11)$$

where c is the speed of light in vacuum, $\varepsilon'_{r,\mathrm{sub}}$ is the substrate's real part of dielectric permittivity, and q is the filling factor.

In our case, for the three-layer substrate, we can assume that the total substrate losses are

$$a_S = a_{\mathrm{sub,\,Si}} + a_{\mathrm{sub,\,PSi}} + a_{\mathrm{sub,\,cap}} \quad (12)$$

where $a_{\mathrm{sub,\,Si}}$, $a_{\mathrm{sub,\,PSi}}$, and $a_{\mathrm{sub,\,cap}}$ are the substrate losses of Si, PSi, and the SiO_2 capping layer, respectively.

From (11) and (12), if we use the suitable filling factors, we derive the following expression for a_S:

$$a_S = \frac{\pi f}{c\cdot\sqrt{\varepsilon_{\mathrm{eff}}}}\cdot\begin{pmatrix}(q_1-q_2)\,\varepsilon'_{r,\mathrm{Si}}\cdot\tan\delta_{\mathrm{Si}}+\\ (q_2-q_3)\,\varepsilon'_{r,\mathrm{PSi}}\cdot\tan\delta_{\mathrm{PSi}}+\\ q_3\varepsilon'_{r,\mathrm{cap}}\cdot\tan\delta_{\mathrm{cap}}\end{pmatrix} \quad (13)$$

where $\tan\delta_{\mathrm{Si}}$ and $\tan\delta_{\mathrm{cap}}$ refer to the loss tangent of Si and SiO_2 capping layer, respectively.

E. Conformal Mapping Approach for CPW Analysis and Substrate Dielectric Parameter Extraction

As discussed in the literature [32], the previous method ignores metal losses and the skin effect that is quite important in low frequencies. An alternative approach is the two-measurement method, described in [32], in which an identical device on a known substrate is used as reference. In our case, we used an identical CPW TLine on quartz that has the same resistance and inductance as the CPW TLine on PSi and negligible substrate losses ($\tan\delta_{\mathrm{Quartz}}\sim 0.0001$). Equation (14) is then used, in which the left term is independent of the conductor losses, while the right one is determined using the CM approximation (6) of the three-layer stack for the CPW TLine on PSi and the one-layer substrate for the CPW TLine on quartz

$$\frac{\varepsilon_{\mathrm{eff,\,PSi}}-\varepsilon_{\mathrm{eff,\,Quartz}}}{\varepsilon_{\mathrm{eff,\,Quartz}}} = \frac{q_1\left(\varepsilon_{r,\mathrm{Si}}-\varepsilon_{r,\mathrm{Quartz}}\right)}{1+q_1\left(\varepsilon_{r,\mathrm{Quartz}}-1\right)} + \frac{q_2\left(\varepsilon_{r,\mathrm{PSi}}-\varepsilon_{r,\mathrm{Si}}\right)+q_3\left(\varepsilon_{r,\mathrm{cap}}-\varepsilon_{r,\mathrm{PSi}}\right)}{1+q_1\left(\varepsilon_{r,\mathrm{Quartz}}-1\right)} \quad (14)$$

where $\varepsilon_{r,\mathrm{Quartz}}$ and $\varepsilon_{\mathrm{eff,\,Quartz}}$ refer to the relative permittivity and the effective permittivity of the CPW on quartz, respectively.

Our assumption of negligible substrate losses on quartz leads to the following calculation of a_S:

$$a_S = a_{T,\,PSi} - a_{T,\,Quartz}. \quad (15)$$

Conclusively, we have shown that by solving (14) we can extract $\varepsilon'_{r\ \mathrm{PSi}}$ and $\varepsilon''_{r\ \mathrm{PSi}}$. Substituting (13), (15), and the extracted values of $\varepsilon'_{r\ \mathrm{PSi}}$ and $\varepsilon''_{r\ \mathrm{PSi}}$ in (5) we can finally extract the effective conductivity of PSi, that is, σ_{PSi}.

IV. Experimental Results and Porous Silicon Parameter Extraction

With the aim to determine the dielectric permittivity of PSi, we performed measurements of S-parameters of CPW TLines on PSi and we then used the above-described formalism to deduce the complex permittivity and effective conductivity of the PSi material from the measurements and analytical formulas. As mentioned before, we have used two series of

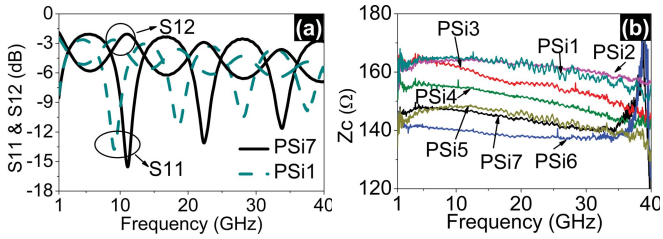

Fig. 4. (a) S_{11} and S_{12} parameters versus frequency for samples PSi1 ($\rho_{Si} = 0.002$ Ω.cm) and PSi7 ($\rho_{Si} = 0.005$ Ω.cm). (b) Characteristic impedance of the CPW TLines of samples PSi1 to PSi7 of series 1 versus frequency.

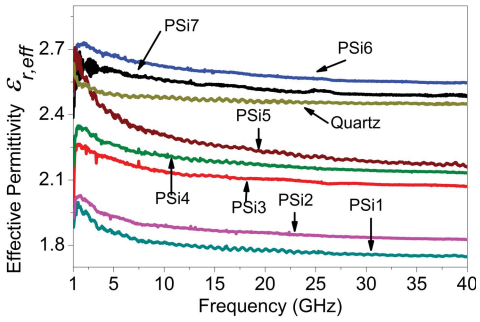

Fig. 5. Effective permittivity of the CPW TLines of samples PSi1 to PSi7 of series 1 as a function of frequency.

samples. In the first series, we used PSi layers from the anodization of Si wafers with different resistivities in the range 1–5 mΩ.cm, and in the second series, we changed the material porosity.

A. PSi Samples From Si Wafers With Different Resistivities

For this study, we used the first series of samples (see Table I), all anodized in the 2HF:3EtOH electrochemical solution with a current density $J = 20$ mA/cm^2. An example of S-parameters of CPW TLines on PSi is given in Fig. 4 for samples PSi1 and PSi7 with the maximum resistivity difference.

By design, the CPW TLines used have three or four resonances in the frequency range 1-40 GHz. The wide range of the oscillations in the S_{11} and S_{12} parameters is attributed to the fact that the characteristic impedance of the samples is around 145–150Ω, while our measurement system is at 50Ω. However, the corresponding accuracy remains <0.5 dB [33]. Resonance frequencies are shifted from one sample to another due to the different dielectric parameters of the two substrates.

The first step of our analysis, as described in Section III, starts with the extraction of ε_{eff}. Fig. 5 shows the effective permittivity of the CPW TLine used for the different PSi samples. For comparison, the effective permittivity of the same CPW TLine on quartz is also given. Advancing the analysis (see Section III-D), we extract $\varepsilon'_{r,\text{PSi}}$, $\tan\delta_{D,\text{PSi}}$, and σ_{PSi} as functions of frequency. These parameters are depicted in Figs. 6–8, respectively, for the different samples used.

From the above figures it can be seen that the parameters $\varepsilon'_{r,\text{PSi}}$ and $\tan\delta_{D,\text{PSi}}$ have a quite constant value above ~15 GHz, without significant frequency dispersion. The dispersion observed at lower frequencies (<15 GHz) can be attributed to small differences in the metallization layer thickness between the CPW TLine on PSi and the reference one that could affect the accurate removal of conductor losses in the two-measurement method. This is negligible at higher frequencies due to the skin effect.

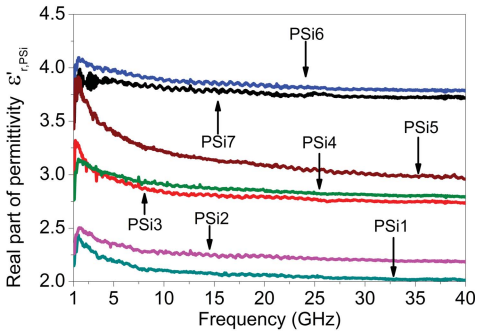

Fig. 6. Real part ($\varepsilon'_{r,\text{PSi}}$) of the dielectric permittivity of PSi as a function of frequency for samples PSi1 to PSi7.

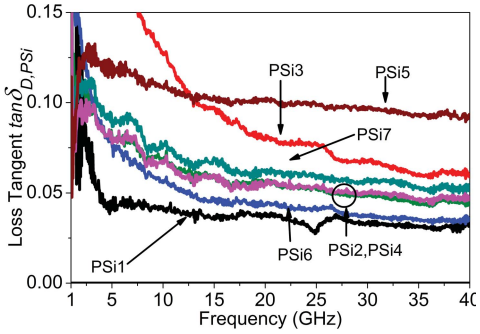

Fig. 7. PSi loss tangent ($\tan\delta_{D,\text{PSi}}$) due to intrinsic polarization in samples PSi1 to PSi7 as a function of frequency.

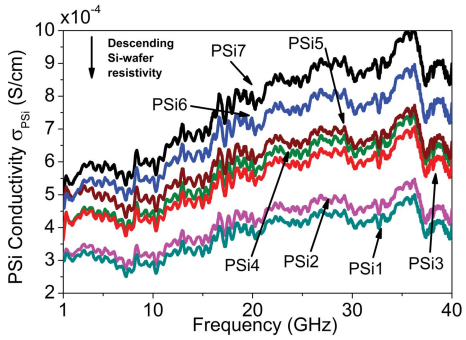

Fig. 8. PSi effective conductivity (σ_{PSi}) in samples PSi1 to PSi7 as a function of frequency.

Concerning PSi conductivity, we have to note that the obtained values reflect the effective conductivity of PSi, considered as an effective medium. Since the PSi material used in this paper shows an anisotropic morphology, conductivity is also anisotropic [19]. This explains the conductivity variation with frequency, since the penetration depth changes with frequency, thus changing the surface-to-depth ratio of the material involved in the EM interaction.

The differences that are observed between the samples are attributed to the different structures and morphologies of

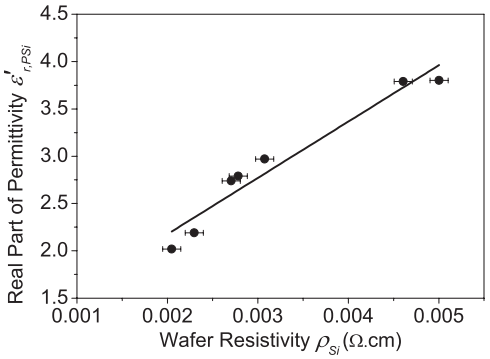

Fig. 9. Real part of the dielectric permittivity of PSi at 40 GHz as a function of the Si wafer resistivity. The almost linear relationship is useful for predicting $\varepsilon'_{r,\mathrm{PSi}}$.

PSi that result from the anodization of wafers with different resistivities. As it can be seen in Fig. 9, an almost linear relationship was obtained between the real part of dielectric permittivity ($\varepsilon'_{r,\mathrm{PSi}}$) and Si wafer resistivity (ρ_{Si}) for the resistivity range used. However, a more complicated relationship is expected in a larger resistivity range. Also, no simple function was found between the other PSi properties and ρ_{Si}. The increase of PSi permittivity with the increase of the starting wafer resistivity is attributed to the resulting lower porosity of the layer with the increasing Si resistivity [12].

The above results prove that there is an important influence of the Si wafer resistivity (that affects the PSi structure and morphology) on the PSi layer dielectric properties. Even the very small variations of ρ_{Si} within the range of 1–5 mΩ.cm resulted in significant differences in $\varepsilon'_{r,\mathrm{PSi}}$. For the design and fabrication of RF devices on a PSi layer, it is thus important to know exactly the wafer resistivity on which the PSi layers are formed. The exact knowledge of ρ_{Si} can improve the reproducibility of the characteristics of the RF devices integrated on the corresponding PSi layers. Dispersion in the literature of the characteristics of RF devices on PSi can be attributed to a difference in PSi morphology due to a different resistivity of the starting Si wafer.

B. Effect of Material Porosity on Dielectric Permittivity

In the second part of our study, we investigated the effect of material porosity on the characteristics of CPW TLines integrated on PSi. It has been reported [11] that by increasing the PSi layer porosity, the transmission characteristics of CPW TLines on top of it are improved. We investigated this effect for three different porosities, namely, 70%, 76%, and 84% porosity. These results are compared with those obtained from identical CPW TLines formed on bulk p-type Si (1–10Ω.cm) and on quartz. Fig. 10(a) shows a comparison of the total attenuation loss of CPW TLines on the three PSi samples, on bulk p-type Si, and on quartz. The quality factor of the CPW TLine on the five different substrates is shown in Fig. 10(b).

It is clearly depicted in Fig. 10(a) and (b) that the attenuation loss is largely reduced when using a PSi substrate compared with using bulk Si, approaching the attenuation achieved with the quartz substrate. Moreover, Q is also largely

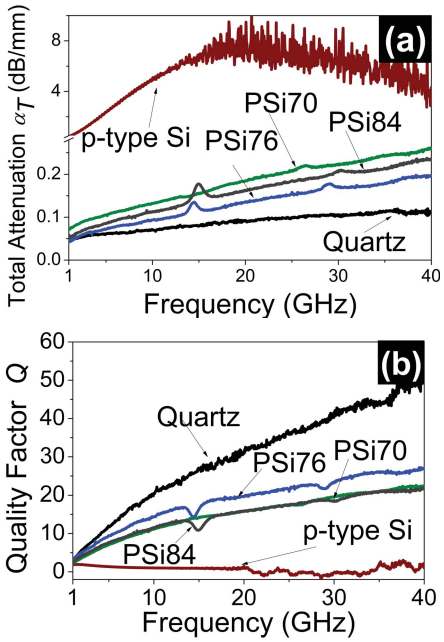

Fig. 10. (a) Total attenuation and (b) quality factor as a function of frequency of the CPW TLine integrated on the three different PSi samples PSi70, PSi76, and PSi85 and on low-resistivity p-type Si and quartz.

improved. However, a_T is not monotonically decreased with increasing P. Particularly, it can be seen that the CPW TLine on the PSi76 ($P = 76\%$) substrate bears better response in all the parameters compared with the two other PSi samples. The response is better than that previously reported by the authors in [9] (improvement is of the order of 12% in a and 10% in Q). Moreover, it can be clearly seen that PSi84 ($P = 84\%$) is worse than PSi76 ($P = 76\%$). This result is in contrast to previously reported results [4] claiming that the increase of porosity always leads to the lowering of dielectric loss. We attribute the above behavior to the different structure and morphology of the PSi layer at 84%, compared to the other two samples. One parameter that changes with increasing porosity is the increasing air:Si ratio, in favor of lower dielectric losses. However, another parameter is pore morphology. Less branched pores and increased structure anisotropy are observed in the 84% porosity sample, compared with the 70% porosity one. The 76% material combines the branch structure and high air:Si ratio. Especially, in the case of 70% porosity, it is clear that the pores are more randomly distributed than in the other samples. This random distribution reduces eddy currents in the substrate. The less branched structure of the 84% porosity layer leaves some electrical paths in eddy currents that reduce dielectric permittivity.

With further analysis of the above results we deduce the dielectric parameters of the different substrates that are depicted in Fig. 11. Analyzing Fig. 11(d) (PSi conductivity), it is depicted that PSi84 ($P = 84\%$) bears the lowest leakage losses. However, the polarization loss, which is described in Fig. 11(c), shows that there is more energy lost in PSi84 than in PSi76. This causes the total attenuation of PSi84 to be larger than the one of PSi76. The change in the material morphology, as mentioned before, can provide a possible explanation and

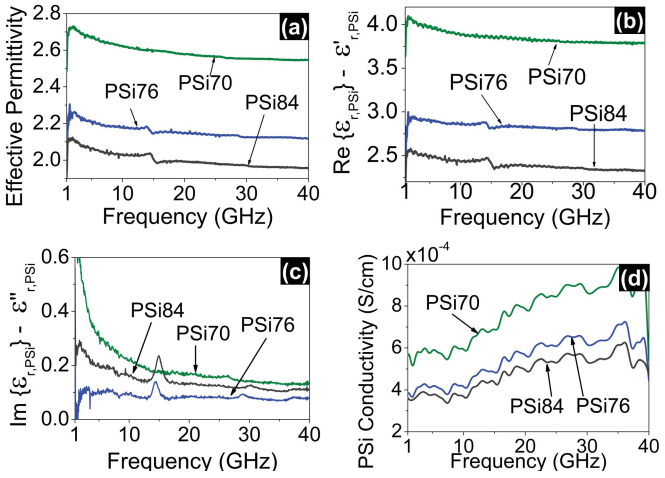

Fig. 11. Substrate and device parameters as a function of frequency, for PSi samples of three different porosities ($P = 70\%$, 76%, and 84%) (a) Effective permittivity of the CPW TLine. (b) Real part of the permittivity of PSi. (c) Imaginary part of the permittivity of PSi. (d) Effective conductivity of PSi.

TABLE III
PARAMETERS OF PSI70, PSI76, AND PSI84 AS EXTRACTED THROUGH THE CONFORMAL MAPPING METHOD

Sample Name	Porosity (%)	Conformal Mapping Method		
		$\varepsilon_{r,\mathrm{PSi}}$	$\tan\delta_{D,\mathrm{PSi}}$	σ_{PSi} ($\times 10^{-4}$ S/cm)
PSi70	70	3.79	0.035	8.8
PSi76	76	2.79	0.028	6.2
PSi84	84	2.33	0.047	5.3

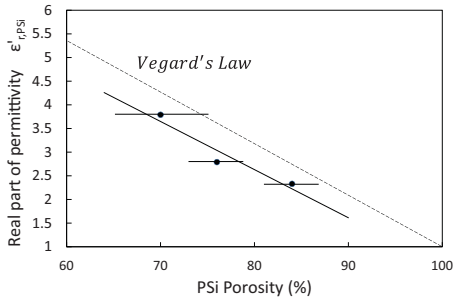

Fig. 12. Real part of dielectric permittivity ($\varepsilon'_{r,\mathrm{PSi}}$) of PSi as a function of porosity. For comparison, the dotted line derived from the simple effective medium approximation that correlates the permittivity to the porosity of PSi is also given. The full line is the best fit to the experimental results.

a hint for further analysis on how morphology affects the RF isolation properties of a PSi layer. For clarity reasons, in the rest of the paper, we will concentrate on the extracted values of $\varepsilon'_{r,\mathrm{PSi}}$, $\tan\delta_{D,\mathrm{PSi}}$, and σ_{PSi} at 40 GHz (see Table III).

Fig. 11(b) demonstrates the real part of the relative permittivity of PSi. It is obvious that higher porosity PSi has reduced $\varepsilon'_{r,\mathrm{PSi}}$. As it can be seen in Fig. 12, this trend is almost linear. Theoretically, the relationship between resistivity and porosity is estimated from Vegard's Law [6], given for PSi by

$$\varepsilon'_{r,\mathrm{PSi}} = (1 - P)\,\varepsilon'_{r,\mathrm{PSi}} + P \cdot \varepsilon'_{r,\mathrm{air}} \tag{16}$$

where P is the porosity. The deviation from this law has also been reported by others in the past [34]. We attribute this to the fact that the above relation considers a composite material composed of Si and air. However, in highly PSi, the remaining Si skeleton is a nanostructured material with different properties than Si (depleted from carriers [35] and having a different dielectric behavior). This explains to our opinion this discrepancy.

V. CONCLUSION

In this paper, we developed a formalism to determine the dielectric function of PSi using analytical formulas in combination with experimental CPW S-parameters. We applied this formalism to two series of experiments. In the first one, we determined the dielectric permittivity of PSi layers formed on Si wafers with different resistivities (ρ_{Si}) in the range of 1–5 mΩ.cm and found that both the etch rate and relative permittivity ($\varepsilon'_{r,\mathrm{PSi}}$) of PSi change with the starting Si wafer resistivity even in the limited resistivity range used. This is attributed to differences in PSi material structure and morphology. Thus, the exact knowledge of the Si wafer resistivity is important for the reproducibility of PSi dielectric properties. Furthermore, we extracted the dielectric parameters (relative permittivity, loss tangent, and effective conductivity) of PSi layers with different porosities in the range of 70%–84%. We have found that device properties do not improve monotonically with increasing porosity, but there is an optimum after which device properties are degraded. This is tentatively attributed not only to the porosity change but also to a change in the PSi material morphology.

REFERENCES

[1] D. Lederer and J. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Dev. Lett.*, vol. 26, no. 11, pp. 805–807, Nov. 2005.
[2] C. R. Neve and J.-P. Raskin, "RF harmonic distortion of CPW lines on HR-Si and trap-rich HR-Si substrates," *IEEE Trans. Electron Dev.*, vol. 59, no. 4, pp. 924–932, Apr. 2012.
[3] C.-Y. Hung and M.-H. Weng, "Investigation of the silicon substrate with different substrate resistivities for integrated filters with excellent performance," *IEEE Trans. Electron Dev.*, vol. 59, no. 4, pp. 1164–1171, Apr. 2012.
[4] K. Chong, Y.-H. Xie, K.-W. Yu, D. Huang, and M.-C. F. Chang, "High-performance inductors integrated on porous silicon," *IEEE Electron Dev. Lett.*, vol. 26, no. 2, pp. 93–95, Feb. 2005.
[5] H.-S. Kim, K. Chong, and Y.-H. Xie, "The promising role of porous Si in mixed-signal integrated circuit technology," *Phys. Stat. Sol. A*, vol. 197, no. 1, pp. 269–274, May 2003.
[6] H.-S. Kim, Y.-H. Xie, M. DeVincentis, T. Itoh, and K. A. Jenkins, "Unoxidized porous Si as an isolation material for mixed-signal integrated circuit applications," *J. Appl. Phys.*, vol. 93, no. 7, pp. 4226–4231, Apr. 2003.
[7] H. Contopanagos, F. Zacharatos, and A. G. Nassiopoulou, "RF characterization and isolation properties of mesoporous Si by on-chip coplanar waveguide measurements," *Solid State Electron.*, vol. 52, no. 11, pp. 1730–1734, Nov. 2008.
[8] F. Zacharatos, H. F. Contopanagos, and A. G. Nassiopoulou, "Optimized porous Si microplate technology for on-chip local RF isolation," *IEEE Trans. Electron Dev.*, vol. 56, no. 11, pp. 2733–2738, Nov. 2009.
[9] A. Porcher, B. Remaki, C. Populaire, and D. Barbier, "Nanostructured porous silicon as thick electrical insulator for radio-frequency applications," *Phys. Stat. Sol. A*, vol. 204, no. 6, pp. 1653–1657, Jun. 2007.
[10] A. Porcher, B. Remaki, C. Malhaire, and D. Barbier, "Low energy loss RF circuits on nanostructured porous silicon layers," *Phys. Stat. Sol. A*, vol. 205, no. 11, pp. 2552–2555, Nov. 2008.
[11] H. Issa, P. Ferrari, E. Hourdakis, and A. G. Nassiopoulou, "On-chip high-performance millimeter-wave transmission lines on locally grown porous silicon areas," *IEEE Trans. Electron Dev.*, vol. 58, no. 11, pp. 3720–3724, Nov. 2011.

[12] L. Canham, *Properties of Porous Silicon*. Chicago, IL, USA: INSPEC, 1997.
[13] M. Capelle, J. Billoue, P. Poveda, and G. Gautier, "N-type porous silicon substrates for integrated RF inductors," *IEEE Trans. Electron Dev.*, vol. 58, no. 11, pp. 4111–4114, Nov. 2011.
[14] G. Kaltsas and A. Nassiopoulou, "Frontside bulk silicon micromachining using porous-silicon technology," *Sens. Actuators A, Phys.*, vol. 65, pp. 175–179, Mar. 1998.
[15] P. Granitzer and K. Rumpf, "Porous silicon—a versatile host material," *Materials*, vol. 3, no. 2, pp. 943–998, Feb. 2010.
[16] D. Molinero, E. Valera, A. Lazaro, D. Girbau, A. Rodriguez, L. Pradell, and R. Alcubilla, "Properties of oxidized porous silicon as insulator material for RF applications," in *Proc. Spanish Conf. Electron Dev.*, Feb. 2005, pp. 131–133.
[17] C.-M. Nam and Y.-S. Kwon, "Coplanar waveguides on silicon substrate with thick oxidized porous silicon (OPS) layer," *IEEE Microw. Guid. Wave Lett.*, vol. 8, no. 11, pp. 369–371, Nov. 1998.
[18] M. Theodoropoulou, D. N. Pagonis, A. G. Nassiopoulou, C. A. Krontiras, and S. N. Georga, "Dielectric characterization of macroporous thick silicon films in the frequency range 1 Hz–1 MHz," *Phys. Stat. Sol. C*, vol. 5, no. 12, pp. 3597–3600, Dec. 2008.
[19] S. Borini, L. Boarino, and G. Amato, "Anisotropic resistivity of (100)-oriented mesoporous silicon," *Appl. Phys. Lett.*, vol. 89, no. 13, pp. 132111-1–132111-3, Sep. 2006.
[20] V. Timoshenko, T. Dittrich, V. Lysenko, M. Lisachenko, and F. Koch, "Free charge carriers in mesoporous silicon," *Phys. Rev. B*, vol. 64, no. 8, pp. 1–8, Aug. 2001.
[21] C. A. Charitidis, A. Skarmoutsou, A. G. Nassiopoulou, and A. Dragoneas, "Nanomechanical properties of thick porous silicon layers grown on p^- and p^+-type bulk crystalline Si," *Mater. Sci. Eng., A*, vol. 528, nos. 29–30, pp. 8715–8722, Nov. 2011.
[22] R. Herino, G. Bomchil, K. Barla, C. Bertrand, and J. L. Ginoux, "Porosity and pore size distributions of porous silicon layers," *J. Electrochem. Soc.*, vol. 134, no. 8, pp. 1994–2000, Aug. 1987.
[23] R. Herino, "Pore size distribution in porous silicon," in *Properties of Porous Silicon*, L. Canham, Ed. London, U.K.: INSPEC, 1997.
[24] L. F. Chen, C. K. Ong, C. P. Neo, V. V. Varadan, and V. K. Varadan, *Microwave Electronics: Measurement and Materials Characterization*. New York, USA: Wiley, 2004.
[25] A. M. Mangan, S. P. Voinigescu, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Dev.*, vol. 53, no. 2, pp. 235–241, Feb. 2006.
[26] H. Cho and D. E. Burk, "A three-step method for the de-embedding of high-frequency S-parameter measurements," *IEEE Trans. Electron Dev.*, vol. 38, no. 6, pp. 1371–1375, Jun. 1991.
[27] C. Schollhorn, W. Zhao, M. Morschbach, and E. Kasper, "Attenuation mechanisms of aluminum millimeter-wave coplanar waveguides on silicon," *IEEE Trans. Electron Dev.*, vol. 50, no. 3, pp. 740–746, Mar. 2003.
[28] R. N. Simons, *Coplanar Waveguide Circuits Components & Systems*, vol. 7. New York, USA: Wiley, 2001.
[29] E. Carlsson and S. Gevorgian, "Conformal mapping of the field and charge distributions in multilayered substrate CPWs," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1544–1552, Aug. 1999.
[30] G. L. Matthaei, K. Kiziloglu, N. Dagli, and S. I. Long, "The nature of the charges, currents, and fields in and about conductors having cross-sectional dimensions of the order of a skin depth," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 8, pp. 1031–1036, Aug. 1990.
[31] R. Collin, *Foundations for Microwave Engineering*, 2nd ed. New York, USA: Wiley, 2000.
[32] M. Ouaddari, S. Delprat, F. Vidal, M. Chaker, and K. Wu, "Microwave characterization of ferroelectric thin-film materials," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1390–1397, Apr. 2005.
[33] *Technical Datasheet & Configuration Guide*, Anritsu, Morgan Hill, CA, USA, 2007.
[34] S. Ramani, A. Cheville, J. Escorcia Garcia, and V. Agarwal, "Conductivity of free-standing porous silicon layers using Terahertz differential time-domain spectroscopy," *Phys. Stat. Sol. C*, vol. 4, no. 6, pp. 2111–2115, May 2007.
[35] V. Lehmann and U. Gosele, "Porous silicon formation: A quantum wire effect," *Appl. Phys. Lett.*, vol. 58, no. 8, pp. 856–858, Feb. 1991.

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