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Demonstration of >8-kV GaN HEMTs With CMOS-Compatible Manufacturing on 6-in Sapphire Substrates for Medium-Voltage Applications

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***Abstract*—Traditional GaN HEMTs on silicon suffer relatively low lateral and vertical blocking voltages and thick buffers, which impede their use in ≥1.2-kV applications. In this work, the prototypes of 8-kV GaN HEMTs on 6-in sapphire are successfully fabricated using CMOS-compatible processing. An etch-stop nitride layer AlN in the in situ SiN cap precisely defines the gate dielectric thickness. Au-free low-temperature ohmic contact and metal I are achieved by Ti/AlCu/Ti/TiN, and gate metal is achieved by TiN/Ti/AlCu/Ti/TiN, which significantly reduces the material cost. The high mechanical strength of sapphire results in low nonuniformity and well-controlled warpage, enabling the use of a 1.5-μm buffer. The fabricated HEMTs with an L_{GD} of 100 μm exhibit a low R_{ON} of 52 $\Omega\cdot$mm and a stable V_{TH} of −20 V. Benefiting from high-quality in situ SiN passivation, the dynamic R_{ON} and V_{TH} shift are maintained within 2.5% and 10%, respectively. The OFF-state breakdown voltage (BV) is increased beyond 8 kV using a simple device structure with only two field plates. The proposed low-cost and CMOS-compatible 8-kV GaN HEMTs fabricated on 6-in sapphire highlight an extremely simple epitaxy process, lateral device structure, and processing flow. Therefore, they offer great potential for serving future medium-voltage applications.**

***Index Terms*—6-in sapphire, 8 kV, GaN HEMTs, medium voltage.**

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I. Introduction

GAN HEMTs have achieved great success in commercial electronics [1], [2], [3], and their applications have focused mainly on mobile and laptop fast chargers [4], [5]. Since 2023, GaN HEMTs have also been adopted for other consumer applications, such as Class D-Audio devices, e-tools, and home appliances [6]. Interest in GaN for dc–dc converters and on-board chargers (OBCs) is growing, and vendors, such as Transphorm and Texas Instruments, have been qualified for electric vehicles use of such devices. Industrial applications are also expected to accelerate after 2024, as the price is expected to continue to fall. In fact, the medium-voltage power electronics market has an enormous demand for ≥1.2-kV power devices for data centers, electric vehicles, renewable energies, industrial automations, smart grids, and even rail traffic. However, emerging 1.2-kV GaN HEMTs have just been reported [7], [8], and 1.7-, 3.3-, 4.5-, and 6.5-kV products remain in development. In contrast, 1.7-kV SiC MOSFETs [9] have been widely commercialized, and 10-kV prototype SiC MOSFETs [10] have been demonstrated; 10-kV Ga_2O_3 charge-balance Schottky rectifiers have been realized by a reduced surface field (RESURF) structure based on p-type NiO [11].

To increase the GaN breakdown voltage (BV), GaN vertical devices, mainly including current aperture vertical electron transistors (CAVETs) [12], vertical GaN trench MOSFETs [13], [14], and GaN vertical FinFETs [15], have been widely explored. Regardless of the complex processing flow, the reliability issue persists in the threshold voltage V_{TH} shift of vertical GaN devices employing gate dielectrics, impeding their application potential [16]. To overcome this gate dielectric problem, Liu et al. [17] successfully fabricated a 1.2-kV-class, 4-A normally off vertical

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GaN fin-channel JFET on a GaN substrate with avalanche capability.

GaN superjunction MOSFETs/HEMTs have also been proposed for 5–20-kV utility applications, but related research has been conducted mainly by simulation [18]. Alternatively, polarization superjunction (PSJ) HEMTs were proposed to promote a BV greater than 3 kV by achieving charge balance by engineering the positive and negative polarization charges inherent in the GaN material [19]. A similar p-GaN RESURF structure was adopted to fabricate a 10-kV monolithic-cascode HEMT with an L_{GD} of 103 μm [20]. Furthermore, 10 400-V BV was obtained on HEMTs with an L_{GD} of 125 μm by means of a thick poly-AlN passivation layer [21]. Furthermore, pioneering multidimensional device architectures were proposed to balance V_{BD} and R_{ON} [22].

Overall, certain solutions are unsuitable for mass production because of requiring complex epitaxy and processing flows. Additionally, devices on large-scale wafers produced by CMOS-compatible processing have seldom been reported. The nonuniformity, reliability, and manufacturability also require detailed elaboration. GaN-on-sapphire is a feasible solution that has attracted great attention recently for $\geq$1200-V applications [7], [20]. Benefiting from the insulating substrate, the buffer vertical leakage path is cut off, and the lateral parasitic leakage channel at the substrate/(Al)GaN interface is also significantly suppressed [23], making GaN-on-sapphire suitable for higher blocking voltages. Although the thermal conductivity of sapphire is only a quarter that of silicon, the total thermal resistance of GaN-on-sapphire, which offers a higher mechanical strength than Si, can be limited by thinning of the sapphire substrate [24].

In this work, the epitaxy and fabrication of 8-kV HEMTs on 6-in sapphire substrates using CMOS-compatible processing are first introduced. Then, the wafer-level nonuniformity is inspected by recording the contactless sheet resistance $R_\square$, warpage testing, and mapping of the current and V_{TH}. Then, OFF-state blocking measurements are recorded on devices with various structures. Finally, dynamic performance is explored further.

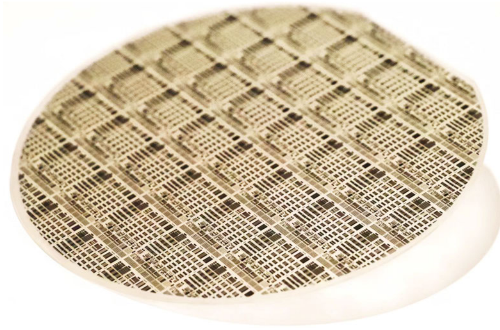

Fig. 1. Photograph of the fabricated 6-in GaN-on-sapphire wafer fabricated by CMOS-compatible processing.

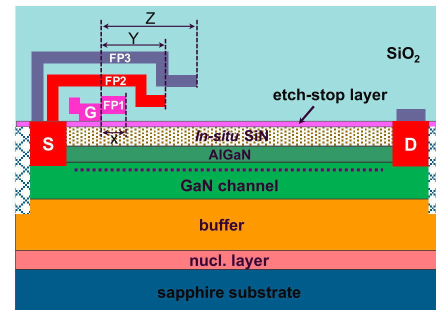

Fig. 2. Cross-sectional schematic of the fabricated GaN HEMTs on a 6-in sapphire.

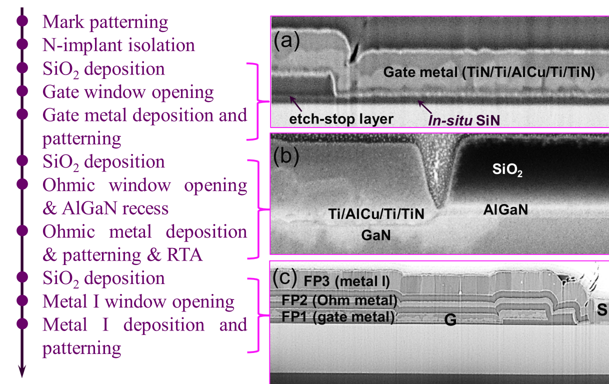

Fig. 3. Processing flow of the GaN HEMTs on 6-in sapphire, in which the SEM images show the areas of (a) gate, (b) low-temperature ohmic contact, and (c) field plates.

II. Epitaxy and Fabrication

The HEMT structure was epitaxially grown by a metal–organic chemical vapor deposition (MOCVD) system on 6-in sapphire substrates, as shown in Fig. 1. The epitaxy stack consists of a 1-mm sapphire substrate, a 35-nm AlGaN nucleation layer, a 1.5-μm GaN buffer layer, a 200-nm GaN channel layer, a 1-nm AlN spacer, a 20-nm $Al_{0.26}GaN$ barrier layer, a 50-nm in situ SiN passivation layer, and a 5-nm etch-stop poly-AlN layer, as depicted in Fig. 2. Notably, the 1.5-μm GaN buffer layer contains a 0.3-μm AlGaN transition layer and a 1.2-μm blocking layer to ensure high crystal quality.

As shown in Fig. 3, CMOS-compatible gate-first manufacturing was initiated by first patterning lithography marks and isolation. The device was isolated through multiple N ion implantation procedures [25].

Then, gate contact was achieved by 150-nm SiO_2 deposition via plasma-enhanced chemical vapor deposition (PECVD), gate window opening via reactive ion etching (RIE), gate metal deposition via physical vapor deposition (PVD), and gate metal patterning via chlorine-based inductively coupled plasma etching (ICP). As shown in Fig. 3(a), the gate metal stack comprises TiN/Ti/AlCu/Ti/TiN (40/20/250/5/30 nm), under which are the 2-nm etch-stop nitride layer and 50-nm in situ SiN dielectric. The etch-stop poly-AlN layer works to terminate RIE etching during gate window opening to guarantee the uniformity of the dielectric thickness and V_{TH} across the whole 6-in wafer. The etching selectivity between poly-AlN and the dielectric material reaches 15, and the etching gases are CF_4 and CHF_3 with flow rates of 10 and 30 sccm, respectively.

Next, a low-temperature Au-free ohmic contact was fabricated by 260-nm SiO_2 deposition, ohmic contact

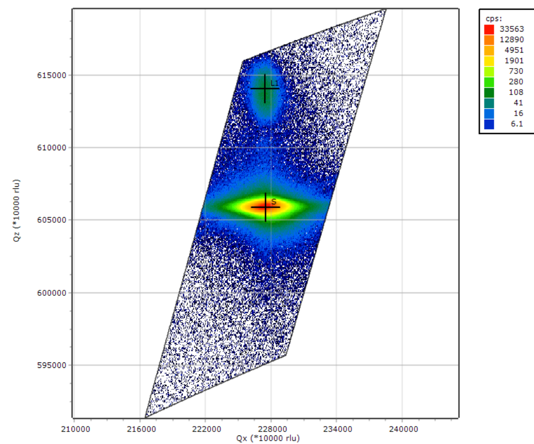

Fig. 4. Measured asymmetric RSM across the (105) plane of the $Al_{0.25}GaN$/GaN heterostructure on sapphire.

window opening, AlGaN recession by ICP, Ti/AlCu/Ti/TiN (5/100/20/60 nm) ohmic metal stack deposition, and rapid thermal annealing at 565 °C for 90 s in the ambient of N_2. The AlGaN recessing is conducted by etching through the AlGaN barrier layer to the GaN channel, with a recession thickness of 40 nm, as shown in Fig. 3(b), to eliminate the injected fluorine introduced by RIE etching [26].

Finally, metal I was processed by 300-nm SiO_2 deposition, Ti/AlCu/Ti/TiN (8/650/5/30 nm) metal stack deposition, and patterning by ICP etching. As shown in Fig. 3(c), metal I works as the 3rd field plate FP3.

The fabricated HEMTs have a gate width W_G of 100 μm, a gate length L_G of 6 μm, a gate–source distance L_{GS} of 1.5 μm, and various gate–drain distances L_{GD} from 22 to 100 μm. The dimensions of the field plates by gate metal, ohmic metal, and metal I are denoted as [X, Y, Z]. The electrical characterization was performed by using Keysight B1500A and B1505A.

III. Results and Discussion

Fig. 4 shows the reciprocal space mapping (RSM) of the $Al_{0.25}GaN$/GaN heterostructure on a 6-in sapphire wafer on which GaN and $Al_{0.25}GaN$ have been distinguished separately. The aligned x coordinate indicates that the $Al_{0.25}GaN$ barrier layer is fully strained. Moreover, the clear mapping image also corroborates the simple epitaxy structure in our work.

The fabricated 6-in wafer exhibited a well-controlled wafer-level nonuniformity of 2%, as verified by the mapping of the contactless sheet resistance $R_\square$ in Fig. 5(a). Moreover, Fig. 5(b) shows that the warpage of the 6-in GaN-on-sapphire wafer is only 16 μm due to the high mechanical strength of the sapphire substrate as well as the dedicated buffer design and processing flow.

Fig. 6(a) shows the output characteristics of the fabricated GaN HEMTs, for which R_{ON} reaches 52 $\Omega \cdot$mm due to the large L_{GD} of 100 μm. It is noticed that R_{ON} reaches 31.5 $\Omega \cdot$mm in [20] when using a complex five-channel wafer. Fig. 6(b) shows the transfer characteristics of 18 HEMTs across the wafer. The relatively tight distribution indicates the low nonuniformity of the epitaxy and the in situ SiN under

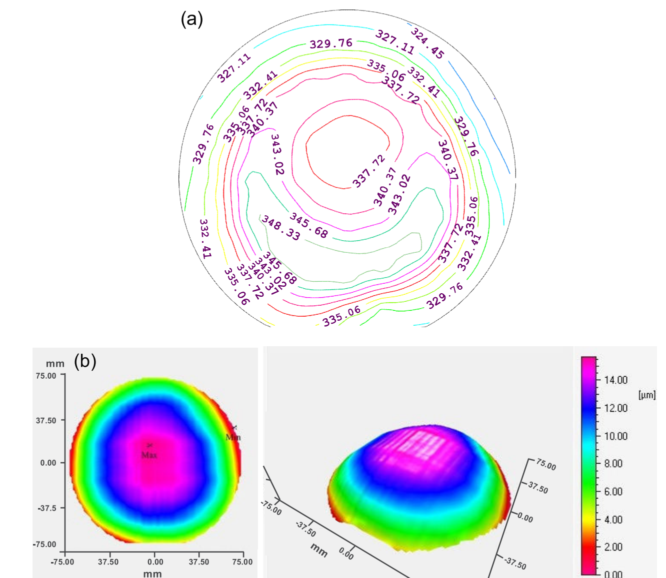

Fig. 5. (a) Mapping of the contactless sheet resistance $R_\square$ and (b) warpage of the fabricated 6-in GaN-on-sapphire wafer.

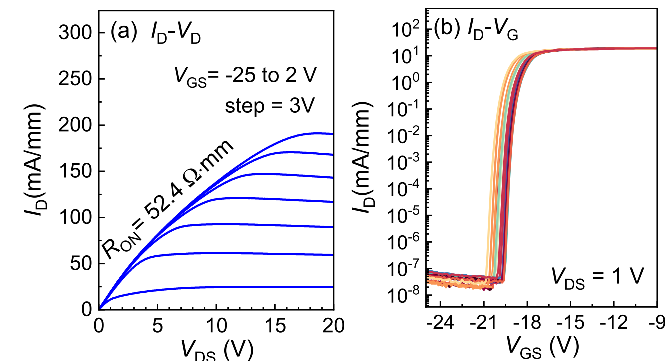

Fig. 6. (a) Output and (b) transfer characteristics of GaN HEMTs with an L_{GD} of 100 μm on 6-in GaN-on-sapphire.

the gate. The V_{TH} of -20 V is determined by the dielectric thickness, which can be easily tuned.

The electrical mapping of R_{ON} and V_{TH} was then conducted to verify the uniformity of the 6-in wafer. As shown in Fig. 7, the R_{ON} values are concentrated in the range of 48.5–56.0 $\Omega \cdot$mm, and the V_{TH} values are concentrated in the range from -21.5 to -18.0 V. The existing nonuniformity is attributed to variations in the SiN thickness and the low-temperature Au-free ohmic contact. Overall, the relatively high uniformity of the GaN-on-sapphire wafer ensures the high productivity of devices fabricated using this technique.

The devices with various structures were then subjected to OFF-state breakdown characterization. Fig. 8(a) and (b) demonstrates the OFF-state breakdown characteristics of the 3-FP and 2-FP HEMTs, respectively. As shown in Fig. 8(c), generally, 2-FP HEMTs with an extremely simplified structure feature a greater blocking capability, for which V_{BD} reaches 8 kV with an L_{GD} of 100 μm. Fig. 9 shows the simulated electric field contours of the 3-FP and 2-FP HEMTs. The electric field crowding effect takes place at the field plate edges. It is demonstrated in Fig. 9(c) that the peak electric field occurs

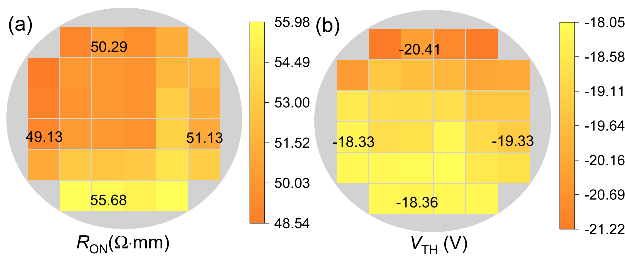

Fig. 7. Electrical mapping of (a) R_{ON} and (b) V_{TH} of the fabricated 6-in GaN-on-sapphire wafer.

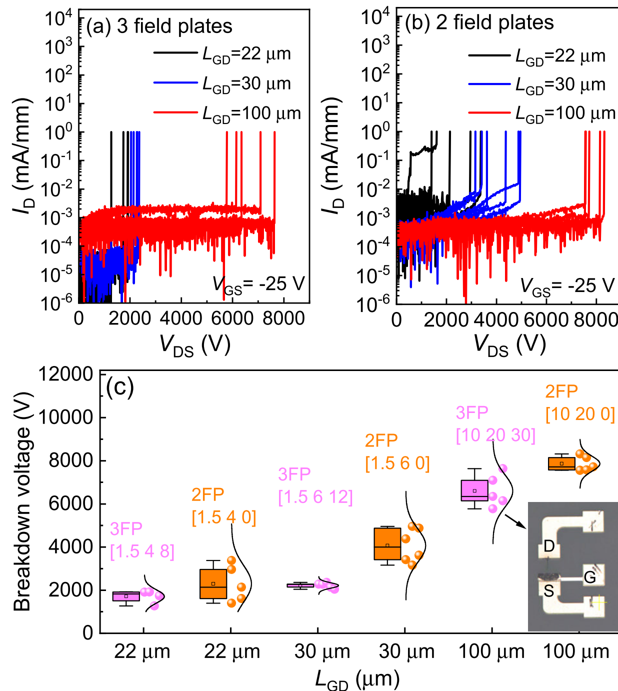

Fig. 8. (a) OFF-state breakdown characteristics of (a) 3-FP and (b) 2-FP HEMTs and (c) statistics of the OFF-state breakdown voltages of the HEMTs with various structures on the 6-in GaN-on-sapphire wafer. The inset of (c) shows a microscopy image of the 3-FP HEMTs with an L_{GD} of 100 μm after OFF-state breakdown.

at the gate field plate edge and the 3-FP HEMT inversely suffers a higher electric field under the same drain bias of 8 kV. This effect is attributed to the presence of field plates that extend outward to approach the drain terminal, which jeopardizes the effective L_{GD}. Therefore, breakdown occurs on the field plates rather than at the gate. This phenomenon has also been observed by Saito et al. [27], [28]. This indicates that for kV-HEMTs, the length of their field plates should be limited to avoid any early failure. If not so, the dielectric under field plates should be thick enough. This hypothesis is verified by the microscopy image of the failed 3-FP HEMTs in the inset of Fig. 8(c), where we can clearly see that failure occurs between the field plate and the drain terminal.

High-voltage OFF-state stress was subsequently applied on the HEMTs with an L_{GD} of 100 μm to probe the dynamic stability. During the measurements, the device was first stressed for 1 s in the OFF-state and then quickly subjected to I_D–V_D and I_D–V_G measurements. Fig. 10(a) shows that the current collapse worsens as the stress voltage increases but gradually saturates after 1500-V stress. Saturation can also be observed

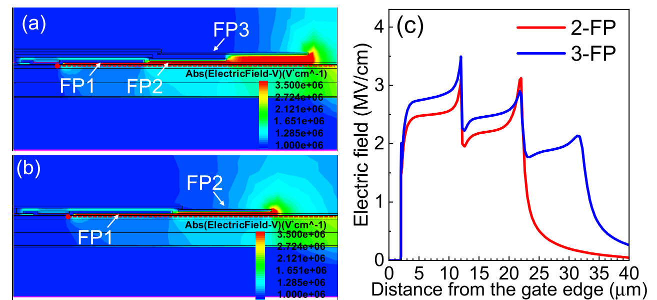

Fig. 9. Simulated electric field contours of (a) 3-FP HEMT and (b) 2-FP HEMT, and the electric field distribution of the two devices along the cutline in (a) and (b).

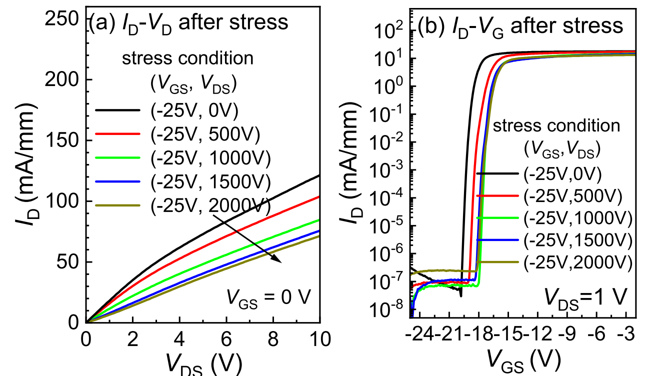

Fig. 10. (a) I_D–V_D and (b) I_D–V_G curves of the 2-FP GaN HEMTs on sapphire with an L_{GD} of 100 μm after various OFF-state stresses.

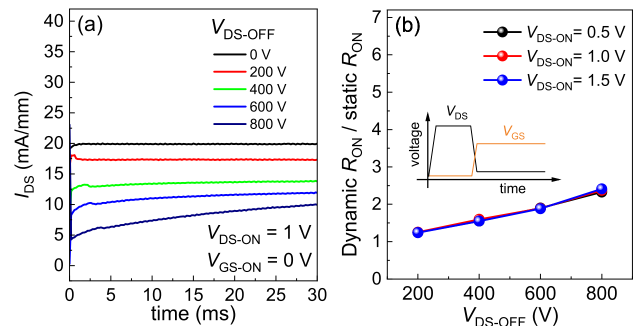

Fig. 11. (a) Transient current and (b) dynamic R_{ON} after high-voltage pulse stress by Keysight N1267A.

in Fig. 10(b), where the V_{TH} shift saturates after the 1000-V stress. The stabilities of the high-quality GaN epitaxy and the in situ SiN dielectric are thereby confirmed. Other passivation strategies, such as LPCVD SiN [29] and Al_2O_3/SiO_2 [30], are also widely adopted in commercial devices. Recently, Wu et al. [31], [32] presented a promising structure of actively passivated p-GaN gate HEMTs to further reduce the dynamic R_{ON}.

Dynamic R_{ON} of the HEMTs was then subjected to high-voltage pulse stress by Keysight N1267A. As shown in the inset of Fig. 11(b), this is actually a hard-switching setup that can strictly assess the dynamic performance, and the relaxation time between the stress and current recording is 200 μs. The dynamic R_{ON} is kept within 2.5 till 800-V stress.

IV. Conclusion

An 8-kV 6-in GaN-on-sapphire wafer, which has the potential to be a breakthrough solution for the medium-voltage

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power electronics market, was successfully demonstrated using our pilot line. The CMOS-compatible processing in this work verifies the feasibility of mass production of these wafers using the existing chip fabs. Moreover, the etch-stop nitride layer and in situ SiN dielectric guarantee high uniformity across the whole wafer. The remarkably simple epitaxy process and device structures, together with the use of large-scale and low-cost GaN-on-sapphire wafers, are potential to facilitate the realization of broader GaN applications in the market.

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