Microwave and Millimeter-Wave GaN HEMTs: Impact of Epitaxial Structure on Short-Channel Effects, Electron Trapping, and Reliability

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***Abstract*— Application of gallium nitride high-electron-mobility transistors (GaN HEMTs) to millimeter-wave power amplifiers requires gate length scaling below 150 nm: in order to control short-channel effects, the gate-to-channel distance must be decreased, and the device epitaxial structure has to be completely redesigned. A high 2-D electron gas (2DEG) carrier density can be preserved even with a very thin top barrier layer by substituting AlGaN with AlN, InAl(Ga)N, or ScAlN. Moreover, to prevent interaction of hot electrons with compensating impurities and defects in the doped GaN buffer, the latter has to be separated from the channel by a back barrier. Other device designs consist in adopting a graded channel (which controls the electric field) or to adopt nitrogen-polar (N-polar) GaN growth (which decreases the distance between gate and channel, thus attenuating short-channel effects). The aim of this article is to review the various options for controlling short-channel effects, improve off-state characteristics, and reduce drain–source leakage current. Advantages and potential drawbacks of each proposed solution are analyzed in terms of current collapse (CC), dispersion effects, and reliability.**

***Index Terms*— Deep levels, electron device failure physics, gallium nitride high-electron-mobility transistors (GaN HEMT), HEMT scaling, microwave transistors, millimeter wave, reliability, short-channel effects.**

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I. Introduction

GALLIUM nitride high-electron-mobility transistors (GaN HEMTs) offer a unique combination of high current and power density, high breakdown voltage, high cutoff frequency (f_T), maximum oscillation frequency (f_{max}), and efficiency [1], [2], [3], [4]. They represent the ideal choice for millimeter-wave power amplifiers offering the increased bandwidth needed for advanced radar and 5G and 6G telecommunication systems.

The improvement of the characteristics of these transistors has been obtained mainly by scaling gate lengths below 150 nm, at the same time keeping short-channel effects under control. The aim of this article is to review the various options for reducing short-channel effects in GaN HEMTs for microwave and millimeter-wave applications, and to analyze the advantages and potential drawbacks of each proposed solution in terms of current collapse (CC), dispersion effects, and reliability. In the following, the state-of-the-art of deep submicron GaN HEMTs with gate lengths of 150 nm and below will be briefly reviewed, followed by an analysis of short-channel effects in GaN HEMTs. The tradeoff between short-channel effects and frequency dispersion effects will be discussed by comparing test results obtained on devices having different epitaxial structures. The reader will find a summary of 2-D electron gas (2DEG) properties and electrical characteristics of tested devices at the end of the article. Conclusions follow.

II. State-of-the-Art of Microwave and Millimeter-Wave GaN HEMT

Micovic et al. [5] at HRL presented at IEDM three generations of scaled GaN HEMTs. The first had a T-shaped gate with a length of 40 nm, with gate-to-drain distance $L_{GD} = 1.1\ \mu$m, and achieved a cutoff frequency $f_T = 160$ GHz and a maximum oscillation frequency f_{max} equal to 380 GHz. The second generation of these devices had $L_G = 20$ nm and drain–source distance $L_{DS} = 100$ nm and reached

f_T/f_{max} = 450/440 GHz. Finally, the third generation adopted a 20-nm self-aligned gate, with asymmetric $L_{GS} \ll L_{GD}$, providing f_T/f_{max} = 320/580 GHz.

Before 2020, performances of W-band amplifiers adopting T-gate scaled gallium-polar (Ga-polar) AlGaN/GaN HEMTs were limited to 1–2 W (80–95 GHz), with approximately 20% power-added efficiency (PAE) [6], [7], [8], [9]; a 6-W 95-GHz power amplifier with 18% PAE was reported in 2020 [10]; device performance reached 3.6 W/mm and 13% PAE at 86 GHz [11] and 1.5 W/mm and 24% at 94 GHz [7], [9]. More recently, the application of polarization engineering in graded-channel (GC) GaN-based HEMT enabled researchers to obtain a better control of electric field and improved power scalability [12], [13], [14]. A reduced peak electric field in GC HEMTs results in higher saturation velocity and lower CC. Moon et al. [13], [15] at HRL presented a 60-nm gate GC AlGaN/GaN HEMTs having f_T = 156 GHz and f_{max} = 308 GHz. More recently. Moon et al. [16], the same group, demonstrated record 45% PAE and 2.1 W/mm at 94 GHz in GC 50-nm GaN HEMTs with a 12-nm AlGaN barrier, having 25% Al, yielding f_T and f_{max} of 170 and 347 GHz, respectively. A low 12% CC was measured at a stress of (−5 V, 15 V) on 50-nm gate devices.

Integrated circuits built at Fraunhofer IAF and based on 100-nm AlGaN/GaN HEMTs have reached operation circuit beyond 200 GHz (G-band) [17]. For a comparison of the state-of-the-art devices, see [18].

A possible alternative for GaN HEMT lateral and vertical scaling is represented by ultrathin (3–4 nm) AlN (or Al-rich) barrier layers: AlN/GaN HEMTs having L_G = 110 nm and L_{GD} =0.5 μm and adopting a C-doped buffer have achieved PAE > 70% and P_{OUT} = 5 W/mm in pulsed conditions, and PAE ≅ 60% and P_{OUT} = 4.3 W/mm in CW at 40 GHz. Drain-induced barrier lowering (DIBL) was as low as 14 mV/V for 3-nm AlN barrier [19]. Superior drain bias operation up to V_{DS} = 30 V, with 60% PAE and P_{OUT} as high as 7.1 W/mm during pulsed operation [20], can be obtained by carefully designing the thickness and composition of the AlGaN back barrier, as well as the thickness of the undoped GaN channel and the C concentration in the GaN buffer. In optimized transistors, short-channel effects were remarkably reduced. These devices also demonstrated excellent on-wafer short-term reliability [21]. AlN/GaN HEMTs having an AlN back barrier have been described in [22]. A record drain current value of 3.6 A/mm was demonstrated; at 10 GHz, P_{OUT} is 3W/mm and PAE = 22.7%. DIBL was as low as 17 mV/V, among the lowest reported DIBL for GaN HEMTs, indicative of the strong carrier confinement in the AlN/GaN/AlN heterostructure. A 20% CC was also measured under (−6- and 10-V stress of 50-nm gate devices.

Due to the absence of inversion symmetry in wurtzite III–nitride materials, the polarization of nitrogen-polar (N-polar) crystals is opposite to that of the Ga-polar (0001) crystals. Consequently, in N-polar GaN HEMTs, the 2DEG is induced above rather than below the wide bandgap (AlGaN) barrier layer [23]. This, as it will be discussed later, greatly helps in reducing short-channel effects and improving source and drain resistance. As a result, millimeter-wave N-polar HEMTs have demonstrated record values of power density and efficiency (8 W/mm at 10, 34, and 94 GHz, with PAE of 28.8% at 94 GHz) [24]. Recently, N-polar GaN-on-sapphire deep recess MIS-HEMTs have reached a high 8.8-dB linear gain in the W-band at 94 GHz at a 260-mA/mm current density bias point, enabling excellent output power density of 5.83 W/mm with record 38.5% PAE at 14 V [25]. At 12-V, those devices demonstrated an even higher PAE of 40.2%, with an associated 4.85 W/mm of output power density.

Most of the devices quoted above have been built on SiC substrates, which offer excellent thermal properties and compatibility with GaN. However, the use of Si substrates within a CMOS processing environment is appealing, especially for large-scale production, such as predicted for 5G and 6G systems [26]. A GaN-on-Si power amplifier, based on L_G = 150 nm AlGaN/GaN HEMT with f_{max} = 160 GHz, was presented in [27]. The amplifier exhibited an output power of 12 dBm with over 5-dB gain at 75–81 GHz. Tirelli et al. [28] at ETHZ presented data related to AlGaN/GaN HEMTs on Si substrates, with gate lengths of 75 and 100 nm. The devices featured peak cutoff frequencies f_T = 107 GHz and f_{max} = 150 GHz (with a simultaneous f_T = 90 GHz). A subsequent paper [29] described the large-signal operation of AlInN/GaN HEMTs at 94 GHz. Devices had gate length L_G = 50 nm and regrown ohmic contacts; they delivered a saturated output power density of 1.35 W/mm and a peak PAE of 12% (@ P_{out} = 1 W/mm).

A common method for evaluating the performance of microwave devices consists in calculating Johnson's figure of merit (J-FOM), given by J-FOM = $BV_{gd} \times f_T$, where BV_{gd} is the device OFF-state breakdown and f_T is the cutoff frequency. Medjdoub et al. [30] at IEMN reported a J-FOM of 7.5 THz × V in AlN/GaN/AlGaN double-heterostructure HEMTs on Si substrate.

A J-FOM of 8.32 THz × V was measured in L_G = 150 nm T-gate AlGaN/GaN HEMTs on Si, with f_T = 63 GHz and BV_{gd} = 132 V, DIBL lower than 30 mV/V, and CC less than 8% [31].

State-of-the-art results for GaN-on-Si microwave devices include 100-nm T-gate HEMTs with f_T = 105 GHz, providing 3.3 W/mm at 30 GHz, with a maximum stable gain of 13 dB [32]. Li et al. [33] at Cornell University developed double-heterostructure AlN/GaN/AlGaN HEMTs on Si, reaching f_T/f_{max} = 250/204 GHz for L_G = 55 nm and L_{SD} = 175 nm. InAlN/GaN HEMTs on Si have been developed by Elkashlan et al. [34] at IMEC; 100-nm gate devices have reached 2.8 W/mm at 28 GHz, with a PAE of 50% at V_{DS} = 10 V.

Integration of GaN HEMTs with Si CMOS opens the way to couple superior high-frequency power density and efficiency of GaN with circuit versatility of CMOS. Moreover, the replacement of SiC with Si substrates enables the adoption of larger substrates (up to 300 mm), compatible with CMOS processing tools, thus improving yield and reducing costs [35]. A 200-mm, fully CMOS-compatible InAlN/GaN-on-Si process, based on oxide–oxide bonding, has been described by

MIT researchers in [35]. Fabricated HEMTs have L_G = 120 nm and L_{GS} = 250 nm with f_T/f_{max} = 51/88 GHz; peak output power under continuous-wave conditions is shown to be 4.5 W/mm with a PAE of 53% at a frequency of 10 GHz.

Then et al. [36], [37], [38] at Intel have demonstrated the first 300-mm heterogeneous integration of Si CMOS transistors with depletion- and enhancement-mode high-k GaN MISHEMTs by means of 3-D layer transfer process integration. An outstanding performance has been obtained for integrated L_G = 50 nm transistors, e.g., 24-dBm output power (V_{DS} = 10 V) and 2.7 W/mm at 28 GHz, f_T/f_{max} = 300/400 GHz, DIBL of 190 mV/V, and SS = 108 mV/dec. More recently, f_{max} of 700 GHz (f_T = 115 GHz) has been achieved by L_G = 50 nm devices with source field plate (SFP) (L_{GD} = 600 nm and L_{SFP} = 100 nm) [38].

III. Short-Channel Effects in GaN HEMTs

In conventional Ga-polar AlGaN/GaN HEMTs, the increase of f_T and f_{max} has been achieved mainly by reducing the gate length and the source–drain distance; for a correct scaling, the thickness of the top barrier layer and the GaN channel has to be reduced in order to maintain aspect ratio and avoid short-channel effects [39]. On the other hand, thinning the wide bandgap barrier layer can have a detrimental effect on 2DEG concentration and, consequently, on current density.

One option consists in adopting a wider bandgap material for the top barrier layer, thus achieving a high 2DEG density even with a thin barrier thickness. To this aim, researchers have studied devices using thin AlN barriers [19], [20], [21], [40], InAl(Ga)N ternary and quaternary barriers [41], [42], [43], and ScAlN barriers [44], [45]; however, the study of the reliability of devices incorporating these new materials is still at its initial stage.

Control of short-channel effects and reduction of drain–source leakage current can be achieved by compensating GaN buffer conductivity using iron (Fe) [46], [47], [48], [49], [50] and/or carbon (C) [51], [52], [53], [54]. Iron (Fe) dopants, for instance, are generally adopted in RF transistors to obtain semi-insulating buffer layers to increase the blocking voltage [48]. In GaN, however, Fe enhances the occurrence of a defect related to a deep acceptor at 0.5–0.6 eV from the conduction band minimum (E_C) [50], [55], [56], [57], which represents a major cause for the CC in GaN HEMTs [57], [58], leading to a decreased output power and to a consequent reduction of PAE.

Compensation with carbon is a common solution to reduce buffer conductivity and increase breakdown voltage for power switching applications [47], [59], [60], [61]. It can provide sharper doping profiles and can be used in CMOS-compatible processes; C-doping also, however, increases CC and dynamic R_{ON} following OFF-state stress [61]. This degradation is usually attributed to deep acceptors (0.9 eV from the valence band), originated by defects consisting in the presence of carbon at nitrogen vacancies (C_N), within the C-doped buffer. Typical C concentration adopted for GaN buffer compensation in power GaN HEMTs is around 10^{19} cm^{-3}; however, the effective acceptor concentration is lower as C also introduces donor states with a density of at least 40% of the C_N one. For microwave devices, the peak Fe concentration is around 10^{18} cm^{-3}; Fe has a strong memory effect during growth, so there is always an exponentially decaying tail to the doping distribution [62].

Since C is unavoidably introduced during MOCVD growth, Fe-compensated microwave HEMTs contain an unknown concentration of electrically active C levels. Depending on dislocation density and C_N concentration and compensation, the trap charging and discharging can be dominated by the transport to and from the depletion layer rather than by the trap emission [28], [31], [62]. Hole bulk transport, as well as leakage along dislocations or interfaces, or 3-D hopping may be involved. This may give rise to additional time constants in drain current transients (DCTs) and may make the value of the apparent trap activation energy dependent on temperature and bias [58], [62].

Several research groups have tried to reduce the interaction between 2DEG electrons and deep levels in the C-doped GaN buffer by interposing an AlGaN barrier between the channel and the buffer [5], [54], [63], [64].

As described above, in Ga-polar devices adopting AlGaN top barriers, there is a tradeoff between 2DEG density and control of short-channel effects and dispersion effects. This tradeoff can be solved by a radical change in the epitaxy, i.e., by adopting N-polar epitaxial material for the fabrication of GaN HEMTs. In fact, N-polar GaN offers a much wider design space with respect to the Ga-polar counterpart. In N-polar devices [23], [24], [25], [65], [66], [67], [68], [69], [70], [71], [72], the AlGaN barrier layer is placed below the GaN channel layer and the 2DEG is formed between the gate contact and the (Al)GaN heterointerface. As a consequence, the distance between the 2DEG and the gate can be reduced without affecting AlGaN thickness and channel conductivity, thus achieving a better channel control and a higher transconductance. Control of electric field is easier in scaled N-polar devices and can even be improved by adopting a GaN cap layer, which, due to polarization, reduces the vertical electric field and enhances access regions conductivity; 2DEG charge density can then be maximized by properly designing the AlGaN layer, without affecting other device characteristics. Moreover, the AlGaN layer also represents a back barrier, further reducing short-channel effects and drain–source leakage. Finally, source and drain contacts are placed over the thin GaN channel layer, thus achieving low series and contact resistance; for highly scaled, self-aligned devices, regrown ohmic contacts are used. Recess gate can be implemented by inserting an AlGaN cap as etch-stop layer, in order to obtain low dispersion, high breakdown voltage, and low parasitic resistances. An MISHEMT structure, adopting SiN gate insulator, further improves gate leakage current and gain. As reported in the previous section, N-polar HEMTs provide a record value of efficiency and power density up to the W-band, at the cost of a complex epitaxial growth.

In the following, we present various options for controlling short-channel effects and analyze the advantages and potential drawbacks of each proposed solution in terms of CC, dispersion effect, and reliability.

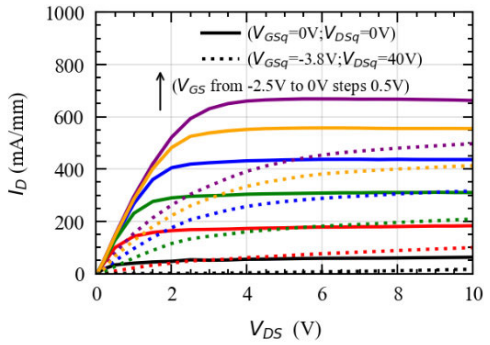

Fig. 1. Pulsed output characteristics of a 0.5-μm gate Fe-doped AlGaN/GaN HEMT from two different baselines: $V_{GSq} = V_{DSq} = 0$ V (solid), and $V_{GSq} = -3.8$ V and $V_{DSq} = 40$ V (dotted). The current dispersion observed is due to the response of iron-related trap located within the buffer. (© [2021] IEEE. Reprinted, with permission from [49]).

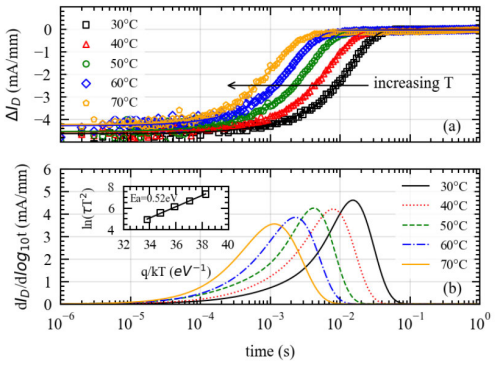

Fig. 2. (a) DCTs measured at different ambient temperatures (from 30 °C to 70 °C) in Fe-doped 0.5-μm gate AlGaN/GaN HEMTs. We represent the current variation (ΔI_D) with respect to the steady-state current value at the end of the transient ($I_{Dsteady}$). (b) $dI_D/dlog_{10}(t)$ used for drawing the Arrhenius plot (figure inset). The linear fit of the logarithmic form of the Arrhenius equation yields an activation energy $E_a = 0.52$ eV. (© [2021] IEEE, reprinted with permission from [15]).

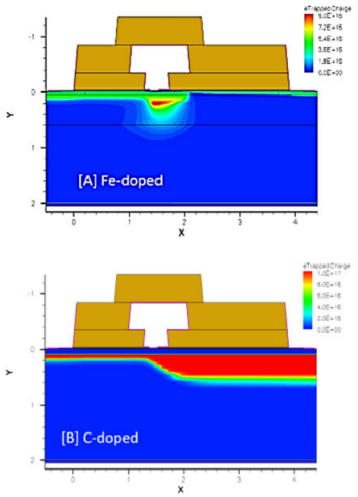

Fig. 3. Hydrodynamic device simulations of the contour plots of the negative charge build-up within the buffer layer of a 0.15-μm gate device with $L_{SD} = 4$ μm at $V_{DS} = 25$ V under OFF-state conditions. The GaN buffer is doped either with Fe or C. For Fe-doped buffer (top), the negative charge corresponds to trapped electrons, while for the C-doped one (bottom), the negative charge corresponds to negatively ionized acceptors due to the emission of holes. (© [2021] IEEE, reprinted with permission from [51]).

IV. Trap-Related Effects in Iron-Doped GaN HEMTs

Fe doping is added during the epitaxial growth of the GaN buffer in the RF transistor, under the undoped GaN channel, in order to increase the device blocking voltage in OFF-state. The deep levels correlated with Fe doping have been extensively studied [73]; Fe enhances the concentration of a defect introducing a deep acceptor at 0.5–0.6 eV from the conduction band of GaN. As a result, Fe represents a major cause of CC in microwave devices, and the Fe doping profile needs to be optimized in order to achieve simultaneously good pinchoff characteristics and reduced dispersion effects [74], [75].

We tested 0.5-μm gate AlGaN/GaN devices [49] grown on SiC with a 20-nm-thick $Al_{0.22}Ga_{0.78}N$ barrier over a 2-μm-thick Fe-doped GaN buffer. Gate–source distance, L_{GS}, and gate–drain distance, L_{GD}, were 1 and 2.5 μm, respectively. Fe concentration in the GaN buffer was constant at 1×10^{18} cm^{-3} starting from the SiC substrate interface until a distance of 0.6 μm from the AlGaN/GaN interface, where the iron concentration starts to decay with a slope of one decade every 0.4 μm; as a matter of fact, sharp Fe doping profiles are difficult to achieve.

Fig. 1 shows the typical 1-/100-μs pulsed I–V characteristics obtained with two different quiescent baselines, i.e., $V_{GSq} = V_{DSq} = 0$ V (solid), and $V_{GSq} = -3.8$ V and $V_{DSq} = 40$ V (dotted). The corresponding DCT has been measured according to the technique described in [49], see Fig. 2, and fitted by a multistretched exponential function. The Arrhenius plot of the associated time constants at different temperatures (T) yielded a 0.52-eV activation energy and a 5×10^{-16} cm^{-2} cross section, consistent with the values reported in the literature and associated with Fe traps (see [49]). Specific features of Fe-related deep levels are: 1) capture time is fast and transients are observed even for 1-μs trap-filling pulse, as in the case of Fig. 2; 2) electron trapping mostly occurs under the gate or at the gate edge toward the drain, thus affecting mostly V_{TH}, with reduced effect on drain resistance, see Fig. 3 (top); and 3) the detrapping time constant τ and its dependence on T are very reproducible and are not remarkably affected by the electric field (e.g., via the Poole–Frenkel effect). As a consequence, the measurement of τ can be used to evaluate the device junction temperature [76].

V. Deep Levels Related to Carbon Doping, Transient and Memory Effects, and Reliability

Due to its compatibility with CMOS fabrication processes, carbon is generally adopted for the compensation of the GaN buffer in GaN HEMTs grown on Si substrates for power switching applications. Carbon enables better control of doping profile and a higher level of doping concentration, so it is under study also for improving breakdown and reducing short-channel effects in microwave devices. Theoretical analysis [77] suggests that substitutional C in GaN originates two levels, an acceptor state due to C at nitrogen site C_N,

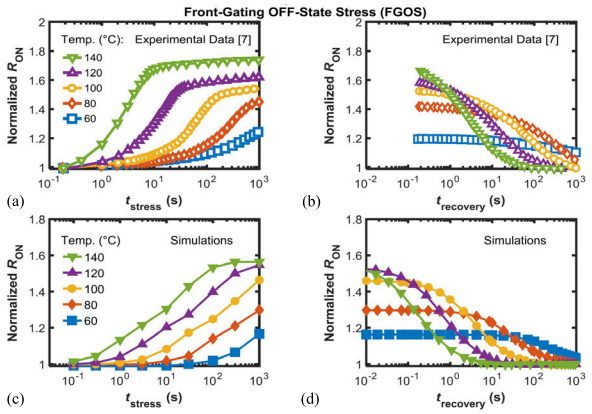

Fig. 4. (a) and (c) R_{ON} variations (normalized with respect to the prestress value) during OFF-state stress and (b) and (d) consequent recovery experiments (from [46]) and simulations carried out at different temperatures (see legend). Stress/recovery conditions are (V_G, V_D, V_B) = (−8, 25, 0) V and (V_G, V_D, V_B) = (0, 0.5, 0) V, respectively. (© [2021] IEEE, reprinted with permission from [18]).

at E_V + 0.9 eV, and a donor state close to the conduction band, when C possibly substitutes Ga, C_{Ga}. C_N level is largely dominant, and Fermi-level pinning at E_V + 0.9 eV occurs, thus making the GaN buffer slightly p-type.

The introduction of C enhances CC and dynamic on-resistance degradation during OFF-state stress. This is due to negative charge build-up in the gate–drain access region. In [52] and [78], the temperature dependence of the R_{ON} transients was studied in power MIS-HEMTs during front- and back-gating experiments, both during the stress and the recovery phase. The same value of activation energy has been found both for the charge build-up (R_{ON} increase) and for the detrapping phase (R_{ON} decrease).

The 2-D device simulations based on the hydrodynamic model of Synopsis SENTAURUS suggested that the activation energy of both the "stress" and the "recovery" processes could be directly attributed to the dominant acceptor trap energy level associated with carbon in the buffer, as a result of hole emission, redistribution, and retrapping in the C-doped buffer, as shown in Fig. 4 [52].

The build-up of negative charge is due to the ionization of C_N acceptors (consequent to hole emission). Peculiar features of trapping/detrapping due to C doping are the following: 1) at moderate stress levels, negative charge is located in the C-doped GaN buffer in the gate–drain region, thus affecting mainly R_{ON}, Fig. 3 (bottom); 2) since recovery involves hole reemission, redistribution, and capture, its time constant at room temperature is extremely long (1–10^3 s), thus possibly inducing significant memory effects, which hinder device operation and testing; and 3) hole emission is accelerated by electric field due to the Poole–Frenkel effect [79].

In [51], Fe- and C-doped 0.15-μm gate AlGaN/GaN HEMTs were submitted to drain voltage step-stress tests. Drain voltage stresses with a duration of 120 s were followed by 300-s unbiased recovery intervals; the drain voltage was incremented by 5-V steps. A complete dc characterization was carried out after each stress/recovery step. During these drain voltage step-stress experiments, we observed small degradation for Fe-doped devices in both OFF- and ON-state conditions, up to breakdown voltage, whereas enhanced R_{ON} and V_{TH} degradation was shown by C-doped devices due to charge accumulation. Two effects contributed to this larger degradation: 1) negative charge can only be partially detrapped during the recovery intervals of the step-stress test because of the very long recovery time of C-doped devices and 2) moreover, during ON-state tests, channel hot electrons can be captured by C_N states, thus inducing a semipermanent increase of V_{TH} and R_{ON}. As the energy offset between E_C and C_N is approximately 2.5 eV, hot electrons captured by C_N states cannot be emitted to the conduction band within the experiment time scale.

Also, in Fe-doped devices, the negative charge stored within the buffer increases during both OFF-state and ON-state stress (as a result of drain–source electron leakage current and channel hot electron injection, respectively), but, in this case, the effect is completely reverted during the recovery phases, due to the 10-ms time constant characterizing electron emission to the conduction band from the 0.56-eV Fe states. Consequently, C-doped GaN HEMTs can be potentially subject to a hot-electron-induced failure mechanism, which does not affect Fe-doped devices.

It should be noted, however, that short-term reliability, in particular for what concerns hot-electron effects, also depends on the interplay between charge trapping and electric field distribution. In [80], we compared the on-wafer reliability of 0.15-μm GaN HEMTs for microwave applications adopting Fe and C co-doping, with the same Fe doping profile, but different levels of C doping within the GaN buffer. At increasing C content, short-channel effects were reduced, at the expense of a slightly higher CC, related to the presence of C_N acceptors. Electroluminescence measurements suggested a decrease in the electric field and hot-electron effects in highly C-doped devices, possibly due to the virtual gating induced by the negative charge of the ionized acceptors in the gate–drain region. As a consequence, degradation in ON-state was stronger in devices having a lower C concentration. The dominant failure mode consisted in a positive threshold voltage shift.

VI. Effect of GaN Channel Thickness and Back Barriers in C-Doped GaN HEMTs

When a C-doped GaN buffer is used, the thickness of the undoped GaN channel and the C concentration in the doped buffer becomes most relevant epi design parameters [40], [53], [81]. At increasing C-doping, short-channel effects are reduced, but dynamic R_{ON} increase and hot-electron degradation are enhanced; the same occurs at decreasing undoped GaN channel thickness.

Figs. 5 and 6 (from [40]) clearly show the tradeoff between short-channel effects and trapping: a higher separation between channel and buffer corresponds to increased DIBL, higher drain–source leakage current in OFF-state, and enhanced short-channel effects, but CC is reduced, see Fig. 5. Higher C doping in the GaN buffer improves DIBL and OFF-state characteristics, including drain leakage but enhances trapping effects, thus confirming that the latter are due to C-related

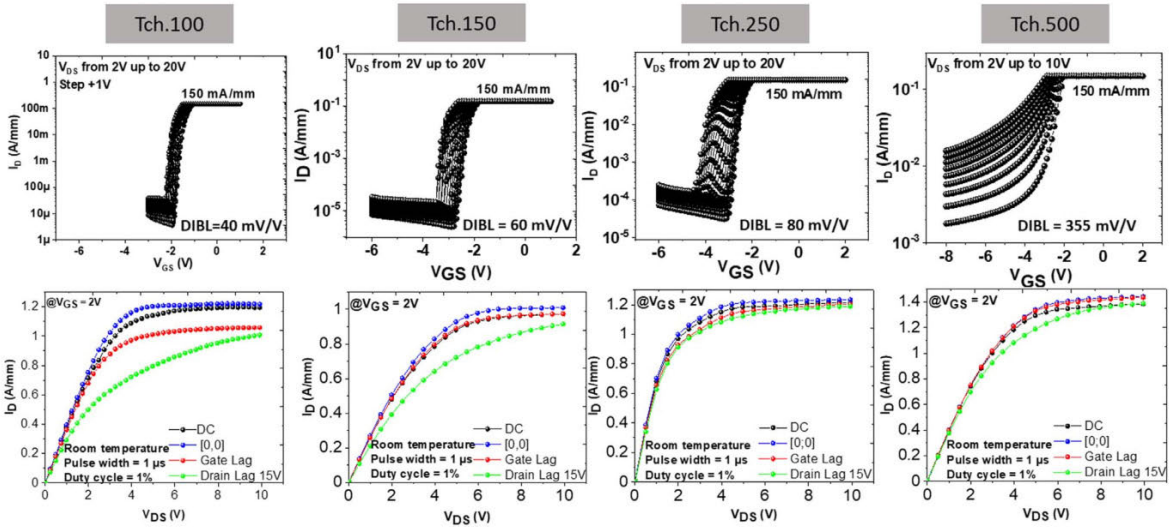

Fig. 5. Transfer characteristics up to $V_{DS} = 20$ V and open channel pulsed I_D–V_{DS} output characteristics of 2 × 50 μm AlN/GaN transistors with $L_{GD} = 1.5$ μm and $L_G = 100$ nm for various channel thicknesses. (© [2022] IOP, reprinted with permission from [40]).

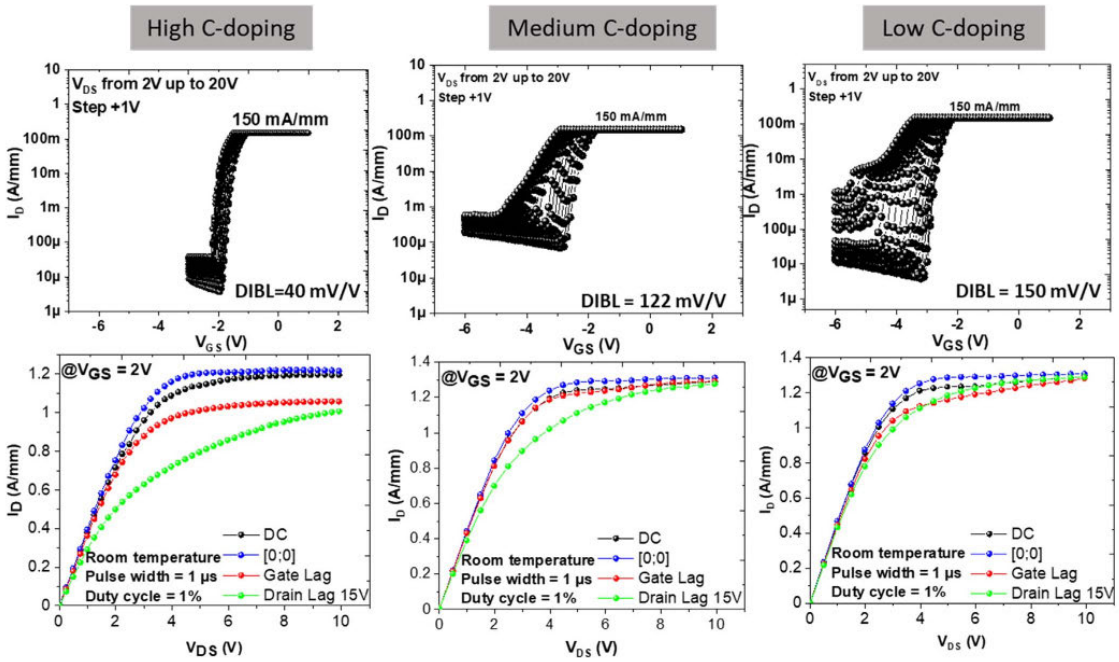

Fig. 6. Transfer characteristics up to $V_{DS} = 20$ V and open channel pulsed I_D–V_{DS} output characteristics of 2 × 50 μm AlN/GaN transistors with $L_{GD} = 1.5$ μm and $L_G = 100$ nm for various carbon doping concentrations in the GaN buffer. (©[2022] IOP, reprinted with permission from [40]).

defects, see Fig. 6. The related values of DIBL and leakage current are reported in Table I.

The effect of varying the thickness (0–300 nm) of the undoped GaN channel grown on a C-doped GaN buffer has also been studied in [53]. It has been found that when channel thickness becomes thinner, the 2DEG sheet resistance as well as the metal-2DEG contact resistance increase. This has been attributed to pinning of the Fermi level close to the valence band edge, due to C_N acceptors, and to reduction in channel mobility. Moreover, a possible lower quality of the GaN epitaxial layer closer to C-doped GaN cannot be excluded. Transconductance (g_m) in the linear region decreases as channel thickness is reduced; on the contrary, at $L_g = 90$ nm and $V_{DS} = 10$ V, the g_m peak increases as the channel thickness is decreased. A stronger knee CC was found in the case of channel thicknesses of 35 and 50 nm compared to 100 nm.

During short-term OFF-state reliability tests, the increased dispersion of R_{ON}, g_m, and V_{TH} was observed for thinner channels and was attributed to the increased interaction of 2DEG with C-related defects. Finally, thin channel devices have increased thermal resistance, due to reduction in lateral heat spreading.

When trying to solve the tradeoff between reducing short-channel effects and avoiding trapping, a further degree of freedom can be gained by introducing wide bandgap back barriers, either C-doped or undoped, between the undoped

TABLE I
DIBL AND OFF-STATE LEAKAGE FOR VARIOUS CHANNEL THICKNESSES FOR SAMPLES HAVING A C CONCENTRATION OF 2×10^{19} cm^{-3} (TOP) AND FOR DIFFERENT C DOPING WITH A CONSTANT CHANNEL THICKNESS OF 100 NM. DATA TAKEN FROM FIGS. 5 AND 6, [40]. DIBL IS MEASURED BETWEEN 2 AND 20 V. DRAIN–SOURCE LEAKAGE CURRENT IS EVALUATED AT $V_{GS} = V_{TH} - 1$ V AND $V_{DS} = 20$ V

Constant doping C = 2 ´10^{19} cm^{-3}	Channel thickness	(100 nm)	(150 nm)	(250 nm)	(500 nm)
	DIBL (mV/V)	31	60	80	357
	Off state I_{DS} leakage, μA/mm	~40	~80 μA	~400	~10000
Constant channel thickness, 100nm	C doping, cm^{-3}	2 ´ 10^{19} cm^{-3}	5 ´ 10^{18} cm^{-3}	1 ´ 10^{18} cm^{-3}	n.a.
	DIBL (mV/V)	40	122	150	
	Off state I_{DS} leakage, μA/mm	~80	~600	~1000	n.a.

GaN channel and the C-doped buffer. Several research groups have tried to reduce the interaction between 2DEG electrons and deep levels in the C-doped GaN buffer using this approach [20], [53], [54], [63], [64]. Yu et al. [54] have studied trapping in C-doped GaN buffer and back barrier by submitting ungated TLM structures to electrical stress. GaN buffer was 1 μm thick, with 6×10^{19} cm^{-3} doping; the barrier layer on top of the undoped GaN channel was either $Al_{0.28}Ga_{0.72}N$ or $In_{0.18}Al_{0.82}N$ (the latter for studying the effect of increased 2DEG carrier density), with or without an undoped $Al_{0.08}Ga_{0.92}N$ back barrier. Consistently with [53], they found that reducing the GaN channel thickness enhances electron confinement but reduces the 2DEG density and enhances dynamic R_{ON} increase. The latter effect has been attributed to trapping in the C-doped buffer or at the back barrier. This is confirmed by the observation that in devices without back barrier, dynamic resistance increase is proportional to $1/th_{ch}$, where th_{ch} is the undoped channel thickness. Insertion of an undoped $Al_{0.08}Ga_{0.92}N$ back barrier reduces both the interaction with the buffer and the back-gate capacitance C_{BG}, thus decreasing dispersion effects.

Yu et al. [54] suggested that the optimum back-barrier design (Al%, thickness, and C concentration in the buffer) should be based on imposing flat energy band within the AlGaN back barrier as a criterion. In this way, the negative C_N charges are screened by the net positive polarization charge at the i-AlGaN/C-doped GaN interface, while the net negative polarization at the i-GaN/i-AlGaN interface provides 2DEG confinement and alleviates short-channel effects.

Harrouche et al. [20] studied the effect of a 100-nm AlGaN back barrier inserted between an undoped 150-nm GaN channel layer and the GaN buffer, the latter moderately doped with C (5×10^{18} cm^{-3}). An ultrathin (3 nm) AlN top barrier was adopted to increase the 2DEG density. The Al concentration in the back barrier was varied between 4% and 25%. At increasing Al content, short-channel effects were progressively mitigated, while trapping effects remained low due to the reduced C concentration. For Al% = 25%, 0.1-μm gate transistors measured at $V_{DS} = 20$ V by load–pull at 40 GHz (CW) provide PAE > 65% and $P_{out} = 3.5$ W/mm. At $V_{DS} = 25$ V, PAE = 57.5% and P_{out} increases up to 4.8 W/mm. By reducing thermal effects in pulsed mode (1 μs and 1% duty cycle) at $V_{DS} = 30$ V, P_{out} reaches 7.1 W/mm with PAE > 60% [20].

In [63] and [64], we studied the effect of a thin undoped AlGaN barrier between undoped GaN channel and C-doped AlGaN buffer. Devices with the additional AlGaN layer have been identified as "bilayer" back-barrier devices, as opposed to "monolayer" devices where the undoped GaN channel was grown directly on the C-doped AlGaN buffer. The "monolayer" devices showed a knee voltage walkout in the I_D–V_{DS} characteristics and a larger R_{ON}, possibly due to enhanced trapping effects. They also show a smaller ratio of electroluminescence intensity (EL) to drain current ratio, EL/I_D, in ON-state, demonstrating a lower electric field as opposite to "bilayer" devices. This electric field decrease could be the result of negative charge trapped in the gate–drain access region.

Deep-level current transient spectroscopy (DCTS) detected two deep levels in "monolayer" devices, one with time constant close to 50 s at 30 °C, having an activation energy E_a close to 0.9 eV and attributed to C; a second one with time constant close to 100 ms and $E_a = 0.82$ eV, unidentified. In "bilayer" devices, there is no signature of the C-related level and a single trap is observed, with 100-ms time constant and $E_a = 0.58$ eV. Results of on-wafer step-stress tests show that degradation in monolayer devices is: 1) much higher in devices having larger GD distance; 2) larger in devices without field plate; 3) it consists in a decrease of transconductance without a shift of threshold voltage; and 4) it is much larger in semi-ON and ON-state than in OFF-state. On-state degradation is enhanced in "monolayer" C-doped devices compared to "bilayer" and Fe-doped reference devices, Fig. 7. Dominant deep-level activation energy is 0.9 eV (attributed to C) in monolayer devices and 0.58 eV in bilayer devices (possibly a trap at the GaN/AlGaN back interface), which do not show any presence of C in DCTS measurements. We therefore attributed degradation of monolayer devices to the interaction of hot electrons with deep levels in the C-doped buffer region, leading to negative charge build-up in the gate–drain access region. By using a "bilayer" AlGaN barrier, the interaction between C-related deep levels and channel hot electrons can be effectively reduced, thus alleviating the recoverable parametric degradation due to trapping effects.

In another experiment, 0.15-μm InAlN/GaN and InAlGaN/GaN HEMTs were implemented using either a Fe-doped GaN buffer or a thick high-resistivity GaN buffer incorporating an AlGaN back barrier, see Fig. 8 [82], [83]. The best performance was obtained for $In_{0.18}Al_{0.82}N$ ternary barrier, with $I_D = 0.8$ A/mm $g_m = 550$ mS/mm, $I_G < 10^{-4}$ A/mm @ $V_{DG} = 17$ V, $R_{ON} < 2$ Ω-mm, SS < 100 mV/decade, $L_{GS} = 0.8$ μm, and $L_{GD} = 1.5$ μm. CC or slump ratio (SR) was defined as

$$\mathrm{CC} = \mathrm{SR} = 1 - \frac{I_{\mathrm{DS,stress}}}{I_{\mathrm{DS,withoutstress}}}\%.$$

For both Fe-doped and back-barrier devices, CC is due to dynamic positive threshold voltage shift, demonstrating that trapping occurs under the gate and not in the access regions. Both InAlN and InAlGaN back-barrier devices

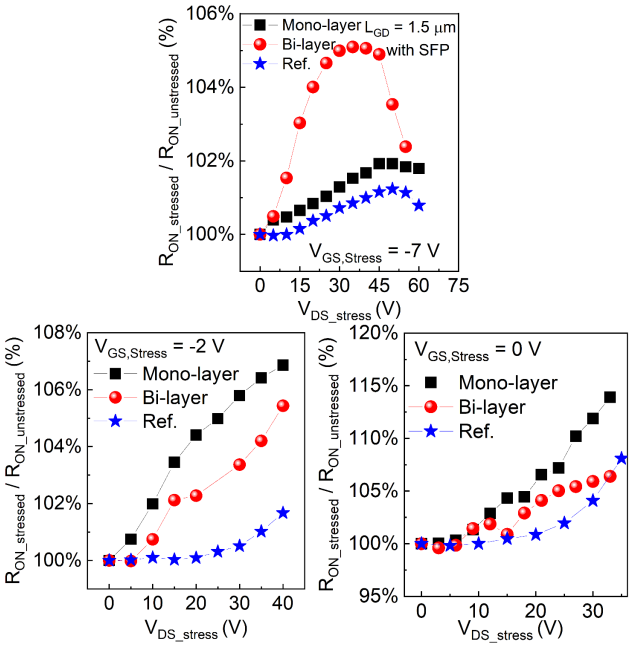

Fig. 7. R_{ON} increase during step-stress tests in devices from "bilayer," "monolayer," and Fe-doped reference wafers: OFF-state test at $V_{GS,Stress} = -7$ V (top); semi-ON state test at $V_{GS,Stress} = -2$ V (bottom left); ON-state test at $V_{GS,Stress} = 0$ V (bottom right). (Devices have $L_{GD} = 1.5$ μm, with SFP; R_{ON} is calculated from the slope of the linear least square fitting of the linear region of I_D–V_{DS} curves, V_{DS} from 0 to 0.5 V). (© [2022] IEEE, reprinted with permission from [63]).

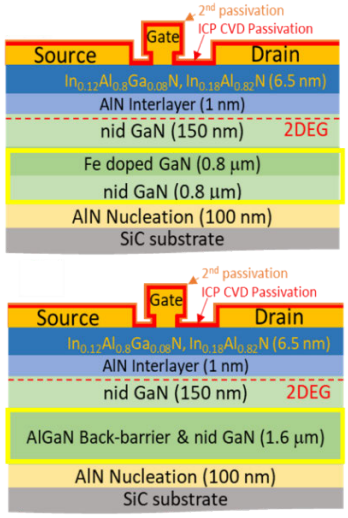

Fig. 8. Schematic cross section of a 0.14-μm GaN HEMT having InAl(Ga)N top barrier and Fe-doped GaN buffer (top). Cross section of a GaN HEMT with the same option for the top barrier, but undoped GaN/AlGaN back barrier (bottom).

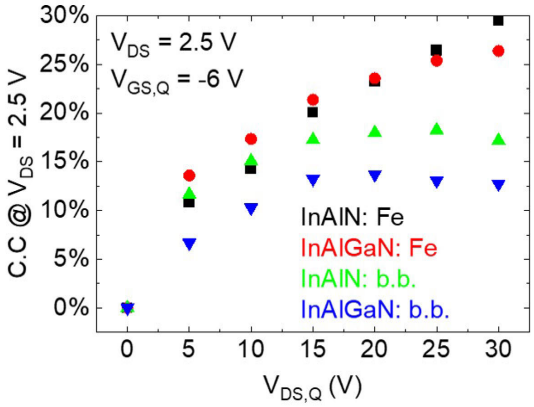

Fig. 9. CC as a function of stress $V_{DS,Q}$ in a double-pulse test of InAl(Ga)N/GaN HEMTs with either Fe-doped GaN buffer or GaN/AlGaN back barrier. Devices were kept in OFF-state at $V_{GS,Q} = -6$ V for 99 μs and then measured at $V_{DS} = 2.5$ V and $V_{GS} = 0$ V for 1 μs.

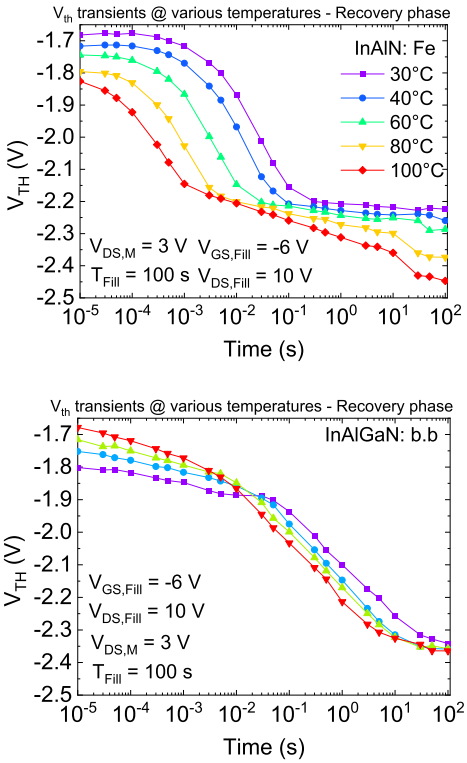

Fig. 10. Dynamic V_{TH} transient in a 0.15-μm InAlN/GaN HEMT with undoped GaN channel over Fe-doped GaN buffer (top). V_{TH} transient in an InAlGaN/GaN HEMT with undoped AlGaN back barrier (bottom). Devices have been stressed in OFF-state for 100 s at $V_{DS} = 10$ V, $V_{GS} = -6$V. V_{TH} is measured at $V_{DS} = 3$ V.

have significantly lower CC with respect to Fe-doped one, see Fig. 9; drain current and threshold voltage transient measurements confirm that dispersion effects in Fe-doped devices are due to deep levels at 0.59 eV, usually correlated with Fe, see Fig. 10 (top); on the contrary, dynamic threshold shift observed in back-barrier devices is originated by C-related defects, with $E_a = 0.7$–0.8 eV, inducing slow I_D recovery transients (up to 100 s), see Fig. 10 (bottom).

Finally, Fe-doped and back-barrier devices have been submitted to OFF-state step-stress tests at $V_{GS} = -5$ V, increasing V_{DS} in 5-V steps from 0 to 50 V, 120 s/step. All devices survived the step-stress test without catastrophic failure. No significant effect was found in Fe-doped devices; for $V_{DS} > 20$ V, in back-barrier devices, a negative V_{TH} shift was observed, due to dynamic detrapping of negative charge, possibly induced by deep-level impact ionization. InAlN and InAlGaN back-barrier GaN HEMTs have been demonstrated to be suitable for reliable operation up to 45 GHz [83].

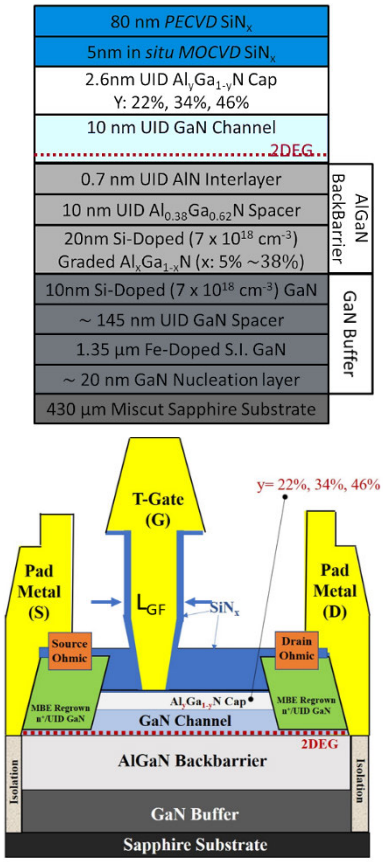

Fig. 11. Epitaxial structure (top) and device structure (bottom) of the N-polar MIS-HEMTs under test. (© [2021] IEE, reprinted with permission from [72]).

VII. Deep-Level Effects in N-Polar MISHEMTs

A solution to the tradeoff between short-channel effect and current density is provided by the N-polar GaN HEMT structure, where the 2DEG is close to the surface and the AlGaN barrier is below the undoped 10-nm GaN channel layer, see Fig. 11. The gate–2DEG distance is reduced, thus maintaining the aspect ratio; the underlying AlGaN layer acts also as a back barrier, contributing, together with a 0.7-nm AlN interlayer and a 10-nm unintentional doped (u.i.d) AlGaN spacer, to separate the electrons from the Fe-doped GaN buffer and the nucleation layer.

We tested N-polar MISHEMTs adopting the process described in [84]. A thin (2.6 nm) AlGaN cap layer was placed on top of the u.i.d GaN channel layer to minimize leakage current and prevent possible dispersion effects. The devices have a T-cap gate shape; the examined transistors have gate foot lengths L_{gf} between 80 and 100 nm, and three different concentrations of Al as 22%, 34%, and 46% in the $Al_xGa_{1-x}N$ cap layer.

Fig. 12 (top) shows the values of gate leakage current (I_G) measured at $V_{GS} = -7$ V and $V_{DS} = 15$ V for devices with different Al concentrations in the cap layer. By increasing the Al%, leakage current is reduced from 70 μA/mm for Al% = 22 to 9 μA/mm for Al% = 46. Correspondingly CC (or SR), as well as I_G, decrease with Al%, reaching 15% for samples with Al% = 46, see Fig. 12 (bottom). CC was found

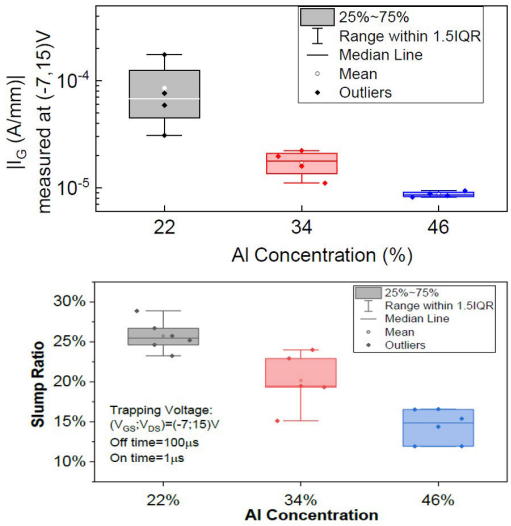

Fig. 12. Gate leakage current measured at $V_{GS} = -7$ V and $V_{DS} = 15$ V for 80–100-nm gate-length N-polar GaN HEMTs with different Al concentrations in the cap layer. Median leakage was found to be 9 μA/mm for Al% = 46%, compared to nearly 70 μA/mm for Al% = 22% (top). Variation of CC, with Al concentration in the AlGaN cap layer. N-polar GaN MIS-HEMTs have been biased at ($V_{GS,Q}$, $V_{DS,Q}$) = (-7 V, 15 V) for 100 μs; pulsed I_D–V_{DS} measurements at $V_{GS,MEAS} = -1$ V; SR has been calculated at $V_{DS,MEAS} = 8$ V (bottom). (© [2021] IEEE, reprinted with permission from [72]).

TABLE II
Main 2DEG and Electrical Properties of Tested Devices (n.a. = Not Available). Devices Are Identified by the Relevant Figure Number

Fig. #	Device	2DEG ns, μ_n cm^{-2} cm^2/Vs	I_D mA/mm	g_m mS/mm	SS mV/dec	DIBL mV/V	Note
1, 2	0,5 µm Fe	n.a.	620	320	224 (V_{DS}=7V)	n.a.	AlGaN/GaN HEMT
4	MISHEMT	n.a.	400	200	90	n.a.	
5	AlN/GaN	2×10^{13} 950	n.a.	n.a.	n.a.	60	t_{ch}=150 nm C: 10^{19} cm^{-3}
6	AlN/GaN	2×10^{13} 950	n.a.	n.a.	n.a.	40	t_{ch}=100 nm C: 2×10^{19} cm^{-3}
7	monolayer	$1,07\times10^{13}$ 2086	910	430 V_{DS}=8V	128 (V_{DS}=10V)	46	AlGaN/GaN HEMT single BB
7	bilayer	$1,11\times10^{13}$ 2049	880	410 V_{DS}=8V	127 (V_{DS}=10V)	41	AlGaN/GaN HEMT bilayer BB
8 ,9	InAlN, Fe	$1,15\times10^{13}$ 1707	735	417 V_{DS}=4V	260 (V_{DS}=4V)	12	InAlN/GaN Fe doped
8 ,9	InAlGaN, Fe	$1,4\times10^{13}$ 1743	712	396 V_{DS}=4V	216 (V_{DS}=4V)	24	InAlGaN/GaN Fe doped
8 ,9	InAlN, BB	$1,2\times10^{13}$ 1546	663	431 V_{DS}=4V	122 (V_{DS}=4V)	15	InAlN/GaN BB
8 ,9	InAlGaN, BB	$1,3\times10^{13}$ 1542	778	528 V_{DS}=4V	100 (V_{DS}=4V)	28	InAlGaN/GaN BB
11	22%Al	$1,3\times10^{13}$ 1728	830	400 V_{DS}=5V	78	33	N-polar HEMT
11	34%Al	n.a.	880	420 V_{DS}=5V	n.a.	n.a.	N-polar HEMT
11	46%Al	n.a.	1090	540 V_{DS}=5V	n.a.	n.a.	N-polar HEMT

to be due to a positive threshold voltage shift [71], [72]; the amount of degradation is independent of the gate length in the 80–100-nm range. The activation energy of the threshold

voltage recovery transient is 0.7 eV for all Al concentrations: the same trap located under the gate is responsible for CC; trapped charge and CC are originated by the gate leakage current.

VIII. Conclusion

The control of short-channel effects in deep-submicron-gate GaN HEMTs for microwave and millimeter-wave applications requires radical changes in the device epitaxial structure. Compensation with Fe does not allow sharp profiles to be implemented and introduces severe CC effects. High C-doping leads not only to CC, long recovery times, and memory effects but also to potential reliability problems due to hot electrons. As shown in this article, significant improvements in short-channel and dispersion effects have been achieved using single or composite AlGaN back barriers, which help suppress both OFF-state drain leakage current as well as drain CC. Back barriers can also improve device reliability, by reducing hot-electrons trapping in the substrate. It should be stressed, however, that the tradeoff between short-channel effects and dispersion effects requires, in general, the use of back barriers in combination with C or Fe doping. Very good device performances up to 45 GHz have been obtained by coupling AlGaN back barriers with InAlN or AlN top barriers [6], [50]. Table II summarizes the 2DEG properties and main electrical characteristics of tested GaN HEMTs, which were described in this present article.

In N-polar HEMTs, CC effects can be remarkably reduced by introducing an $Al_{0.46}Ga_{0.54}N$ cap layer, consequently reducing gate leakage current, leading to excellent performances up to 94 GHz [24], [25].

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