Report of GaN HEMTs on 8-in Sapphire

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***Abstract*—The two crucial factors of large scale and high voltage can hardly be balanced for the traditional GaN HEMTs on Si substrates. Recently, one promising solution, GaN-on-sapphire, has attracted great attention. However, the commercialized GaN-on-sapphire wafers ever reported are usually 6 in. It is urgent to develop 8-in GaN-on-sapphire to reduce the cost and meet the market demands. In this work, to the best of our knowledge, an 8-in GaN-on-sapphire wafer is demonstrated for the first time. The sheet resistance $R_{\square}$ exhibits a wafer-level nonuniformity of 4% and an average value of 310 $\Omega/\square$, and the warpage is kept to 30 μm, by dedicatedly tuning the 1.98-μm buffer stack. The fabricated 200-V HEMTs exhibit a low R_{ON} of 6.5 $\Omega\cdot$mm, a V_{TH} of -4.2 V, and an OFF-state breakdown voltage above 500 V without any field plate. The electrical mapping visualizes R_{ON} and V_{TH} distributed in concentric circles across the wafer. Generally, this work demonstrates the feasibility of realizing 8-in GaN-on-sapphire for power electronics applications in the future.**

***Index Terms*—8-in sapphire, GaN HEMTs, power electronics.**

I. Introduction

GaN HEMTs are expected to be applied in industrial applications since 2024. The current–voltage rating of the commercial GaN HEMTs is still mainly ≤650 V and aimed at the applications of fast chargers, class D-Audio, e-tools, and home appliances [1], [2], [3], [4], [5], [6], [7]. Industrial and even vehicle applications are expected to be accelerated since 2024 [8], [9]. However, huge demands of ≥650 V power devices for the areas of motor drivers and charging piles are rapidly growing [10], [11], [12].

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Recently, great interests have been raised for a new technique, i.e., GaN-on-sapphire [13]. First, GaN buffer can be much thinner, and kV-blocking capability can be easily obtained because of the insulating substrate [14]. Second, the cost is expected to reduce, considering the simple epitaxy and device structures. Third, GaN-on-sapphire is compatible with the existing silicon production lines [15]. The 1200-V d-mode GaN switches on sapphire for a 900:450 V buck converter have been presented by Transphorm [16], [17]. Later, p-GaN gate HEMTs on sapphire with a high breakdown voltage V_{BD} of 1.4 kV were demonstrated [18]. We have recently presented the 1700-V d-mode GaN HEMTs on sapphire with a 1.5-μm buffer [14] and 8000-V GaN HEMTs by CMOS-compatible processing [19]. Wu et al. [20] presented a structure of actively passivated p-GaN gate HEMTs on sapphire to suppress the dynamic R_{ON} [21]. Li et al. [22] further adopted GaN-on-sapphire for monolithically integrating 1200-V half-bridge and drivers.

Until now, the sapphire substrates used for GaN devices usually have a diameter of 6 in or even smaller. Therefore, larger diameter GaN-on-sapphire wafers are urgently needed to compete with GaN-on-Si that has reached 12 in [23]. Benefiting from the upcoming mass production of the 8-in sapphire substrates [24], the feasibility of developing 8-in GaN-on-sapphire technique is ready. In this work, epitaxy and device processing will be introduced first. Then, crystal quality, warpage, and wafer-level uniformity will be assessed. Finally, the dynamic performance of the fabricated 200-V HEMTs will be evaluated.

II. Epitaxy and Fabrication

The HEMT structure was epitaxially grown by a metalorganic chemical vapor deposition (MOCVD) system on an 8-in 1150-μm-thick sapphire substrate, as shown in Fig. 1. The epitaxy stack consists of a 35-nm AlGaN nucleation layer, a 1.98-μm GaN buffer layer, a 420-nm GaN channel layer, a 1-nm AlN spacer, a 21-nm $Al_{0.27}Ga_{0.73}N$ barrier layer, and, finally, a 2-nm in situ SiN cap layer.

As shown in Fig. 1, the device processing was commenced by first evaporating the Ti/Au (20/50 nm) lithography marks by e-beam evaporation and liftoff. Then, the ohmic contact was made via SiN etching by reactive ion etching (RIE), Ti/Al/Ni/Au (20/140/55/45 nm) evaporation, and rapid thermal annealing (RTA) at 830 °C for 30 s in the ambient of N_2. Later, the device isolation was conducted through multiple

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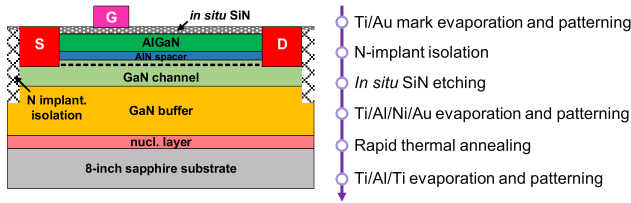

Fig. 1. Cross-sectional schematic of the fabricated GaN HEMTs on the 8-in sapphire and the processing flow.

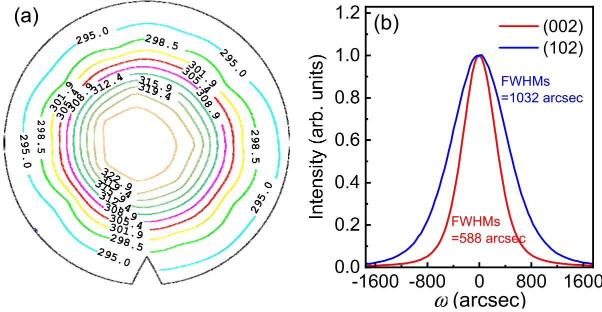

Fig. 2. (a) Mapping of the contactless sheet resistance $R_{\square}$. (b) XRD (002) and (102) rocking curves of the AlGaN/GaN HEMT structure epitaxially grown on 8-in sapphire.

conditions of N ion implantation with energies of 80, 140, and 250 keV [25]. Finally, the processing ended with evaporating Ti/Al/Ti (20/80/20 nm) as gate metal.

The fabricated GaN HEMTs on 8-in sapphire have a gate width W_G of 100 μm, a gate length L_G of 4 μm, a gate–source distance L_{GS} of 1.5 μm, and a gate–drain distance L_{GD} of 6 μm. The crystal quality was characterized by X-ray diffraction (XRD), wafer warpage was measured by photoluminescence (PL) mapping, the sheet resistance $R_{\square}$ was measured by contactless Hall measurement, and electrical characterizations were performed by Keysight B1500A and B1505A.

III. Results and Discussion

The sheet resistance $R_{\square}$ of the fabricated 8-in GaN-on-sapphire wafer exhibits a wafer-level nonuniformity of 4% and average value of 310 $\Omega/\square$, as shown in Fig. 2(a). Fig. 2(b) shows the ω-rocking curves for (002) and (102) planes of the GaN buffer on sapphire. It is clear that the full-width at half-maximum (FWHM) of ω-rocking curves for (002) and (102) planes is 588 and 1032 arcsec, respectively. Further improvement of the epitaxy uniformity and quality can be made by tuning the buffer stack, gas flow, chamber pressure, temperature field, and so on. Fig. 3 shows the warpage of the 8-in GaN-on-sapphire wafer is only 30 μm, thanks to the dedicated buffer stack design.

The fabricated 8-in GaN-on-sapphire wafer is demonstrated in Fig. 4. Fig. 5(a) plots the output characteristics of the fabricated 200-V GaN HEMTs, where the ON-resitance R_{ON} reaches 6.5 $\Omega \cdot$ mm corresponding to L_{GD} of 6 μm. The transfer characteristics of ten devices are depicted in Fig. 5(b), indicating that the threshold voltage V_{TH} reaches -4.2 V.

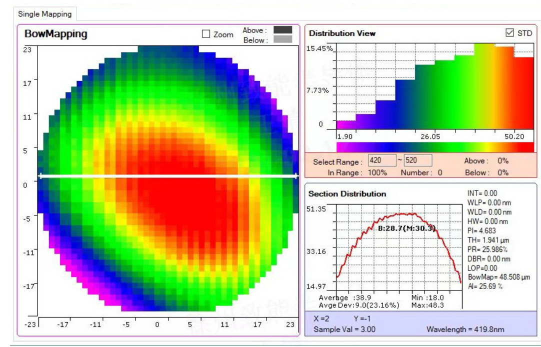

Fig. 3. Warpage of the 8-in GaN-on-sapphire wafer measured by PL mapping.

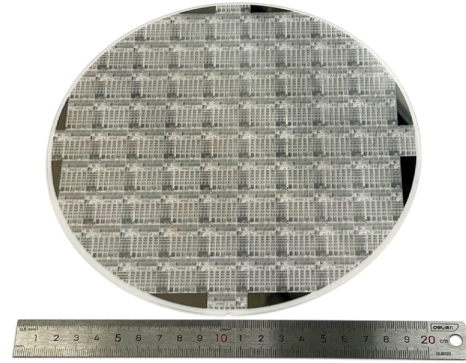

Fig. 4. Photograph of the fabricated 8-in GaN-on-sapphire wafer.

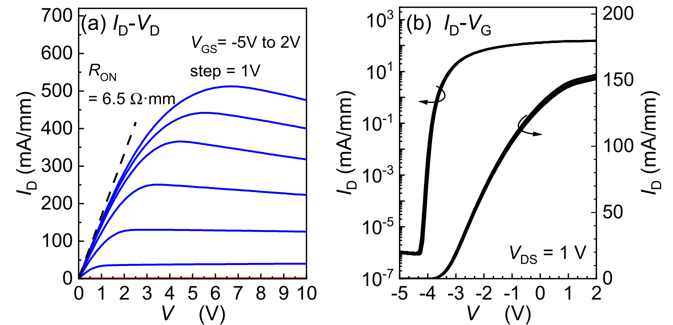

Fig. 5. (a) Output and (b) transfer characteristics of the 200-V GaN HEMTs with L_{GD} of 6 μm on 8-in GaN-on-sapphire.

Electrical mapping of R_{ON} and V_{TH} was then conducted, as illustrated in Fig. 6. The V_{TH} values range from -4.15 to -3.16 V, and the R_{ON} values range from 6.49 to 8.59 $\Omega \cdot$ mm. It is not difficult to observe the relatively higher V_{TH} and R_{ON} values concentrated in the center of the 8-in wafer, which is consistent with the contactless $R_{\square}$ contour in Fig. 2(a). This is an intrinsic problem of the MOCVD chamber. Moreover, the contact resistance R_C of the fabricated devices suffers a wide distribution of 0.7–1.5 $\Omega \cdot$ mm, which also jeopardizes the uniformity of R_{ON}.

The OFF-state breakdown characterizations were then conducted on the 200- and 650-V HEMTs. As shown in Fig. 7, for the devices with L_{GD} of 6 μm, the OFF-state breakdown voltages exceed 500 V without any field plate, which is sufficient for the 200-V devices. For the devices with L_{GD} of 16 μm, the OFF-state breakdown voltages exceed 1200 V.

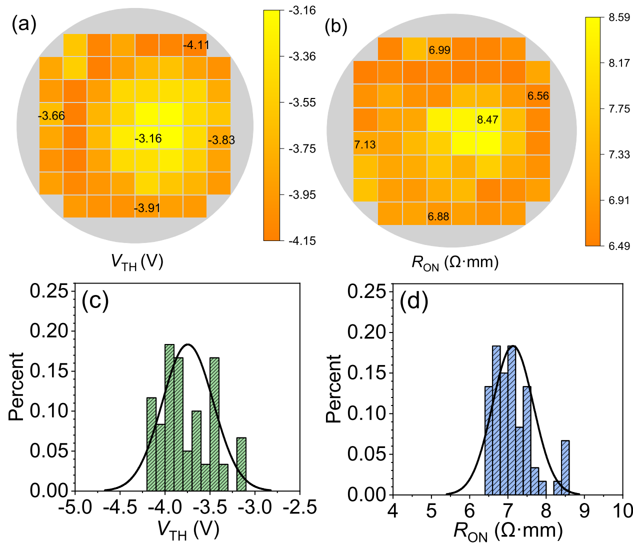

Fig. 6. (a) Electrical mapping and (c) statistical distribution of V_{TH}, and (b) electrical mapping and (d) statistical distribution of R_{ON} of the 200-V HEMTs across the 8-in GaN-on-sapphire wafer.

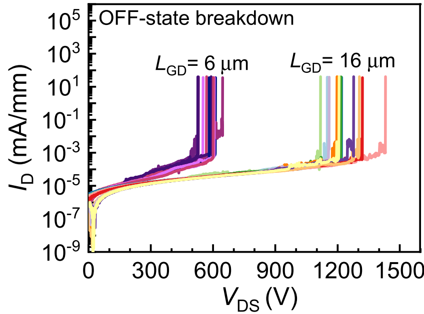

Fig. 7. OFF-state breakdown characteristics of the 200-V HEMTs with L_{GD} of 6 μm and 650-V HEMTs L_{GD} of 16 μm.

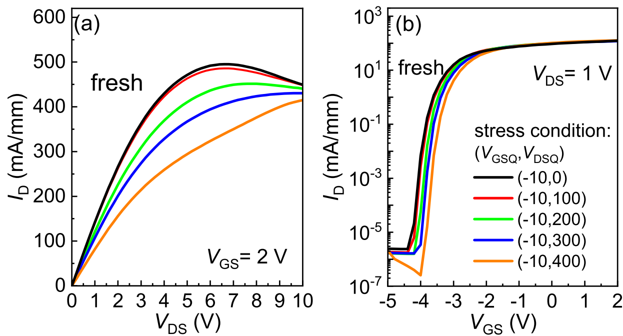

Fig. 8. (a) I_D–V_D and (c) I_D–V_G curves of the 200-V GaN HEMTs on sapphire with L_{GD} of 6 μm after various OFF-state stresses.

Further improvement can be made through dedicated field plate design and passivation [14].

The 200-V device was then subjected to high-voltage OFF-state stress to assess the dynamic performance. During the measurements, the device was first stressed for 1 s in OFF-state under various stress conditions and then quickly subjected to I_D–V_D and I_D–V_G measurements. We can see from Fig. 8(a) that the current collapse is aggravated until 400 V by 41%. However, for the 200-V stress, which is the most strict stress condition in application for the 200-V HEMTs, the current collapse is as low as 15%. The current collapse is jointly induced by the V_{TH} shift as in Fig. 8(b) and trapping effect in the access region [26]. Results in our work are comparable with that of the GaN-on-SiC [27]. Further suppression of dynamic R_{ON} can be made through field plate design [28].

IV. Conclusion

An 8-in GaN-on-sapphire wafer, a landmark technique, has been successfully demonstrated. Wafer warpage and uniformity have been tuned by dedicatedly designing the buffer stack and epitaxy. GaN HEMTs have been fabricated on the 8-in wafer with a simple processing and device structure. The wafer-level uniformity is visualized by the electrical mapping of the devices. Moreover, the OFF-state blocking capability and dynamic reliability of the devices have also been evaluated and qualified. The 8-in GaN-on-sapphire, although suffers certain nonuniformity due to the limitations of epitaxy and processing facilities, anyhow verifies the feasibility of fabricating low-cost and high-voltage lateral HEMTs on large-scale sapphire substrates, which might lead power semiconductor to a new age.

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