Effects of Electron Quantum Confinement on Velocity Overshoot in Si Nanosheet Gate-All-Around FETs

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***Abstract*— We study the relationship between velocity overshoot (VO) and quantum confinement (QC) in electron transport in Si nanosheet (NS) gate-all-around (GAA) field-effect transistors (FETs) through device simulation. VO is incorporated into the simulation with an energy transport (ET) model, and QC with a density-gradient (DG) model. We measure the effects of VO on the NS FETs by comparing their static characteristics obtained with the ET model and with a drift–diffusion (DD) model, which essentially cannot consider VO, and then examine the differences in the VO effects between the cases with and without QC. VO increases the drain current, and QC enhances this increase by gathering electrons inside the NS. This enhancement increases as the gate length decreases, although it eventually begins to decrease. It also generally increases as the gate voltage decreases. However, it shows a more complex behavior for a change in NS thickness, depending on the gate length and gate voltage. These behaviors of the VO effect enhancement by QC can be well explained from the effective potential acting on electrons in the NS.**

***Index Terms*— Device simulation, gate-all-around (GAA), nanosheet (NS) field-effect transistor (FET), quantum confinement, technology computer-aided design (TCAD), velocity overshoot.**

I. Introduction

TECHNOLOGICAL and industrial development of artificial intelligence is gaining momentum, with chatbot software based on large language models becoming popular in a significantly short period, and the demand for computational resources is expected to continue to grow. Processors and memories, representatives of physical computational resources, have continuously achieved a higher performance by miniaturizing components, such as transistors, and integrating them in larger numbers on a chip. Si nanosheet (NS) gate-all-around (GAA) field-effect transistor (FET), in which Si NSs are used as channels with their sides covered with gate metal, is expected to be fabricated with scaled dimensions compared with Si fin FET, the current mainstream transistor for logic ICs, owing to its higher gate controllability over the potential in channels [2], [3], [4]. If this miniaturization can be achieved, NS FET–based ICs are expected to be superior to fin FET–based ICs in terms of not only area but also speed and power consumption [5], [6]. The NS FET also offers more flexibility in terms of effective gate width, which is advantageous in the design of ICs [7], [8]. For these reasons, it has been chosen as the successor to the fin FET and its research and development is being vigorously pursued to bring its products to market [9], [10], [11]. To this end, a detailed understanding of carrier transport in the NS FET is essential, which can be achieved with device simulation.

Carriers accelerated by a strong electric field can temporarily exceed their saturation velocity [12], [13], [14]. This phenomenon is known as velocity overshoot (VO) and is considered to affect the performance of FETs when the gate length is short. In this situation, ballistic transport is also considered to occur, in which carriers pass through a channel without experiencing scattering. As scattering sources such as phonons are always present, in reality, most of the carriers would be scattered even if only a few times, and the carrier transport would not be purely ballistic but quasi-ballistic. The carrier transport we assume in this study is such that carriers are not scattered frequently enough for their overshot velocity to settle down to the saturation velocity, which situation is similar to that in the quasi-ballistic transport. In fact, the previous study [15] has pointed out that VO can occur in quasi-ballistic transport. In addition, when carriers are confined to a narrow space, their quantum-mechanical behavior becomes pronounced. A typical example observed in FETs is that, at high gate voltages, the carrier density peak is slightly away from the semiconductor–insulator interface where the peak should be located according to classical mechanics [16]. This phenomenon is known as a quantum confinement (QC) effect. Both VO and QC will definitely affect the performance of NS FETs. Most device simulators can incorporate VO into the simulations with an energy transport (ET) model, commonly referred to as a hydrodynamic model, and QC with a quantum correction model such as a density-gradient (DG) model. Such simulations have been widely performed for various types of FETs, including NS FETs [17], [18], [19]. However, the interaction between VO and QC is not yet fully understood.

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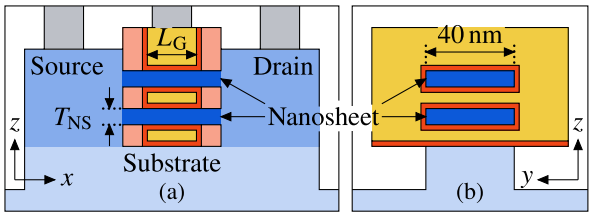

Fig. 1. Sectional views of Si NS GAA FETs along (a) the x-axis and (b) the y-axis, parallel to the gate length and width directions, respectively.

In this study, we investigate the effects of QC on VO in electron transport in Si NS GAA FETs using device simulation. To this end, we measure the effects of VO on device performance by comparing the static characteristics of the NS FETs obtained with and without the consideration of VO, and then examine how much the VO effects change depending on the presence or absence of QC. Although we have already demonstrated such changes in our previous work [20], here, we discuss them in detail along with their causes. The findings of this study will improve our understanding of electron transport not only in NS FETs but also in other ultrascaled FETs.

II. Simulation Framework

We employed the ET and DG models to incorporate VO and QC into the simulation, respectively. Although the two models are well known, their forms differ among device simulators. To clarify the forms and facilitate the discussion of the simulation results, we describe the two models below, as well as the device structure considered and the simulator used in this study.

A. Device Structure

Fig. 1 illustrates the structure of Si NS GAA FETs with a gate length of L_G. Each FET comprises two Si NSs with a thickness of T_{NS} and width of 40 nm, gate insulating films with a thickness of 2 nm and relative permittivity ε_{OX} of 7.8, and gate sidewalls with a thickness of 5 nm and relative permittivity of 5.0. Thus, the NS length is 14 nm longer than L_G. Moreover, the spacing between the two NSs and that between the lower NS and the substrate are 10 nm. In this study, the NS FETs were assumed to be of n-type. The donor concentration was N_{SD} in the source/drain and decreased away from there according to a Gaussian distribution with a standard deviation of 3 nm. The substrate was doped with acceptors at a concentration of 1×10^{18} cm^{-3} to weaken parasitic transistors. In addition, we set N_{SD} to 1×10^{20} cm^{-3}, the gate metal work function to 4.6 eV, and the supply voltage to 0.65 V.

B. Velocity Overshoot

The overshoot of carrier velocity in Si involves the energy dependence of carrier scattering [15]. In device simulation, carrier transport in semiconductors is usually described by a drift–diffusion (DD) model consisting of Poisson and current continuity equations. The DD model provides information on the number of carriers but not the energy. We therefore solved the following energy balance equation for electrons [21]:

$$\partial nw/\partial t + \nabla \cdot \boldsymbol{S} - \boldsymbol{J} \cdot \boldsymbol{\mathcal{E}} - H + n(w - w_0)/\tau_w = 0 \quad (1)$$

where n is the electron density, $\boldsymbol{J}$ the current density, w the average energy, w_0 its value in thermal equilibrium, H the net energy gain rate, τ_w the energy relaxation time, and $\boldsymbol{\mathcal{E}}$ the electric field. When only the thermal energy is considered, w and w_0 are approximated with $(3/2)k_BT$ and $(3/2)k_BT_{dev}$, where T and T_{dev} are the electron and device temperatures, respectively. Moreover, the energy flux density $\boldsymbol{S}$ is given by

$$\boldsymbol{S} = -(5/2)(\mu_S/\mu)(k_BT/q)(\boldsymbol{J} + \mu n k_B \nabla T) \quad (2)$$

where μ and μ_S are the electron mobility and its $\boldsymbol{S}$'s counterpart, respectively. The DD model in combination with the energy balance equation is called the ET model. In our simulation, it was applied to electron transport in the NSs and source/drain along with H given by [22]

$$H = (3/2)k_BT G_{SRH} + \left[(3/2)k_B(T - T_{dev}) - E_g\right]G_{Aug} \quad (3)$$

and τ_w given by [23]

$$\tau_w(\omega) = \left(0.27 + 0.62\omega - 0.63\omega^2 + 0.13\omega^3 + 0.01\omega^4\right)\tau_{w0}. \quad (4)$$

Here, G_{SRH} and G_{Aug} are the net generation rates of electron–hole pairs due to Shockley–Read–Hall and Auger recombinations, respectively; E_g is the bandgap energy; ω is w divided by 1 eV; and τ_{w0} is 1 ps. In addition, the mobility ratio μ_S/μ was set to 0.8 [21] and T_{dev} to 300 K. In the substrate, by contrast, the DD model was applied to electron transport and T was assumed to be equal to T_{dev}. Regarding hole transport, the DD model was used for all regions.

The energy dependence of electron scattering was represented by an energy-dependent mobility model. In the DD model, as a lateral field–dependent mobility model that determines the final value of carrier mobility, the following Caughey–Thomas model [24] was used:

$$\mu = \mu_{low}\left[1 + (\mu_{low}|\boldsymbol{\mathcal{E}}_{drv}|/v_{sat})^b\right]^{-1/b} \quad (5)$$

where $\boldsymbol{\mathcal{E}}_{drv}$ is the driving field, v_{sat} is the carrier saturation velocity, μ_{low} is the low-field mobility considering the effects up to the transverse field, and b is a fitting parameter. From this driving-field dependence of the carrier mobility, the energy dependence can be derived with the method described in [25]. Solving (1) with assumptions that the system is homogeneous and stationary and $H = 0$ yields the average energy that an electron will eventually have under a given $\boldsymbol{\mathcal{E}}_{drv}$ as

$$w(\boldsymbol{\mathcal{E}}_{drv}) = q\mu|\boldsymbol{\mathcal{E}}_{drv}|^2\tau_w + w_0. \quad (6)$$

By eliminating $\boldsymbol{\mathcal{E}}_{drv}$ from (5) with this equation, we obtained the energy-dependent mobility model for electrons. Note that, if T was lower than T_{dev}, μ was fixed at μ_{low}. When an electron under an $\boldsymbol{\mathcal{E}}_{drv}$ has an energy lower than that given by (6), its velocity can exceed v_{sat}, that is, VO can occur.

In the DD model, as $\boldsymbol{J}$ can be written as $\boldsymbol{J} = n\mu\nabla E_{qF}$ with the electron quasi-Fermi level E_{qF} if T is uniform, for electrons, $\boldsymbol{\mathcal{E}}_{drv}$ was assumed to be given by $\boldsymbol{\mathcal{E}}_{drv} = \nabla E_{qF}/q$. Moreover, v_{sat} was set to 1.07×10^7 cm/s and b to 1.109. Other settings of the DD model have been described in [26]; however, band-to-band tunneling was ignored in this study.

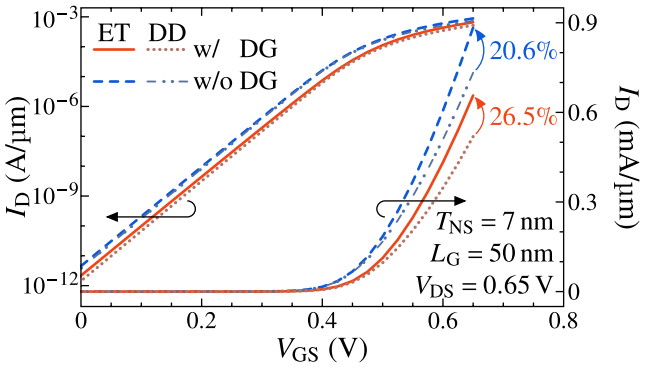

Fig. 2. I_D–V_{GS} characteristics of NS FETs with an L_G of 50 nm and T_{NS} of 7 nm at a V_{DS} of 0.65 V. The characteristics obtained with both ET and DG models are shown by the solid lines, those obtained with the DD model instead of the ET model by the lines containing dots, and those obtained without the DG model by the lines containing dashes. The values of I_D are normalized by the NS width, which is 40 nm.

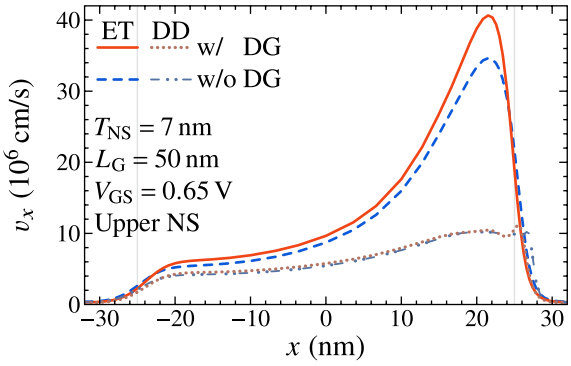

Fig. 3. Electron velocity in the x-direction v_x in the upper NS at a V_{GS} of 0.65 V. It is plotted along the x-axis after being averaged over each section with a weight of n.

C. Quantum Confinement

We incorporated electron QC into the simulation with the DG model [27], which introduces the quantum potential

$$U_{QC} = -\left(\hbar^2/6m_{QC}\right)\nabla^2\sqrt{n}\,/\,\sqrt{n} \tag{7}$$

for electrons, where m_{QC} is the electron effective mass related to QC. The quantity U_{QC} represents the influence of potentials at distant locations and, in practice, acts as a modifier of the conduction band edge E_C. For example, n is modified as

$$n = N_C \exp\left\{\left[E_{qF} - \left(E_C + U_{QC}\right)\right]/k_B T\right\} \tag{8}$$

where N_C is the conduction-band effective density of states.

As with the ET model, the DG model was applied to electrons in the NSs and source/drain. At the Si–insulator interface, the same boundary condition as described in [28] was used and the insulator was assumed to be made of SiO_2. The boundary condition parameters and m_{QC} were adjusted so that, for an NS with a T_{NS} of 7 nm, the profile of n along the central axis in the T_{NS}-direction is close to that obtained from a one-dimensional Schrödinger–Poisson equation. Then, m_{QC} was determined to be $0.14m_0$ for Si and $0.08m_0$ for SiO_2. The latter value is required for the boundary condition. At the interface of the source/drain with the substrate and electrodes, U_{QC} was assumed to be zero.

D. Device Simulator

We used our homemade device simulator, Impulse TCAD [29], to simulate NS FETs. Although Impulse TCAD solves equations with the Newton method, it automatically calculates the Jacobians of the equations at run time. Thanks to this feature, users can easily incorporate their own models into simulations without providing the models' Jacobians, and besides through simulation control scripts without hard coding the models. In this way, we incorporated the ET and DG models into the simulation. Both models are widely used; however, they have limitations [21], [30]. To verify our simulation framework, including the models' validity, we simulated the three-layer NS FET with an L_G of 12 nm and T_{NS} of 5 nm [9]. The simulation results were found to be in reasonable agreement with the experimental data on drain current I_D versus gate-to-source voltage V_{GS} characteristics under assumptions that ε_{OX} is 9.0 and N_{SD} is $6 \times 10^{19}\,\mathrm{cm}^{-3}$. Furthermore, no serious problems were observed that could be attributed to the models' limitations. Note that the unit of the experimental I_D was assumed to be $10^{-2}\,\mathrm{A}/\mu\mathrm{m}$ [19] because it is not specified.

III. Results and Discussion

We simulated the Si NS GAA FETs shown in Fig. 1 and measured the effects of VO on them by comparing their static characteristics obtained with the ET model and with the DD model, and then examined how much the VO effects change depending on the application or non-application of the DG model, that is, the presence or absence of QC.

A. VO and QC Effects on Device Performance

Fig. 2 shows the I_D–V_{GS} characteristics of NS FETs with an L_G of 50 nm and T_{NS} of 7 nm at a drain-to-source voltage V_{DS} of 0.65 V. The characteristics obtained when the ET and DG models were applied to electrons in the NSs and source/drain are shown by the solid lines, those obtained with the DD model instead of the ET model by the lines containing dots, and those obtained without the DG model by the lines containing dashes. Comparing the characteristics obtained with the ET model and with the DD model, we see that the ET model produces a larger I_D. This is because the ET model reproduces VO as shown in Fig. 3, where the electron velocity v in the upper NS is plotted in the L_G-direction. The velocity is limited to v_{sat} in the DD model, whereas it exceeds v_{sat} in the ET model. This VO leads to an increase in I_D. Note that, in the ET model, a diffusion current due to the gradient of T flows, which is not considered in the DD model. This current was found to contribute much less to I_D than the drift current and the diffusion current due to the gradient of n. Furthermore, it carried electrons from the hot drain to the cold source and decreased I_D. Therefore, the larger I_D in the ET model than in the DD model is entirely due to VO.

Comparing the I_D–V_{GS} characteristics obtained with and without the DG model, we see that QC decreases I_D. As shown in Fig. 4(a), QC moves electrons away from the surface in an NS, which degrades the effective capacitance of the gate insulating film. Consequently, the number of electrons induced by a given V_{GS} decreases, and I_D also decreases.

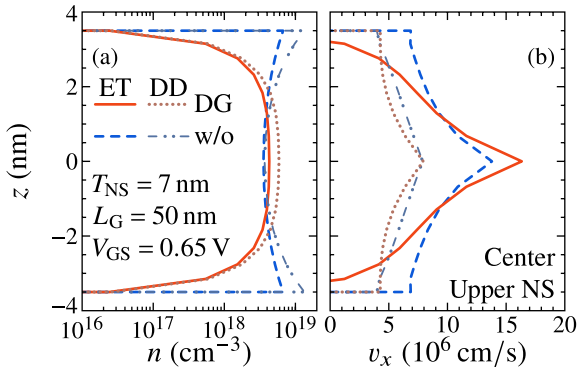

Fig. 4. (a) n and (b) v_x on the center section of the upper NS. Both quantities are averaged over the width and plotted in the T_{NS}-direction. In the averaging of v_x, n is used as a weight.

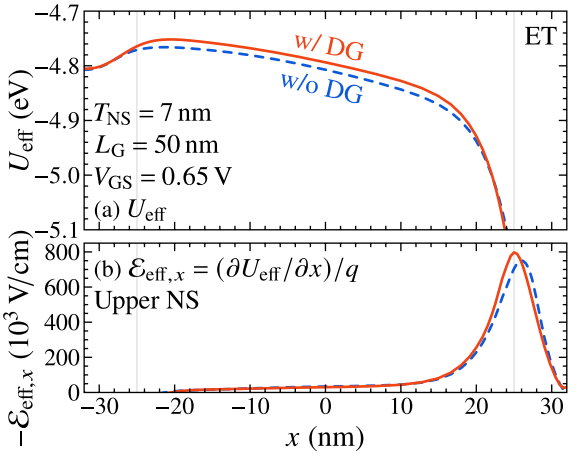

Fig. 5. (a) U_{eff}. (b) $\partial U_{eff}/\partial x$ in terms of the electric field. Both quantities are obtained for the upper NS with the ET model and plotted along the x-axis after being averaged over each section with a weight of n.

B. VO Effect Enhancement by QC

As VO is expected to mitigate the decrease in I_D due to device miniaturization [12], we focused on the ON-state current I_{on} and measured the VO effect on it in terms of the difference between the I_{on}'s obtained with the ET model and with the DD model. As shown in Fig. 2, VO increases I_{on} by 26.5% with QC while by 20.6% without it, which indicates that QC enhances the VO effect. This enhancement is intuitively explained as follows: first, electrons are more accelerated when they are located more inside an NS, as shown in Fig. 4(b), because the lateral field is stronger owing to a weaker influence of the gate, and furthermore the mobility is higher owing to a weaker effect of the surface; second, QC gathers electrons inside the NS. The more precise reason is discussed below.

Fig. 5 shows the L_G-direction profiles of the effective potential U_{eff} and lateral field acting on electrons as obtained for the upper NS with the ET model, where U_{eff} considers U_{QC} and is given by $U_{eff} = E_C + U_{QC}$. In an NS, when electrons are farther away from the surface, U_{eff} is higher and its drop between the NS and the drain is larger, which is of course the case when V_{GS} is higher than the flat-band voltage. In addition, as the gate influence on U_{eff} is weaker, the drain influence extends deeper into the NS. As a result, the lateral field near the drain is stronger in the case with QC than in the case without it.

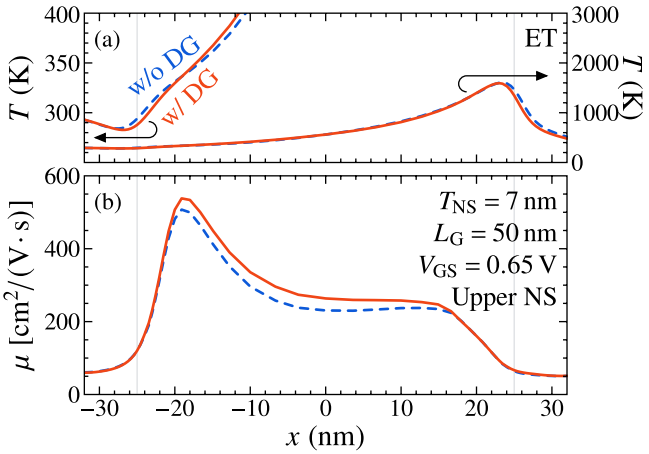

Fig. 6. x-axis profiles of (a) T and (b) μ. Both quantities are obtained for the upper NS with the ET model and averaged over each section with a weight of n.

Furthermore, as electrons move away from the surface, the surface scattering becomes less effective and μ_{low} increases. The final mobility, μ, decreases from μ_{low} with w in the ET model. Overall, there is little difference in w, and hence μ is higher in the case with QC, as shown in Fig. 6. In the figure, w is converted to T according to the relation, $w = (3/2)k_B T$. Before reaching the potential barrier top, in the case with QC, electrons clime a higher barrier and lose more energy, resulting in a lower w. This lowering contributes to the higher μ and to the fact that the v in the case with QC exceeds that in the case without it. Then, as the electrons approach the drain, they are more accelerated by the higher μ and stronger lateral field. As a result, the difference in v between the two cases increases. In the DD model, however, there is no such difference because μ decreases with increasing μ_{low} and $\mathcal{E}_{drv}$, as seen from (5), and besides v is eventually limited to v_{sat}. Therefore, the difference in v observed in the ET model directly related to the difference in the VO effects on device performance, and the relative increase in I_{on} due to VO is higher in the case with QC than in the case without it. A simple explanation for these two points is provided below. First, let us represent the VO effect on I_D by the ratio α of the I_D density obtained with the ET model, $J^{ET} = -qn^{ET}v^{ET}$, to that obtained with the DD model, $J^{DD} = -qn^{DD}v^{DD}$, and next, the α in the case with QC by $\alpha_{QC} = J^{ET}_{QC}/J^{DD}_{QC} = n^{ET}_{QC}v^{ET}_{QC}/n^{DD}_{QC}v^{DD}_{QC}$ and that in the case without QC by $\alpha_0 = J^{ET}_0/J^{DD}_0 = n^{ET}_0 v^{ET}_0/n^{DD}_0 v^{DD}_0$. Then, the ratio of the two α's, $\beta = \alpha_{QC}/\alpha_0$, indicates how much QC affects the VO effect. As $v^{DD}_{QC} \approx v^{DD}_0$, and also $n^{ET}_{QC}/n^{DD}_{QC} \approx n^{ET}_0/n^{DD}_0$ from Fig. 4(a), β can be approximated as $\beta \approx v^{ET}_{QC}/v^{ET}_0$. As discussed above, $v^{ET}_{QC}/v^{ET}_0 > 1$; therefore, $\beta > 1$, that is, QC enhances the VO effect on I_D.

C. L_G, T_{NS}, and V_{GS} Dependences of the Enhancement

As described in Section III-B, QC enhances the VO effects on device performance through the extension of the drain influence on U_{eff} deep into an NS. As L_G becomes shorter, the proportion of the region influenced by the drain in the NS increases, and therefore the enhancement is expected to become larger. Fig. 7 shows I_{on} and its α and β as functions of L_G. As expected, β increases with shortening L_G. However,

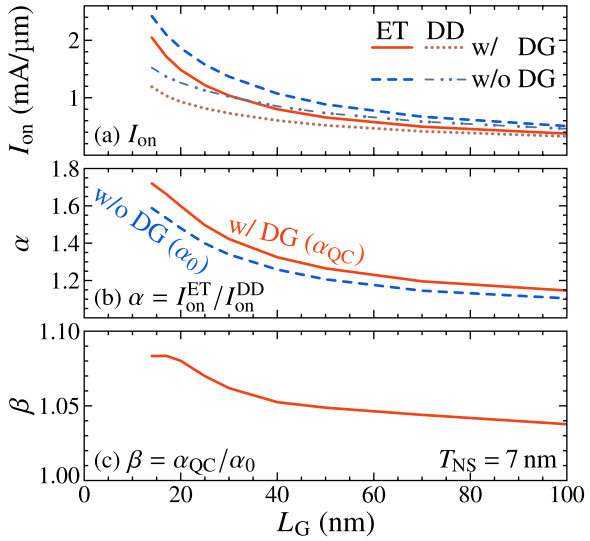

Fig. 7. (a) I_{on} and [(b) and (c)] its α and β as functions of L_G.

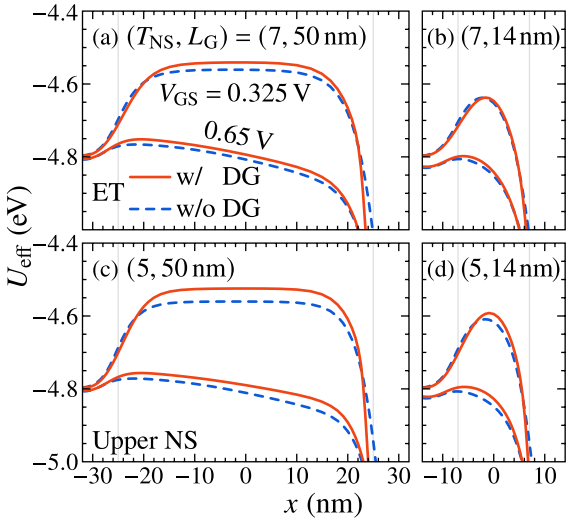

Fig. 8. x-axis profiles of U_{eff} in the upper NS at V_{GS}'s of 0.65 and 0.325 V. The values of U_{eff} are obtained for (T_{NS}, L_G)-pairs of (a) (7, 50 nm), (b) (7, 14 nm), (c) (5, 50 nm), and (d) (5, 14 nm) with the ET model and averaged over each section with a weight of n.

when L_G becomes significantly short, less than 17 nm, β begins to decrease. This is because a rise in U_{eff}, another factor enhancing the VO effects, is suppressed by the extended drain influence, as shown in Fig. 8(b). Fig. 8 shows the L_G-direction profiles of U_{eff} in the upper NS for L_G's of 50 and 14 nm, T_{NS}'s of 7 and 5 nm, and V_{GS}'s of 0.65 and 0.325 V.

We also examined the VO effect enhancement by QC for its dependence on T_{NS}. Fig. 9(a) shows β as a function of L_G for T_{NS}'s of 5 and 10 nm as well as 7 nm. Although QC becomes stronger with thinning T_{NS}, β is lower when T_{NS} is 5 nm than 7 nm. As electrons approach the drain in an NS, their velocity increases, while their number decreases to maintain current continuity. Accordingly, the electrons gather more inside the NS in the case with QC. This is because, if they are close to equilibrium, their population in the ground subband relatively increases, which can be reproduced by the DG model. In reality, however, they would be in non-equilibrium near the drain. It is therefore necessary to verify whether the scattering of them to the ground subband is

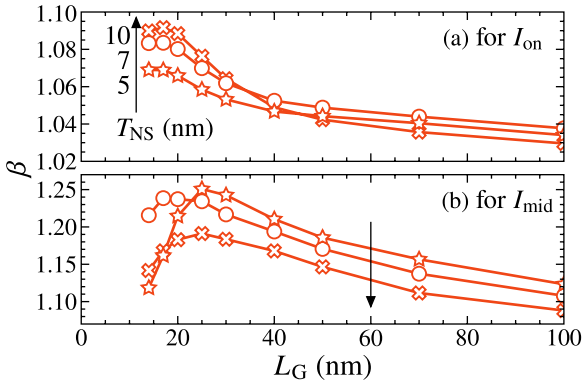

Fig. 9. β's for (a) I_{on} and (b) I_{mid} and for different T_{NS}'s of 5, 7, and 10 nm, plotted as functions of L_G.

sufficient, although optical phonon scattering becomes more frequent as their energy increases. This verification is beyond the scope of this study. For now, let us consider the simulation result that electrons gather more inside an NS as they approach the drain, which acts to raise U_{eff} gradually and weaken the lateral field as opposed to the drain influence extension. When T_{NS} is 5 nm, β is not at its highest because, as shown in Fig. 8(c), this negative contribution is large. When T_{NS} is 10 nm, β is expected to be at its lowest because of the weakest QC. However, the opposite occurs when L_G is short, approximately 30 nm or lower. This is because, as the gate can no longer sufficiently control U_{eff}, the drain influence extended by QC significantly impacts I_{on}.

Finally, we discuss the V_{GS} dependence of the VO effect enhancement by QC. As V_{GS} becomes lower, the electrons in an NS decrease in number, and in the case with QC, they gather more inside the NS. As a result, U_{eff} rises more and its drop near the drain increases more, as seen in Fig. 8(a) and (c). In addition, the extension of the drain influence and the improvement in μ also increase more. Thus, the VO effect enhancement becomes larger. Fig. 9(b) shows the β for the I_D at a V_{DS} of 0.65 V and V_{GS} of 0.325 V, I_{mid}. Comparing this β with the β for I_{on} shown in Fig. 9(a), respectively denoted by β_{mid} and β_{on}, we see that β_{mid} is higher than β_{on}, as expected. Unlike β_{on}, the β_{mid} for a T_{NS} of 5 nm is the highest among the three β_{mid}'s for different T_{NS}'s when L_G is long. This is because, at a V_{GS} of 0.375 V, significantly fewer electrons are present under the gate than at a V_{GS} of 0.65 V. They are gathered sufficiently inside an NS even on the source side, so that a decrease in their number toward the drain does not weaken the lateral field, as shown in Fig. 8(c). However, as L_G shortens from 25 nm, the β_{mid} for a T_{NS} of 5 nm decreases sharply. QC extends not only the drain influence but also the source influence on U_{eff} deep into an NS. The extended source influence moves the potential barrier top toward the drain and shortens the distance over which electrons are accelerated by the lateral field, thereby contributing to a decrease in β at short L_G's. As can be seen from Fig. 8(b) and (d), in the case where T_{NS} is 5 nm and V_{GS} is 0.325 V, as QC basically raises U_{eff} more, the shortening ratio of the acceleration distance is also higher compared with the cases where T_{NS} or V_{GS} is varied. This is the cause of the sharp decrease in the β_{mid} for a T_{NS} of 5 nm. When T_{NS} is 10 nm, β_{mid} does not increase rapidly

at short L_G's, unlike β_{on}. As a lower V_{GS} raises the potential barrier, the enhancement of the electron diffusion flow toward the barrier top by QC, or an increase in μ, is more reflected in β. However, at short L_G's, the extended source and drain influences degrade the QC-induced barrier rise and hence this increase in μ, which slows an increase in β_{mid}. Furthermore, when V_{GS} is low enough for electrons to gather inside an NS even in the case without QC, the trend for β to increase with lowering V_{GS} may change; however, such a change was not observed in the V_{GS} range down to 0 V.

IV. Conclusion

In this study, we performed the device simulation of n-type Si NS GAA FETs while considering VO and QC and investigated how much QC changes the effects of VO on their static characteristics. VO increases the drain current, and QC enhances this increase. This enhancement increases as the gate length becomes shorter, although it eventually begins to decrease. It also generally increases as the gate voltage becomes lower. However, its dependence on the NS thickness is more complex and varies with the gate length and gate voltage. These behaviors of the VO effect enhancement by QC can be fully explained from the effective potential acting on electrons and their mobility in the NS. Furthermore, the gathering of electrons toward the inside of the NS, the most fundamental result of QC, plays a pivotal role in the determination of both these quantities. The findings of this study will be helpful in understanding electron transport in ultrascaled devices, including those other than the NS FETs, and in predicting their performance.

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