A Nanosheet Oxide Semiconductor FET Using ALD InGaOx Channel for 3-D Integrated Devices

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***Abstract*— We have developed atomic layer deposition (ALD) process of InGaOx (IGO) and InSnOx for transistor channel and electrode and investigated the tradeoff among mobility, electrostatics, and reliability in single-gate (SG) IGO FETs. Threshold voltage (V_{th}) shift after positive gate bias was observed especially in high Ga concentration and thin IGO channel devices, which can be attributed to excess oxygen. We also extracted interface and bulk state density (D_{it} and N_{bulk}) using the subthreshold swing (SS) measurement results from the channel thickness dependence. D_{it} is as low as 1–2 $\times$ 10^{11} cm $^{-2}$ eV^{-1}, which means the formation of the defect-less interface between IGO channel and HfO_2 gate dielectric. Ga concentration dependence of N_{bulk} indicates the impact of O_2 dimer generation in high Ga concentration devices. To break the characteristics tradeoff, we fabricated multigate nanosheet (NS) IGO FETs and demonstrated normally OFF operation, high mobility (>30 cm^2/Vs), and high reliability. The drive current of the double-gate (DG) IGO FET is 2.2 times higher and the mobility is 1.2 times higher than that of the SG IGO FET, thanks to the multichannel structure and excess oxygen reduction by passivation process. The difference in positive bias instability (PBI) and negative bias instability (NBI) degradation between SG and DG structure was discussed by comparing the electric field distribution of TCAD simulation results of SG and DG IGO FET. This work shows the most well-balanced performance among preceding ALD IGO FETs with respect to mobility, V_{th}, and SS, and shows the possibility of future 3-D back end of line (BEOL) monolithic and 3-D memory integration using ALD IGO channel.**

***Index Terms*— Atomic layer deposition (ALD), InGaOx (IGO), nanosheet (NS) FET, oxide semiconductor (OS).**

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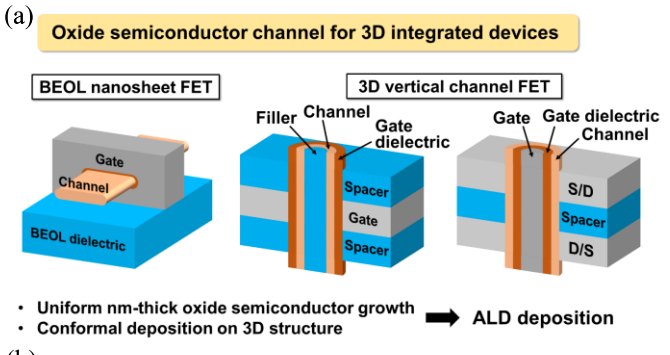
I. Introduction

OXIDE semiconductor (OS) FETs, such as amorphous IGZO FETs, are widely used in current flat panel display (FPD) devices, thanks to their transparency, relatively high mobility, and productivity using sputtering deposition at room temperature [1]. They also have low leakage current and high voltage tolerance derived from wide bandgap, good interfaces with high-k dielectric, and high thermal stability. To take advantage of them, there are some researches applying them to not only FPD devices but also large-scale integration (LSI) devices [2]. And recently, they are attracting more attentions for monolithic 3-D integration in back end of line (BEOL) [3], [4], [5], [6], [7], [8] and 3-D structure memory devices [9], [10] [Fig. 1(a)]. For those applications, nanometer-thick films are needed to be uniformly deposited on complicated 3-D structure. Sputtering is conventionally used for OS material deposition of FPD devices, but it does not meet this requirement. Recently, atomic layer deposition (ALD) has been reported to fulfill the conformal deposition of OS films [11]. The selection of OS channel material is one of the key factors to determine OS FET's performance depending on the applications. Unlike FPD devices, thermal stability is one of the most important challenges for the LSI process. InGaOx (IGO) is a promising candidate of simple ternary compounds for ALD process controllability with high mobility, oxygen dissociation energy, and thermal stability [Fig. 1(b)]. Practical device designs and integration technology of IGO FETs for LSI application have not been reported in detail, though basic material studies on IGO FETs were reported [12]. We also consider that OS electrode such as InSnOx (ITO) is useful for OS FETs because the integration flow introduces oxygen incorporation [7], [8] and ITO electrode can be tolerant to oxidation. The ALD process of OS electrode [13] is also desired for future 3-D integration but not so much featured and reported for integration process yet.

Based on the motivations above, in this study, we develop the ALD IGO and ITO process applicable to 3-D structure, fabricate FETs to systematically investigate device characteristics and tradeoff among mobility, threshold voltage (V_{th}), and reliability, and finally propose and demonstrate a nanosheet (NS) IGO FET targeting normally OFF operation, high mobility, and high bias reliability. This article is an extended version



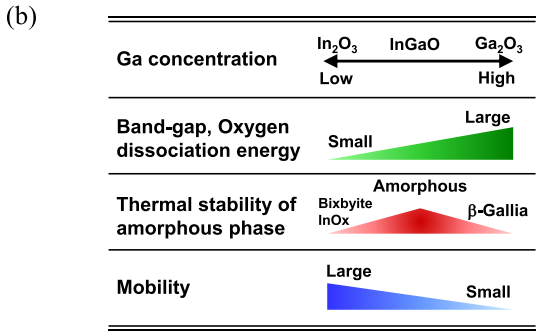


Fig. 1. (a) Schematic of oxide-semiconductor-based 3-D integrated devices: BEOL NS FET and 3-D vertical channel FET. (b) Characteristic trend of IGO with different Ga concentrations: material property, thermal stability, and electron mobility.

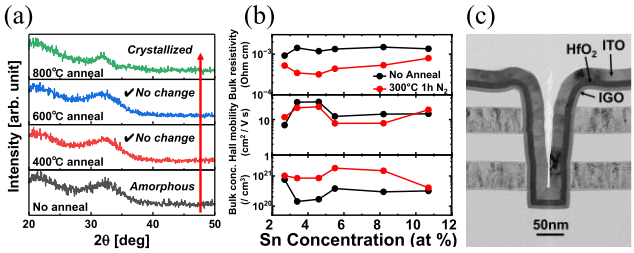


Fig. 2. (a) GI-XRD spectra of 10-nm-thick IGO films on SiO_2 after anneal for 1 h at different temperatures. (b) Hall measurement results of ALD ITO with different Sn concentrations. (c) Cross-sectional TEM image showing conformal deposition of IGO, HfO_2 and ITO on test structure.

of the conference abstract [14] with more detail description and comprehensive data of elemental composition and thickness dependence of bias stress instability, and analysis with the help of TCAD simulation.

II. Device Fabrication

The unit process of IGO and ITO layer deposition was built for the channel and the gate electrode, respectively, using thermal ALD with alkyl-based precursors. Triethyl-indium, triethyl-gallium, and tetraethyl-tin with O_3 oxidant were used for the precursors of In_2O_3, Ga_2O_3, and SnO_2.

Fig. 2(a) shows GI-XRD spectra of the deposited ALD IGO films. It shows only halo pattern up to 600 °C. This indicates that the ALD IGO layer is kept as amorphous above 400 °C which is acceptable process temperature for BEOL. Fig. 2(b) shows Hall measurement results of the deposited ALD ITO films. It is highly conductive and the result shows minimum resistivity of 300 $\mu\Omega$-cm at 5% Sn concentration. We created a test trench structure and deposited IGO and ITO film [Fig. 2(c)]. Conformal deposition of each layer was confirmed.

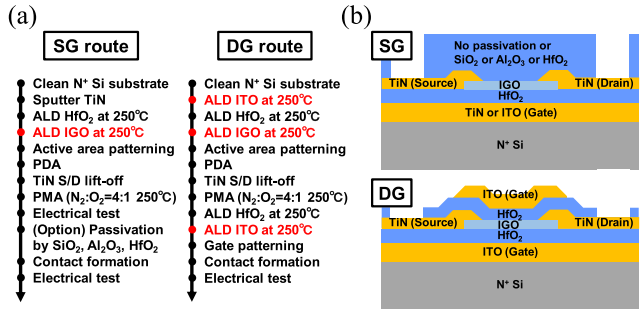


Fig. 3. (a) Device fabrication process flow of fabricated devices and (b) cross section schematics. SG FETs are fabricated with BG, while DG FETs are fabricated with TG and BG. IGO and ITO are deposited by the ALD process with O_3.

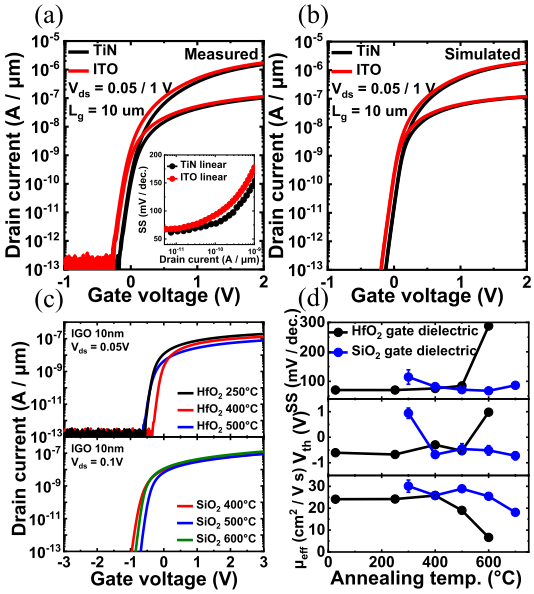


Fig. 4. (a) Measured I_d–V_g curves of the fabricated SG IGO FET with TiN and ITO gate electrode. The inset shows SS versus I_d. (b) Simulated I_d–V_g curves of TCAD simulation. (c) Measured I_d–V_g curves of SG IGO FETs with HfO_2 and SiO_2 gate oxide. IGO was annealed at different temperatures. (d) SS, V_{th}, and μ_{eff} of SG IGO FETs with HfO_2 and SiO_2 gate oxide as a function of IGO anneal temperature.

Afterward, we fabricated: 1) single-gate (SG) IGO FET and 2) double-gate (DG) IGO FET, as a proof-of-concept of NS FET in our university laboratory by following the process flow, shown in Fig. 3(a). Fig. 3(b) shows the cross section schematics of SG and DG IGO FET. The depositions of IGO, ITO, and HfO_2 were performed at the same temperature of 250 °C. Post deposition annealing (PDA) and post metallization annealing (PMA) were performed at 300 °C and 250 °C in air, for an hour each. SG IGO FET has a bottom gate (BG) structure. DG IGO FET has a gate dielectric and a gate electrode on both the top and bottom sides of the device.

III. Results and Discussions

Before systematic studies of IGO FETs, we checked gate electrode differences between TiN and ALD ITO gate. Fig. 4(a) shows the drain current (I_d)–gate voltage (V_g) curves of IGO FETs with TiN and ITO gate fabricated by our baseline process, and Fig. 4(b) shows the TCAD simulation results. Both the results of TiN and ITO gate show good subthreshold characteristics. V_{th} difference mainly derives from the work function of the gate electrodes. The work function of a typical

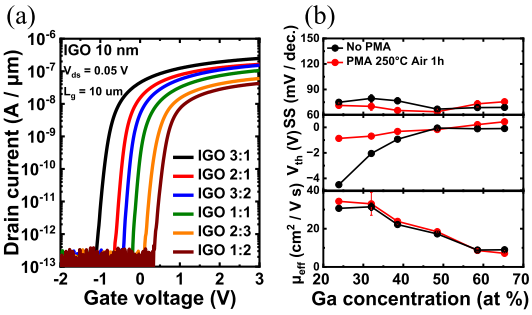


Fig. 5. (a) Measured I_d–V_g curves of the fabricated SG IGO FETs with different Ga concentrations for the 10-nm-thick IGO channel. (b) SS, V_{th}, and μ_{eff} of SG IGO FETs as a function of different Ga concentrations with and without PMA.

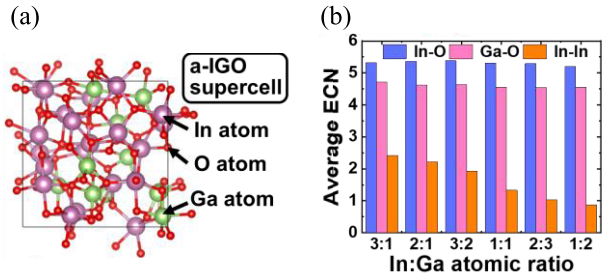


Fig. 6. (a) Schematic of an amorphous-IGO (a-IGO) supercell and (b) simulated ECN of In–O, Ga–O, and In–In for different In:Ga ratios.

ITO is 4.3 eV and lower than that of TiN from [15] and [16], and the TCAD simulation results reproduce the measurement results by adjusting the parameter of gate work function of TiN and ITO with the difference in 0.1 eV.

A. SG IGO FET and Characteristics Tradeoff

First, we studied thermal stability by checking PDA temperature dependence. Fig. 4(b) shows the I_d–V_g curves with different PDA temperatures, and Fig. 4(c) summarizes the electrical characteristics. The electrical characteristics of the IGO FETs are maintained up to 500 °C, above which our thick HfO_2 gate oxide is crystallized and it becomes difficult to precisely evaluate the characteristics. To eliminate the impact of gate oxide crystallization, we also used SiO_2 gate oxide for IGO FETs and confirmed that the performance of the FETs was maintained up to 600 °C, which is consistent with the thermal stability of the IGO films in Fig. 2(a).

Second, we studied Ga concentration dependence to obtain optimal Ga composition for the IGO channel. Fig. 5(a) shows the I_d–V_g curves with different Ga concentrations, and Fig. 5(b) summarizes the electrical characteristics. As Ga concentration increases, we can clearly see V_{th} increase and the decrease in effective mobility (μ_{eff}) while subthreshold swing (SS) is almost maintained. PMA helps annihilate oxygen vacancies (V_o), reduces donor concentration, and thus increases V_{th}. Note that the measurement results of the fifth V_g sweep are shown for these I_d–V_g curves.

InOx is a highly conductive material and a source of high carrier concentration and high mobility, while Ga added in InOx matrix hampers carrier conduction [17], [18]. To survey the effect of Ga on carrier conduction, we performed ab initio molecular dynamic simulation (AIMD) for amorphous-IGO supercells using Quantum ATK simulation and checked effective coordination number (ECN) of In–O, Ga–O, and In–In as

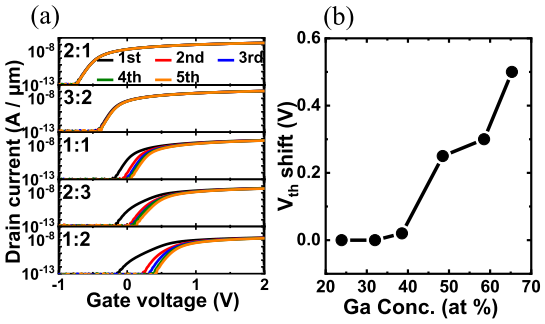


Fig. 7. (a) Measured I_d–V_g curves of the fabricated SG IGO FETs with the 10-nm-thick IGO and different Ga concentrations by five consecutive V_g sweeps. (b) V_{th} shift of the fabricated SG IGO FETs with different Ga concentrations extracted from (a).

shown in Fig. 6(a) and (b). Amorphous oxide structures were generated using first principles MD liquid quench simulations. Modeling the crystal structure was based on a bixbyite space group Ia-3 structure of bulk In_2O_3 with the conventional 80 atom unit cell. For IGO, In atoms were randomly substituted with a specific number of Ga atoms. The unit cell was then structurally optimized for positions and volume until reaching the lowest energy structure. The optimized structure was then heated up from 0 to 5500 K for 1 fs and subsequently maintained at 5500 K for another 1 fs. The structure was rapidly quenched to 300 K with a cooling time of 100 fs followed by temperature equilibrium at 300 K for another 100 fs to obtain the representative ensemble. The canonical NVT (constant number, volume, and temperature) constraint was used. The generalized gradient approximation of Perdew–Burke–Ernzerhof (GGA-PBE) based on projected augmented wave (PAW) was used as an exchange correlational functional. The cutoff energy for plane wave basis of 75 Hartree was used with the Brillouin zone integration sampled by 4 × 4 × 4 k-point mesh which was used for AMID simulations. The structural optimizations were carried out when the Hellmann–Feynman forces used on each atom became less than 0.05 eV/Å. The coordination number is a measure of the number of neighboring atoms or ions with which a central atom is bonded. ECN is calculated for every metal atom by assigning weight to each bond with respect to the shortest M–O bond in the given MO polyhedron [19], [20]

$$\mathrm{ECN} = \sum_i \exp\left(1 - \left(\frac{l_i}{l_{\mathrm{av}}}\right)^6\right) \tag{1}$$

where l_{av} and l_i denote the average pair-correlation function between M–O and M–O distance in the ith MO polyhedron, respectively. We confirmed undercoordinated In–O and Ga–O. In particular, ECN of In–In decreases as Ga concentration increases. This indicates that Ga prevents In s-orbital overlap and decreases mobility, which is consistent with Fig. 5(b).

Fig. 7(a) shows the I_d–V_g curves with different Ga concentrations by five consecutive V_g sweeps, and Fig. 7(b) summarizes V_{th} shift (ΔV_{th}) of Fig. 7(a). As Ga concentration of IGO channel increases, positive ΔV_{th} after positive bias stress increases. This ΔV_{th} is recoverable like positive bias temperature instability (PBTI) and would cause reliability issues. We chose the ALD cycle ratio of In:Ga = 3:2 and

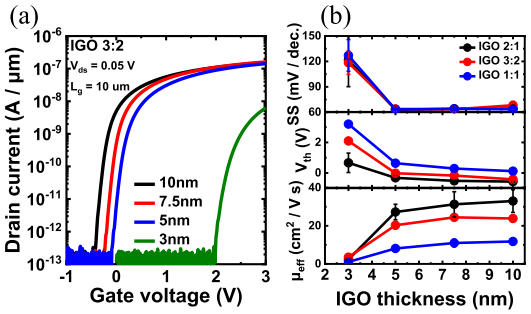


Fig. 8. (a) Measured I_d–V_g curves of the fabricated SG IGO FETs with different IGO thicknesses for In:Ga = 3:2. (b) SS, V_{th}, μ_{eff} of the fabricated SG IGO FETs with different IGO thicknesses for In:Ga = 2:1, 3:2, 1:1.

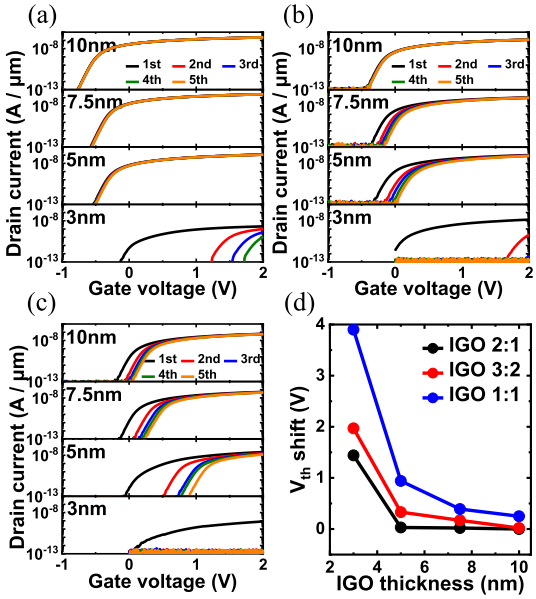


Fig. 9. Measured I_d–V_g curves of the fabricated SG IGO FETs with different IGO thicknesses for (a) In:Ga = 2:1, (b) In:Ga = 3:2, and (c) In:Ga = 1:1. (d) V_{th} shift of the fabricated SG IGO FETs extracted from (a) to (c).

the atomic ratio of $In_{0.61}Ga_{0.39}Ox$, which is well-balanced for device design.

Third, we studied IGO thickness dependence of V_{th}, targeting normally OFF operation and investigating thickness scalability. Fig. 8(a) shows the I_d–V_g curves with different thicknesses, and Fig. 8(b) summarizes the electrical characteristics. As IGO thickness decreases, V_{th} increases, while SS and mobility are maintained above 3-nm-thick IGO. Note that these I_d–V_g curves are taken after the fifth V_g sweep. Fig. 9(a)–(c) shows the I_d–V_g curves with different thicknesses by five consecutive V_g sweeps for In:Ga = 2:1, 3:2, and 1:1, respectively. Fig. 9(d)summarizes ΔV_{th} from Fig. 9(a) to (c). As IGO thickness decreases, the amount of positive ΔV_{th} after multiple V_g sweeps increases. The thinner the IGO thickness, the larger the ΔV_{th}. This instability appears similar to Fig. 7(a) and (b). We concluded that IGO thickness of the 5–7.5-nm range is a choice for controlling short-channel effect in scaled devices while maintaining IGO channel properties.

V_{th} instability in high Ga concentration and very thin IGO FETs can be explained by excess (interstitial) oxygen [21], [22] due to the ALD O_3 process and ambient air exposure with the annealing process as shown in Fig. 10(a).

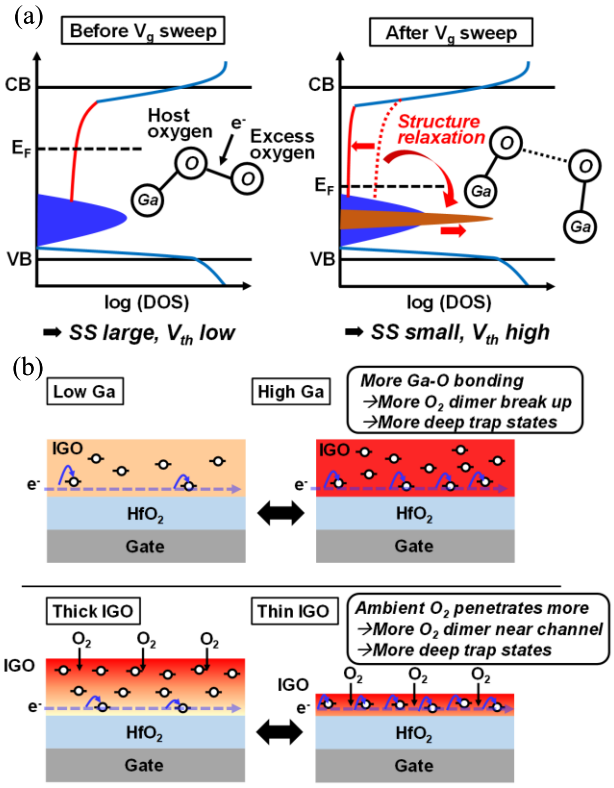


Fig. 10. Schematic of (a) effect of excess (interstitial) oxygen on gap state formation and V_{th} instability for (b) high Ga concentration and thin IGO channel devices based on [21] and [22].

Those oxygen atoms form O_2 dimer which generates shallow gap states near the conduction band. Thereby, V_{th} is low but SS is large for the first V_g sweep. After several V_g sweeps, the dimer is broken by trapping carrier electrons and the shallow gap states are converted into deep gap states by structure relaxation. This makes V_{th} high and SS small. In the case of high Ga concentration, ΔV_{th} becomes larger because Ga is strongly bonded to oxygen and more oxygen dimers are generated and broken into Ga–O bonds. In the case of thin-film IGO, since ambient oxygen can easily penetrate into the channel region and more oxygen dimers are formed near the interface of channel and gate insulator, ΔV_{th} also becomes larger as shown in Fig. 10(b).

We extracted interface state density (D_{it}) and bulk state density (N_{bulk}) from thickness dependence of SS in Fig. 11(a) and the following simplified equation of SS for thin-film transistors [23]

$$SS = \frac{k_B T \ln(10)}{q}\left(1 + \frac{q^2(N_{bulk} t_{ch} + D_{it})}{C_{ox}}\right) \quad (2)$$

where k_B, T, q, t_{ch}, and C_{ox} denote Boltzmann's constant, absolute temperature, electronic charge, channel thickness, and oxide capacitance per unit area, respectively. Note that measurements were performed after multiple V_g sweeps. Fig. 11(b) shows that D_{it} value is as low as 1–2 × 10^{11} $cm^{-2}eV^{-1}$, which indicates the benefit of OS FETs with oxide–oxide interface for high-k gate dielectric, comparing to Si FETs with high-k gate dielectric. D_{it} value is not largely dependent of Ga concentration and PMA. N_{bulk} is lower for higher Ga concentration, which can be explained by the break of more

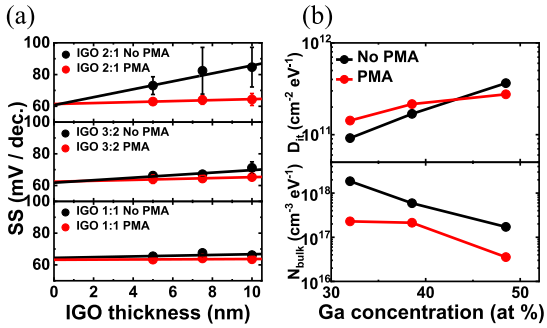


Fig. 11. (a) SS of the fabricated SG IGO FETs as a function of IGO thickness for different Ga concentrations of In:Ga = 2:1, 3:2, 1:1 and (b) derived D_{it} and N_{bulk} from the intercept and slope of (a), with and without PMA.

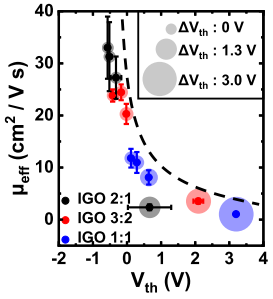


Fig. 12. Tradeoff of μ_{eff}, V_{th}, and V_{th} shift (ΔV_{th}) in SG IGO FETs with different Ga concentrations and IGO thicknesses.

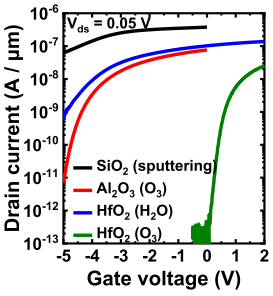


Fig. 13. Measured I_d–V_g curves of the fabricated SG IGO FETs with different passivation layers: SiO_2, Al_2O_3 and HfO_2 (with H_2O and O_3).

oxygen dimers and lower DOS in the upper half of band gap after multiple V_g sweeps. PMA improves N_{bulk} for all Ga concentrations because V_o is annihilated by air annealing.

Finally, Fig. 12 summarizes μ_{eff} versus V_{th} as well as ΔV_{th} for all Ga concentrations and thicknesses of IGO FETs. It shows clear tradeoff between μ_{eff} and V_{th} for SG IGO FETs. This tradeoff needs to be overcome for achieving both high mobility and normally OFF operation by process optimization and device structure design.

B. DG NS IGO FET

To break the tradeoff from the aspect of device design, we considered multigate NS IGO FETs.

First, we conducted a comparative study on passivation effect of top gate (TG) insulator on IGO FET to determine the best passivation layer material and condition. Fig. 13 shows the I_d–V_g curves of different passivation materials and conditions: sputtered SiO_2, ALD Al_2O_3 with O_3 as an oxidant, HfO_2 with H_2O as an oxidant, and HfO_2 with O_3 as an oxidant. In the case of sputtered SiO_2 and Al_2O_3, V_o is formed in the IGO layer because SiO_2 and Al_2O_3 absorb oxygen from IGO,

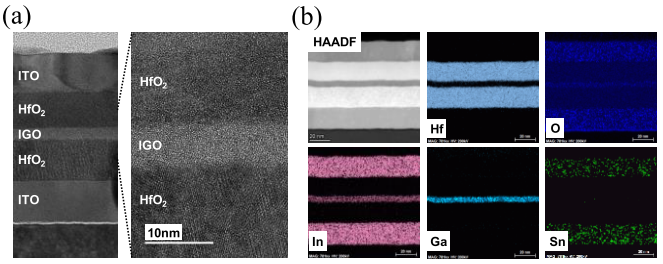


Fig. 14. (a) Cross-sectional TEM images and (b) EDX mapping of the DG IGO FET.

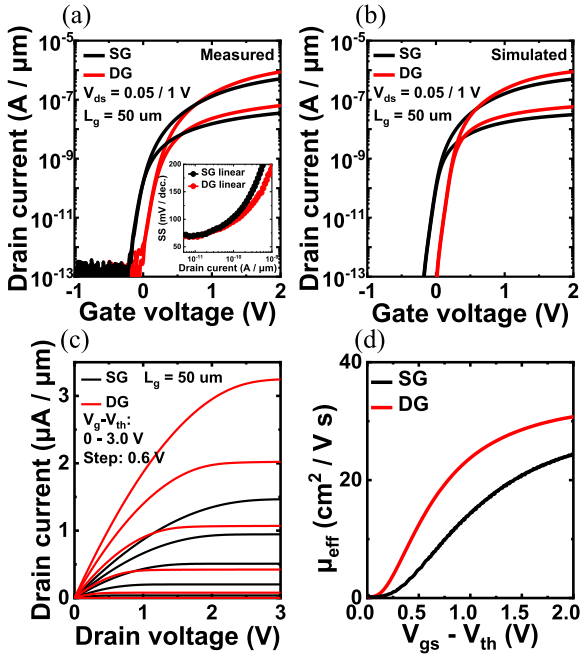


Fig. 15. (a) Measured and (b) simulated I_d–V_g curves of the DG NS IGO FET compared with the SG IGO FET. The inset is I_d–SS. (c) Measured I_d–V_d curves of the DG NS IGO FET compared with the SG IGO FET. (d) Extracted μ_{eff} of the fabricated SG and DG NS IGO FET.

which makes carrier concentration in the channel region high. Thus, V_{th} becomes significantly negative. In the case of HfO_2 with H_2O, H_2O induces hydrogen in the IGO channel layer and makes carrier concentration high. This also results in negative V_{th} shift after passivation. When HfO_2 is deposited with O_3, there is no change in V_{th} before and after passivation. This is possibly because in situ N_2 anneal in vacuum desorbs excess oxygen before HfO_2 deposition, and O_3 oxidant process does not introduce much hydrogen. We determine to use ALD HfO_2 with O_3 for the TG insulator and the bottom one.

Second, Fig. 14 shows the cross-sectional TEM images and the corresponding EDX mapping of the fabricated DG NS FET with 7-nm-thick IGO channel and ITO gate. Layers are uniformly deposited and sharp interfaces without interdiffusion are confirmed. Fig. 15(a) shows the I_d–V_g curves of the SG and DG NS FET, and Fig. 15(b) shows the TCAD simulation results. The simulation results were able to reproduce the measurement results. The DG NS FET shows normally OFF operation because TG and BG need to pinch off only half of the IGO thickness. It also shows twice higher drive current in linear region operation compared with the SG FET, thanks to multichannel conduction. The I_d–V_d curves and μ_{eff} are shown in Fig. 15(c) and (d). The DG NS IGO FET shows 2.2 times

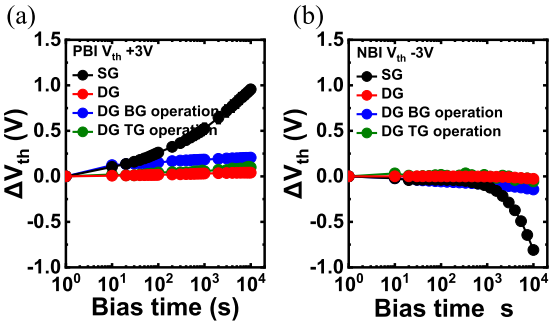


Fig. 16. (a) PBI and (b) NBI characteristics of the fabricated SG and DG IGO FETs. Blue (green) line represents the only BG (TG) operation of the fabricated DG NS IGO FET.

higher drive current and 1.2 times higher mobility of over 30 cm^2/Vs than the SG IGO FET. The mobility improvement can be due to defect reduction by good passivation of the IGO layer with DG structure.

Third, we checked the bias stress reliability of IGO FETs. Fig. 16(a) and (b) shows ΔV_{th} under positive and negative bias stresses for the SG FET, which does not have any passivation layers, and the DG NS FET. The values of the stress V_g are $V_{th} + 3$ V for positive bias and $V_{th} - 3$ V for negative bias. The total bias time is set for 10k s, and the source and drain are grounded during the gate stress. We measured positive bias instability (PBI) and negative bias instability (NBI) in four conditions: SG device, DG device with the same bias voltage applied from both TG and BG, DG device with the bias voltage applied only from the BG, and DG device with the bias voltage applied only from the TG. Note that when DG devices are operated only by one side gate, the other side gate is floating. All the measurements were conducted at room temperature without light. Both the bias stabilities are significantly improved using the DG NS structure. This improvement can also be attributed to the excess oxygen reduction by in situ N_2 anneal before top HfO_2 gate dielectric deposition and defect reduction by good passivation with the DG NS structure. Moreover, electric field reduction by DG operation may also help for reducing ΔV_{th}.

To study the contribution of electric field reduction by DG structure, we conducted TCAD simulation and checked electric field distribution of SG and DG. Fig. 17(a) and (b) shows the electric field in the simulated SG and DG FETs under PBI and NBI bias conditions. Enlarged views inside the IGO and near the bottom interface under PBI bias condition are shown in Fig. 17(c) and (d). In the PBI bias condition, we can find that the electric field was almost the same in the SG and DG FETs except that there is a small difference inside the IGO layer. This may suggest that excess oxygen suppression and passivation can be the main reason for PBI improvement in DG NS FET. In the NBI condition, we can clearly see the electric field reduction at the HfO_2/IGO interface and inside the IGO layer for the DG NS FET. This results in the less formation of V_o and ionized oxygen vacancies (V_O^+ and V_O^{2+}) which act as shallow donor state near the conduction band and smaller negative ΔV_{th} [24].

Finally, we demonstrated the most well-balanced performance among the reported ALD IGO FETs in terms of

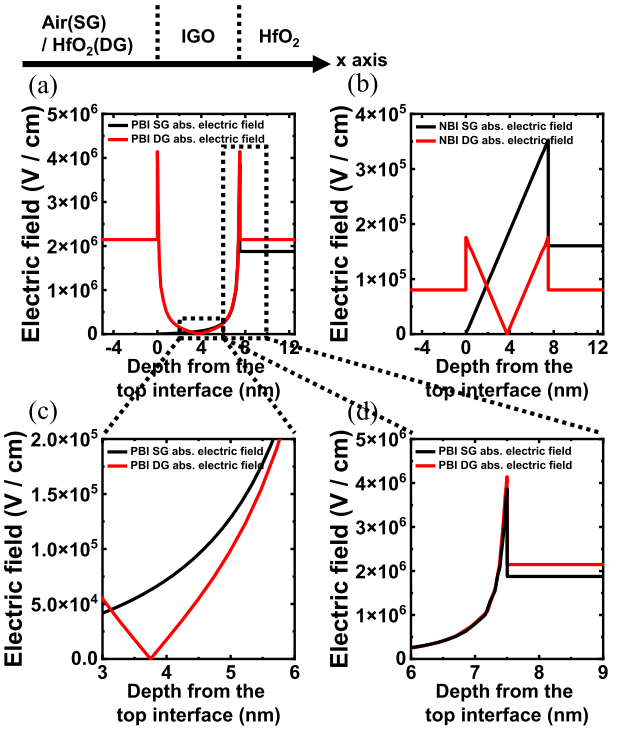


Fig. 17. TCAD simulation results of electric field distribution under (a) PBI ($V_{th} + 3$ V) and (b) NBI ($V_{th} - 3$ V) bias conditions. Enlarged views (c) inside the IGO channel and (d) near the bottom IGO/HfO_2 interface. The top interface between IGO and air (SG) /HfO_2 (DG) is set for the origin of x-axis.

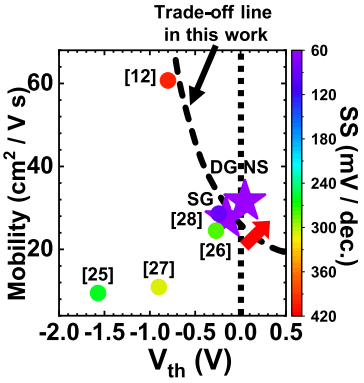


Fig. 18. Benchmark of ALD-deposited IGO channel FETs for mobility and V_{th}, as well as SS. Our DG NS FET outperforms and breaks the tradeoff.

mobility, V_{th}, and SS and made the benchmark as shown in Fig. 18 [12], [25], [26], [27], [28].

IV. Conclusion

We developed unit process of ALD InGaOx and InSnOx deposition for channel and electrode and investigated the tradeoff among mobility, electrostatics, and reliability in SG IGO FETs. ΔV_{th} after positive V_g sweep was observed for high Ga concentration and thin IGO thickness, which can be attributed to the excess oxygen. We also extracted D_{it} and N_{bulk} using thickness dependence of SS. We obtained low D_{it}, which means the formation of defect-less interface between the IGO channel and HfO_2 gate dielectric. Ga concentration dependence of N_{bulk} can be related to the formation and structure relaxation of O_2 dimer by excess oxygen. To break

the tradeoff among mobility, electrostatics, and reliability, we demonstrated DG NS IGO FETs and achieved normally OFF operation, high mobility, and high reliability. The PBI and NBI are improved using DG structure and good surface passivation. The differences in PBI and NBI between SG and DG structure were discussed by comparing the electric field of the TCAD simulation results. This work shows the most well-balanced performance among preceding ALD IGO FETs with respect to mobility, V_{th}, and SS, and provides the possibility of future 3-D BEOL monolithic and 3-D memory devices using ALD IGO channel.

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