Lagging Thermal Annealing for Barrier Height Uniformity Evolution of Ni/4H-SiC Schottky Contacts

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***Abstract*— The electrical behavior improvement of nonuniform Ni/4H-SiC Schottky diodes, akin to that caused by thermal annealing, is demonstrated after continuous exposure to high operating temperatures (400 °C). After only the standard rapid thermal annealing (RTA), samples with different contact diameters exhibit barrier height and ideality factor fluctuations, typical for nonuniform contacts. After 2 h at 400 °C, a shift in Schottky barrier is observed, toward a plateau of 1.63 V, constant with temperature and bias, for all investigated structures, with current flow being nearly fully accounted for by single-barrier thermionic emission. Coupled with operational contact area enhancement, this lagging treatment ensures the devices' ability to operate at high temperatures.**

***Index Terms*— Barrier height, high-temperature operation, Schottky diode, silicon carbide (SiC), thermal annealing.**

I. Introduction

IN INDUSTRIAL applications, where control of vital processes occurring over vast temperature spans is normal, silicon carbide (SiC) Schottky diodes should be very appealing, due to their versatile uses and performances in both switching and sensing. The wide bandgap of SiC enables the fabrication of Schottky diodes with elevated barrier height (such as with Ni/SiC contacts), which allows them to maintain good rectifying properties and exponential current–voltage ($I-V$) dependence over temperature ranges far exceeding Si. However, current commercial SiC diodes still generally exhibit restricted safe temperature limits under 175 °C [1], [2]. This ceiling is considerably lower than the proven capabilities of even such SiC devices and can be traced back to two primary reasons: packaging cost and contact inhomogeneity. While the first roadblock can be justifiably overcome for applications, which demand such harsh working environments [3], [4], the issue of contact inhomogeneity affects device performances [5], [6], [7] in terms of both electrical behavior and reliability, hindering commercial introduction even to this day.

The thermal annealing of metal–semiconductor contacts represents a crucial, intensely researched step toward obtaining high-quality interfaces and eliminating unwanted, localized defects [1], [5], [8], [9], [10], [11], [12]. The essentially used process of rapid thermal annealing (RTA) was shown to improve the performances of SiC-Schottky contacts [6], [7]. The effects of RTA temperature on the metal-SiC Schottky contact electrical properties have been under investigation for more than 20 years [5], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22]. These briefs sometimes report differing results despite identical annealing temperatures—they can be attributed to other significant process factors, such as surface preparation before Schottky metal deposition [23]. In spite of this, clear trends still emerge for the effects of treatment temperature on Schottky contact characteristics.

Higher annealing temperatures (500 °C–850 °C) lead to the formation of silicides (which act as Schottky metals), with improved contact adherence and reduced series resistance [14], [17], [18]. Furthermore, barrier height is increased [6], [7], [13], [14], [16], [17], [21], [22], enabling operation at higher temperatures. Other parameters, such as the reverse leakage current [16], [17], [21] and the breakdown voltage [16] are also improved. However, such treatments exacerbate existing contact inhomogeneity or even generate it [5], [13], [14], [20], [22].

Lower annealing temperatures (<500 °C) were shown to lead to better Schottky contact uniformity [5], [13], [14], [20], [22]. Based on the abovementioned, in this brief, we propose a simple method for improving SiC Schottky diode parameter stability and reliability by using a tandem between

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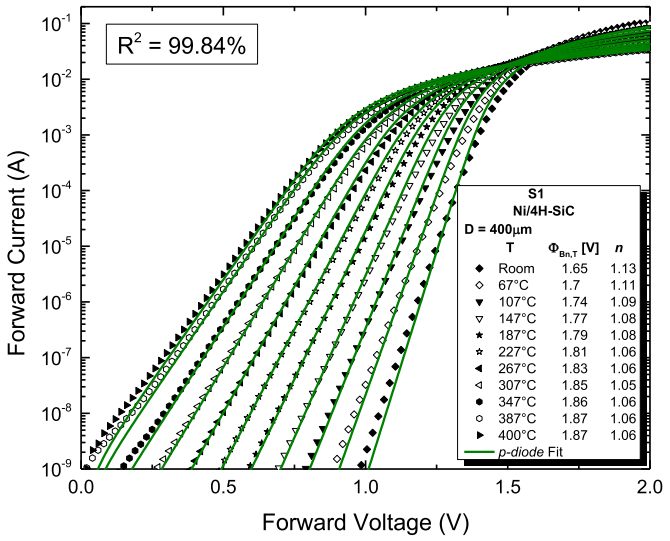

Fig. 1. Forward characteristics of a post-RTA, only, Ni/4H-SiC Schottky diode with 400 μm diameter.

fast, high-temperature annealing (RTA) and a lagging thermal annealing (LTA), performed over a longer time span, at temperatures close to the devices' intended maximum. A significant enhancement in Schottky barrier uniformity and extension of effective current-conducting area are evinced.

II. Sample Preparation

Experimental Schottky diodes were fabricated on n-type 4H-SiC wafers with 8-μm epitaxial layer and approx. 10^{16}cm^{-3} doping density. Initially, a field oxide (500 nm thickness) was deposited by low-pressure chemical vapor deposition at 750 °C. Using standard photolithography, circular windows with different diameters (200, 300, and 400 μm) were defined on the wafer frontside. When the backside oxide was completely removed, an ohmic contact was formed after a successive metallic deposition of Ti (30 nm) and Ni (100 nm), followed by a sintering at 1050 °C, in Ar atmosphere, for 3 min. During this process, the front-side windows were shielded from impurities by a very thin sacrificial oxide layer. The Schottky contacts were obtained following Ni deposition (100 nm) on the wafer frontside and subsequent 3-min RTA at 750 °C in inert atmosphere (Ar). The test samples were packaged in TO39 capsules [3] using the wire bonding technology.

III. Results and Discussion

The forward characteristics of post-RTA Schottky samples, having the different contact diameters (S1—400 μm, S2—300 μm, and S3—200 μm), were measured from room temperature to 400 °C using a Keithley 4200 Semiconductor Characterization System together with a Varian Chromatograph oven [7]. All devices exhibited exponential $I-V$ characteristics over at least six orders of magnitude across the entire domain, as exemplified in Fig. 1 (symbols), for S1. In consequence, such diodes should be suitable for adequate operation up to 400 °C.

TABLE I
Conventional Parameters

Sample	Contact diameter [μm]	Average $\Phi_{Bn,T}$ [V]	ε_Φ [%]	Average n	ε_n [%]	R_S [Ω]
S1	400	1.79	12.2	1.08	7.7	4.1 – 25.8
S2	300	1.76	5.9	1.04	5.6	2.6 – 9.1
S3	200	1.75	5	1.05	4.9	3.3 – 16.4

First, a standard analysis and parameter extraction were performed, based on the ideal thermionic emission equation [5], [6], [7], [24], [25]

$$I_F = A_n A_S T^2 \exp\left(\frac{-\Phi_{Bn,T}}{V_{th}}\right)\left[\exp\left(\frac{V_F - R_S I_F}{n V_{th}}\right) - 1\right] \quad (1)$$

where A_n is Richardson's constant (146 A·cm^{-2}·K^{-2} for 4H-SiC [6]), A_S is the nominal contact area, T is the absolute temperature, V_{Th} is its associated thermal voltage, n is the ideality factor, and R_S is the series resistance. $\Phi_{Bn,T}$ represents the conventional Schottky barrier height, specific to measurements at a single temperature, assuming that current flows uniformly through the nominal contact surface (A_S) [25]. $\Phi_{Bn,T}$ and n temperature dependences for S1 are shown in Fig. 1 legend. Significant fluctuations with temperature is evinced, indicating that the contacts are, in fact, nonuniform, despite relatively low ideality factor values [24], [25]. The average values for $\Phi_{Bn,T}$, n (and the R_S intervals) are given in Table I for all samples. Here, ε_Φ and ε_n are the barrier and ideality factor relative deviations, calculated as their overall temperature variation with respect to the average.

In order to assess the degree of inhomogeneity, our p-diode model was employed, according to which the current flow through a real Schottky contact is given by [6], [7]

$$I_F = A_n A_S T^2 \sum_{i=1}^{m} \exp\left(\frac{-\Phi_{Bn,i}}{V_{th}} - p_{eff,i}\right) \times \left[\exp\left(\frac{V_F - R_{S,i} I_{F,i}}{n V_{th}}\right) - 1\right]. \quad (2)$$

The sum in (2) signifies that the total current is composed of multiple contributions coming from m separate Schottky regions on the contact surface, according to the parallel-conduction concept [25]. Each region, acting as a *parallel diode*, has a specific barrier height ($\Phi_{Bn,i}$), independent of temperature, a series resistance ($R_{S,i}$), and nonuniformity parameter ($p_{eff,i}$), which gives a quantitative indication of occupied area. High $p_{eff,i}$ values correspond to small zones, which still significantly influence current value.

The measured samples were parameterized according to this model, with results given in Table II. All *parallel diodes* are considered to have a quasi-unitary ideality factor ($n = 1.03$) to account for just image-force lowering and avoid parameter redundancy. Values for the coefficients of determination (R^2) are also included, indicating the matching degree between model-calculated curves [using (2)] and measured data. First, $m = 1$, for all samples, is considered, in order to determine whether current flow is dictated by a single region. In the case of S2 and S3, the good R^2 value attests to this approach. The

TABLE II
INITIAL *p-diode* PARAMETERS

Sample	Parallel -diodes	Φ_{Bn} [V]	n	p_{eff}	R_S [Ω]	R^2 [%]
S1	Single	1.67	1.03	3.89	5.7 – 27	99.84
S2	Single	1.72		1.31	3.1 – 8.9	99.97
S3	Single	1.73		0.96	4 – 16.1	99.92
S1	Dp1.1	1.9		0.01	4.3 – 27	99.94
	Dp1.2	1.63		5.71		
	Dp1.3	1.59		6.42	~5k	

p-diode model parameters indicate that these samples have relatively stable barrier heights throughout the entire investigated temperature range, although the effective conductive area is smaller than the nominal one ($p_{\text{eff}} \neq 0$).

When modeling S1 with $m = 1$, the lower R^2 values indicate that more than one diode influences current conduction throughout the temperature domain. Indeed, comparing model calculated curves (lines—Fig. 1) with experimental data (symbols—Fig. 1), a visible discrepancy is evinced both in the low and the high bias regions, especially at lower temperatures. Consequently, S1 requires modeling with multiple parallel diodes (Dp1.1–Dp1.3—Table II). An improvement in fitting accuracy was achieved (see R^2 increase—Table II). It can be seen that, eventhough Dp1.1 occupies nearly the entire contact area (p_{eff}, $1 \cong 0$), there are two other regions, with much smaller surfaces ($p_{\text{eff},2,3} > 5.5$), which also contribute to current flow. Indeed, real Schottky contacts are more likely to exhibit nonuniform behavior as their surface increases, as current is exponentially influenced by barrier height and only linearly by area. Thus, even small-surface defect occurrences can affect electrical behavior, as is the case for S1.

Note that series resistances in Tables I and II were conventionally extracted from measurements at high bias (V_F over 1.5 V), giving values in the order of ohms. They generally represent lumped contributions from multiple sources (drift layer, substrate, ohmic contact, packaging, measurement setup, etc.) Exceptionally, in the case of S1 modeling with three *parallel diodes*, the series resistance extraction is not as trivial. Thus, at high bias levels, both Dp1.1 and Dp1.2 contribute comparable currents, making the deconvolution of R_S values impossible (Table II gives the result for the equivalent parallel grouping). The series resistance afferent to Dp1.3 was estimated in order to enhance fitting accuracy. Its high value shunts the parallel-diode's contribution after a certain bias level, enabling Dp1.1 and Dp1.2 to overtake conduction for S1.

In order to assess Schottky parameter stability and reproducibility up to the limit operating temperature for such SiC diodes, the samples were subsequently kept at 400 °C, in ambient atmosphere, for over 3 h, with their forward characteristics being acquired every 15 min. The variations in conventional barrier height ($\Phi_{Bn,T}$) and ideality factor were determined and are plotted in Fig. 2.

After roughly 1 h, a significant shift in $\Phi_{Bn,T}$ is observed, which dampens after a further 60 min for S1 and 120 min for samples S2 and S3. Ideality factors vary very slightly during this time, with values close to the one selected in

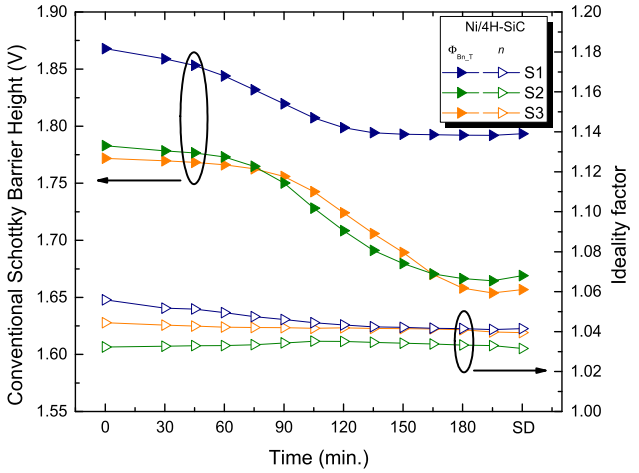

Fig. 2. Conventional barrier height and ideality factor evolution for the three samples subjected to 400 °C for over 3 h.

TABLE III
POST-LTA *p-diode* PARAMETERS

Sample	Parallel -diodes	Φ_{Bn} [V]	n	p_{eff}	R_S [Ω]	R^2 [%]
S1	Single	1.63	1.03	2.77	4.6 – 27	99.99
S2	Single	1.63		0.58	2.6 – 9.9	99.99
S3	Single	1.64		0.34	3.4 – 17.6	> 99.99

Table II. This behavior is typical during annealing processes. The forward characteristics of S1–S3 were reacquired on a separate day. Barrier and ideality factor determinations at 400 °C are also given in Fig. 2 (denoted by SD). Also, the post-LTA measured forward curves were modeled with the *p-diode* technique. Model parameters are given in Table III. They remarkably indicate a noticeable improvement in contact quality. Thus, real barrier heights have become unitary and stable with temperature and bias across the devices, indicating that the same contact composition is dominant. The post-LTA inhomogeneity drop was strongly confirmed by both a significant reduction in p_{eff} (indicating that the effective conduction area was substantially expanded) and a near perfect fit ($R^2 > 99.99\%$) between measured curves and pure thermionic emission (modeling with a single diode, only, see Table III). Under these circumstances, the reduction in barrier height value (to approx. 1.63 V) is expected, in order to ensure current conduction through this larger effective area.

This excellent agreement between measured data and *p-diode* model fitted curves is evinced in Fig. 3, for S1. A comparison between pre (red) and post (green)-LTA forward characteristics is, also, given in Fig. 3 inset. The clear fitting improvement is also observable by contrasting Figs. 1 and 3. This device is no longer influenced by three separate regions on its Schottky contact surface, but rather a single such zone dictates current flow, associated with Dp1.2 (Table II). For this parallel diode, the effective area was expanded, as indicated in Table III. However, in contrast with S2 and S3, the p_{eff} value of S1 still shows that the treatment did not manage to make the contact entirely uniform.

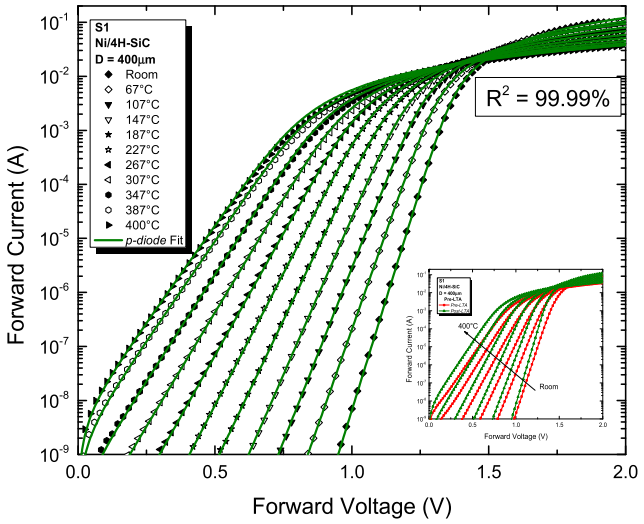

Fig. 3. Forward characteristics of post-LTA Ni/4H-SiC Schottky diode with 400 μm diameter (symbols), alongside *p*-diode model fitted curves (lines).

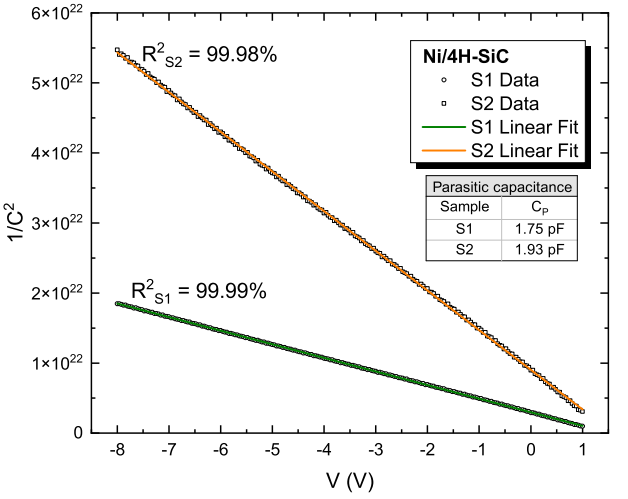

Fig. 4. Adjusted $1/C^2$ curves of post-LTA Ni/4H-SiC Schottky diodes with 400 and 300 μm diameter (symbols), alongside linear fitting (lines).

For Samples S1 and S2, Schottky barrier heights were also evaluated from $C-V$ characteristics. Measurements were acquired in a dc range (-8 V$\cdots$1 V) and at a small signal (10-mV and 10-MHz frequency). The presence of parasitic capacitances (C_p, such as from our high-temperature capable packaging, bonding, and wires) significantly impacted the linearity of the $1/C^2(V)$ plot, leading to $\Phi_{\mathrm{Bn},C\text{-}V}$ bias dependence. In order to alleviate this effect, this parasitic value was subtracted from measured data. C_p was iteratively tuned, starting from the measured equivalent wire and package capacitances, until the $1/C^2$ (V) curves reached a peak linearity (given by R^2). Resulting plots are depicted in Fig. 4.

Following a linear fitting over the entire measurement interval, the barrier height was extracted from the X-axis intercept [25]. Thus, $\Phi_{\mathrm{Bn},C\text{-}V}$ values of 1.76 and 1.82 V were obtained for S1 and S2, respectively. As expected, these $C-V$ barrier heights are larger than those determined from $I-V$ forward measurements. Doping levels, obtained from the slope of the linear fit, were close to the epitaxial layer's nominal concentration. It should be noted, however, that, even with the linearization, $\Phi_{\mathrm{Bn},C\text{-}V}$ values are still somewhat dependent on bias interval. Furthermore, the knowledge of precise contact area is also required to correctly determine this parameter. As such, the $\Phi_{\mathrm{Bn,C-V}}$ values given above should be taken as indicative rather than exact. Conversely, the barrier determinations from $I-V$ characteristics give a much higher degree of confidence, as the accurate fitting of forward curves leaves little room for error (Φ_{Bn} has exponential impact on calculated I_F values).

IV. Conclusion

This brief showed that what should be tolerable operating conditions for Ni/4H-SiC Schottky diodes can lead to significant contact quality shifts. Alongside the RTA at high temperature (750 °C), the samples also suffered a lagging thermal annealing, during prolonged exposure, for some hours, to 400 °C. This LTA improved the uniformity of Schottky barrier height, making it nearly independent of temperature and bias. Additionally, it enhanced the operational contact area, nearing its nominal designed value (A_S). Thus, for SiC-devices meant to work above conventional temperature limits (175 °C), the well-known high-heat sintering processes, accompanied by LTA, can lead to a significant temperature operation extension, toward 400 °C for high-barrier Schottky diodes. This threshold is subject to changes for other Schottky metals, primarily limited by the devices' Φ_{Bn} operational value.

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