Characterization and Advanced Modeling of Dielectric Defects in Low-Thermal Budget RMG MOSFETs Using 1/*f* Noise Analysis

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***Abstract*— This study presents a comprehensive investigation of defects in the gate-stack of low-thermal budget replacement metal gate (RMG) MOSFETs treated with novel dielectric passivation techniques using 1/*f* noise characterization and advanced modeling. This research demonstrates that MOSFETs with gate-stacks treated with atomic hydrogen (H*) and oxygen (O*) ($T < 450$ °C) yield 1/*f* noise levels comparable to those of high-thermal budget devices. We also demonstrate that the noise of both pMOSFETs and nMOSFETs mainly originates from defects in the SiO_2 interfacial layer (IL). In addition, accurate modeling of 1/*f* noise provides useful insights into the dielectric defect densities before and after passivation. Notably, the contribution of O-vacancies in HfO_2 to 1/*f* noise appears negligible, whereas it is very important for positive bias temperature instabilities (PBTIs). The results confirm the effectiveness of H* and O* treatments in reducing the electrically active dielectric defects while contributing to a better understanding of the underlying passivation mechanisms.**

***Index Terms*— 1/*f* noise, characterization, complementary field-effect transistor (CFET), replacement metal gate (RMG), sequential 3-D.**

I. Introduction

THE introduction of 3-D stacking techniques for MOSFETs is envisioned in the CMOS scaling roadmap to enable higher device density and improved functionality within the area footprint [1], [2], [3]. Two integration schemes are mainly used for high-κ/metal gate-stacks: gate-first (often referred to as MIPS, "metal-inserted poly-Si") and gate-last (also called RMG, "replacement metal gate") [4]. The terminologies "first" and "last" refer to whether the gate electrode is deposited before or after the high-temperature S/D doping activation anneal(s) of the flow. Focusing on the RMG process, two main alternatives are possible for 3-D stacking: sequential [5], [6] and monolithic [7] integration. In sequential 3-D integration, a fresh slab of Si is attached by oxide-to-oxide bonding on top of a bottom device tier to fabricate a top device tier with nanometric alignment to the bottom counterpart. In such scheme, the top-tier device needs to be fabricated at a reduced thermal budget (typically max $T < 550$ °C) to preserve the integrity of the bottom device. Conventionally, high-temperature anneals are performed to passivate dielectric defects [8]; these high-T processes are not compatible with top tier fabrication, posing concerns over the reliability and noise of the device. Moreover, gate-stacks with a reduced thermal budget would be beneficial also for complementary field-effect transistor (CFET) monolithic integration [7], since in this integration flow the contacts of the bottom device are already in place during the RMG flow and their performance might degrade at higher temperatures.

To solve this issue, novel dielectric passivation techniques involving hydrogen (H*) and oxygen (O*) radicals at low-thermal budgets ($T < 450$ °C) have been recently proposed [9], [10]. These techniques have shown BTI reliability in line with devices fabricated with high-thermal budget processes. However, the noise of these low-thermal budget devices has not been experimentally evaluated so far.

In this article, we characterize and model the defects in low-thermal budget RMG MOSFETs through 1/*f* noise experiments and exploit advanced noise models for the interpretation of the results. This analysis further proves the ability of the H* and O* treatments to passivate dielectric defects and gives additional physical insights into the defects involved in the passivation. This article proceeds as follows: Section II introduces the measurement setup and the devices considered in this study. Section III shows the measurement results and the main implications. Section IV describes the interpretation of the experimental data with comprehensive models

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TABLE I
PARAMETERS OF THE DEVICES CONSIDERED IN THIS ARTICLE

Device	eWF [eV]	EOT [nm]	T_{IL} [nm]	ε_{IL}	T_{HK} [nm]	ε_{HK}
pMOS as dep.	4.81	0.97	1.12	6.6	1.9	24
pMOS mild H*	4.91	0.93	1.11	6.0	1.3	24
pMOS H*	4.97	1.12	1.10	4.7	1.3	24
pMOS H*-O*	4.90	1.37	1.28	4.7	1.9	24
pMOS PDA	4.92	1.13	1.32	6.25	1.9	24
nMOS as dep.	4.32	0.87	0.95	6.6	1.9	24
nMOS H*	4.43	1.01	0.96	4.7	1.3	24
nMOS O*	4.27	1.25	1.59	6.6	1.9	24
nMOS H*-O*	4.26	1.41	1.44	4.7	1.3	24
nMOS PDA	4.56[1]	1.16	1.36	6.25	1.9	24

of $1/f$ noise providing insights on the defect passivations. Finally, the concluding Section V summarizes the main results.

II. MEASUREMENT SETUP AND DEVICES

We considered planar nMOSFETs and pMOSFETs with $W = L = 1$ μm, SiO_2/HfO_2 as gate dielectrics, and Ti-based metal gates. The source and drain of these test devices consist of highly doped Si regions without any strain booster technology. The devices have been fabricated with the same RMG process but different annealing techniques and thermal budgets, as listed in Table I. In particular, atomic hydrogen (H*) anneals of the SiO_2 interfacial layer (IL) and atomic oxygen (O*) anneals of the high-κ dielectric (HK) [11] are compared and combined. The values of equivalent oxide thickness (EOT) and effective work function (eWF) in Table I are obtained by calibrating a Schrödinger–Poisson solver to the experimental C–V curves [12], [13] (not shown here).

For the pMOS, we measured devices with low-thermal budget processes without any annealing (i.e., as-deposited), treated with "mild" H* (where the exposure to atomic hydrogen has been limited to avoid excessive EOT increase related to the desorption of OH-groups from the IL [9]), treated with H*, or with both H* and O*. The same goes for the nMOSFETs, where an O*-only case replaces the case with "mild" H* of the pMOSFET. In addition, we measured both nMOSFETs and pMOSFETs devices treated with a high-temperature postdeposition anneal (PDA) at 850 °C (done after the high-κ dielectric deposition and before the gate metal deposition) to have a direct comparison with devices with standard high-thermal budget processing. Apart from this latter case, all the other gate-stacks have a maximum process temperature of 450 °C, in line with 3-D integration requirements.

All the pMOSFETs use the same p-work function metal (WFM, TiN), while the nMOSFETs use an n-WFM based on TiAl, except for the nMOSFET subject to high-T PDA, which uses a midgap WFM [resulting in slightly higher V_T; see Fig. 1(a)]. The midgap WFM is obtained by modifying the thickness of the bottom TiN and TiAl metal layers in the n-WFM gate metal stack in line with industry practice [14]. The eWF values are reported in Table I. Note that each annealing scheme induces some eWF changes, as discussed in [9] and [10], due to the passivation of "fixed" charge in the dielectrics; nevertheless, the pMOS and nMOS V_Ts remain in a range compatible with CMOS integration requirements in all the cases (Fig. 1).

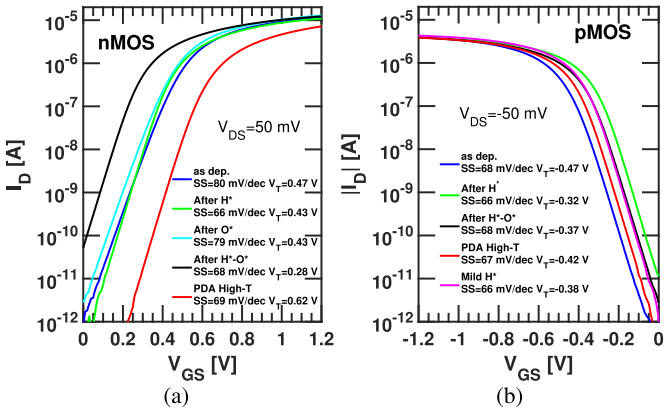

Fig. 1. I_D versus V_{GS} for (a) nMOSFETs and (b) pMOSFETs with the parameters of Table I and $|V_{DS}| = 50$ mV.

All the devices were subject to a conventional sintering anneal at the end of the fabrication flow, at 420 °C for 20 min in forming gas.

We used a Keithley B1500 and a Keysight low-frequency noise analyzer to perform the dc and noise characterization at a controlled temperature of 25 °C. Moreover, we kept the drain voltage ($|V_{DS}|$) equal to 50 mV during the noise measurements to bias the devices in the linear regime.

III. MEASUREMENTS AND DISCUSSION

This section presents the experimental results, beginning with the I-V measurements, followed by the characterization with $1/f$ noise.

A. I–V Curves

Fig. 1 shows comparison of $I_D - V_{GS}$ at $|V_{DS}| = 50$ mV for both the nMOSFETs (a) and the pMOSFETs (b) described in Table I. The threshold voltage V_T is extrapolated from the linear $I_D - V_{GS}$ curve at the point of maximum transconductance [15], while the SS is extracted by taking the median value of SS in the 0.1–100-nA drain current range. Extensive performance and reliability assessment of these devices, including the I_{ON} and I_{OFF} values, can be found in [11].

For the nMOS, we note that the low-temperature H* treatment improves the subthreshold swing (SS) with respect to the "as-deposited" case, reaching a value of 66 mV/dec that is in line with the PDA device with a high-thermal budget. This suggests that the H* treatment passivates defects that affect the SS of the "as-deposited" devices. The threshold voltage shifts between nMOSFETs with different treatments are mostly attributed to the changes in EOT (see Table I), variation in trapped charge inside the dielectrics after passivation, and, for the nMOSFET with PDA, the different gate metal work function.

When looking at the pMOSFETs, the low-thermal budget devices have SS values in line with the high-thermal budget PDA device. Moreover, we do not observe significant changes in the SS with the treatments. This suggests that low-thermal budget dielectrics do not have a sufficient number of defects in the energy range that can be probed by monitoring the subthreshold swing variation in pMOSFETs [16], especially

considering the limited SS sensitivity to defects in gate-stacks with extremely scaled EOTs. However, we note that the H* treatment introduces a threshold voltage shift with respect to the as-deposited case. This is ascribed to the passivation of defects in the SiO_2 interlayer reducing the fixed charge in the dielectric [9]. In addition, there is a component of threshold voltage shift related to the change in EOT and the introduction of the O* treatment. Nevertheless, the threshold voltages after H* and O* treatments are in a range that is compatible with CMOS technology requirements.

B. 1/f Noise

We now evaluate the effect of the various passivation treatments on the drain current noise of the device. To interpret the measured power spectral density, we consider the well-known expression for the input-referred drain current noise [17]

$$S_{vg} = \frac{S_{id}}{g_m^2} = \frac{qkTN_{BT}}{WLC_{ox}^2\alpha}\frac{1}{f}\left(1+\alpha_{sc}\mu_{\text{eff}}C_{ox}\frac{I_D}{g_m}\right)^2 \quad (1)$$

where S_{id} is the power spectral density of the drain current noise, g_m is the transconductance, μ_{eff} is the effective mobility, N_{BT} is an effective dielectric trap density per unit volume and unit energy, α is a tunneling coefficient estimated through the Wentzel–Kramers–Brillouin (WKB) approximation, C_{ox} is the effective gate dielectric capacitance per unit area, q is the elementary charge, T is the temperature, f is the frequency and α_{sc} is a parameter related to mobility fluctuations (MF). More accurate and complete models for $1/f$ noise will be used in Section IV.

Equation (1) allows us to discriminate between carrier number fluctuations (CNFs) and MF by looking at the drain current dependence of the S_{vg}. Our analysis will focus only on CNF since MF could be caused not only by dielectric defects [18], [19]. On the other hand, in the CNF theory [18], $1/f$ noise in the drain current is attributed to charge fluctuation in dielectric traps. Therefore, the analysis of $1/f$ noise in the CNF region is a powerful tool to evaluate the quality of dielectrics and to monitor their degradation/improvement after stress/treatments.

Fig. 2 shows comparison of the measured S_{vg} spectra of nMOS (a) and pMOS (b) devices with different annealing techniques at $V_{GS} - V_T = V_{ov} = 0$ V. The noise spectra follow a $1/f$ dependence and do not show any white noise contribution, which could originate from trap-assisted tunneling (TAT) leakage current in the gate flowing toward the drain or thermal noise. Moreover, the noise of the devices treated with the low-thermal budget H*–O* treatments is comparable to the one with high-temperature PDA and significantly lower than the devices with the dielectrics "as-deposited." Note that S_{vg} also has a strong dependence on C_{ox} [see (1)]. Thus, the noise reduction observed in Fig. 2 appears smaller than the actual reduction in the trap densities N_{BT} derived from (1), primarily due to minor variations in the EOT of the devices.

The $1/f$ noise in the CNFs regime ($\alpha_{sc}\mu_{\text{eff}}C_{ox}I_D/g_m \ll 1$) is proportional to the effective trap density N_{BT} inside the dielectrics

$$N_{BT} = S_{vg}\frac{WLC_{ox}^2\alpha f}{\text{qkT}}. \quad (2)$$

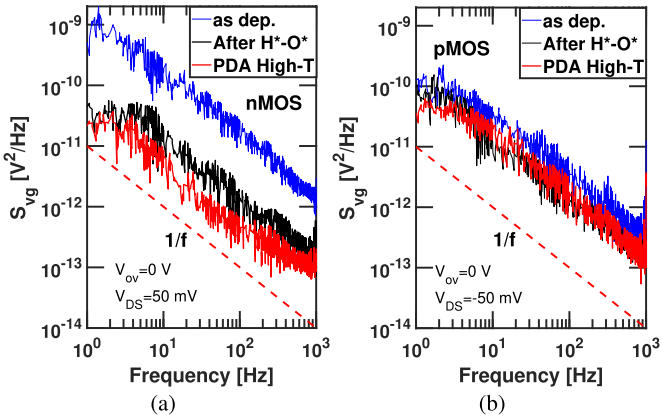

Fig. 2. S_{vg} versus frequency for (a) nMOSFETs and (b) pMOSFETs with dielectrics "as-deposited," treated with H*–O*, or treated with high-temperature PDA at $V_{ov} = 0$ V and $|V_{DS}| = 50$ mV.

This quantity represents an effective trap density since it does not take into account the spatial sensitivity of noise to the dielectric trap fluctuations and the trapping/detrapping events involving the gate electrode [20], [21], [22]. However, despite these limitations, S_{vg} in the CNF regime can serve as a monitor of the quality of gate dielectrics, particularly when comparing devices with similar gate-stacks (i.e., same gate metals and as-deposited dielectric thicknesses), as it is in our study. Note that (1) gives no dependence on I_D in the CNF regime if we assume that the distribution of the dielectric traps probed by the noise does not vary much for different biases (i.e., different energy alignment between the Fermi levels of the carrier reservoirs and the dielectric trap energy levels).

To see whether a given bias point falls in the CNF regime, we plot in Fig. 3 $S_{vg} \cdot f$ (which is essentially constant versus frequency since S_{vg} goes as $1/f$) against I_D. For the nMOSFETs, there is a range of bias points where we see almost no dependence on I_D [Fig. 3(a)]. On the other hand, it is difficult to identify such a range of biases for the pMOSFETs [Fig. 3(b)]. However, we note that S_{vg} curves tend to flatten out going toward the points at low currents. In the following, we will use the data at the lowest currents in Fig. 3 (which correspond to $V_{ov} = 0$ V) to extract an effective N_{BT} with (2), assuming the devices operate in the CNF regime.

Note that the increase in S_{vg} with drain current has been extensively observed [23] and it can be fit with an $\alpha_{sc}\mu_{\text{eff}}$ coefficient of about $\approx 10^6$ cm^2/C, consistently with [23]. However, there is a strong debate on the underlying cause of noise in this region, and it could be due not only to dielectric traps [18], [19]. For this reason, we are not extracting N_{BT} from the noise points falling in this region.

The N_{BT} values extracted with (2) at $V_{ov} = 0$ V (the points at lowest current in Fig. 3) are presented in Fig. 4 for both nMOSFETs and pMOSFETs with the different annealing treatments of Table I. The effective N_{BT} for both nMOS and pMOS is significantly reduced with the introduction of the H* low-thermal budget treatment (approximately 27x for the nMOS and 4x for the pMOS) and essentially unaffected when O* is also inserted (although a 4x reduction can be observed in the nMOS case with O* treatment alone). Since

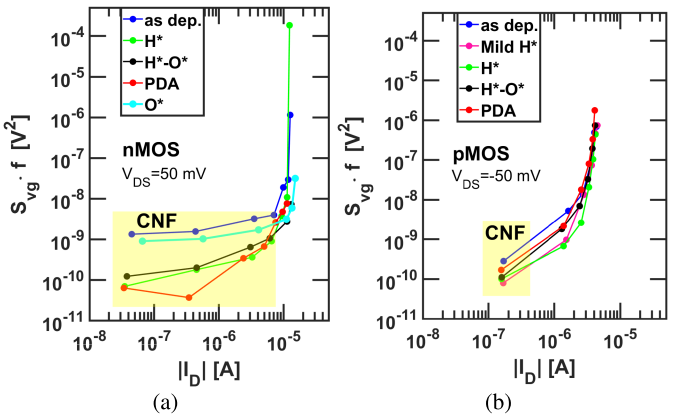

Fig. 3. $S_{vg} \cdot f$ versus $|I_D|$ for (a) nMOSFETs and (b) pMOSFETs listed in Table I at $|V_{DS}| = 50$ mV.

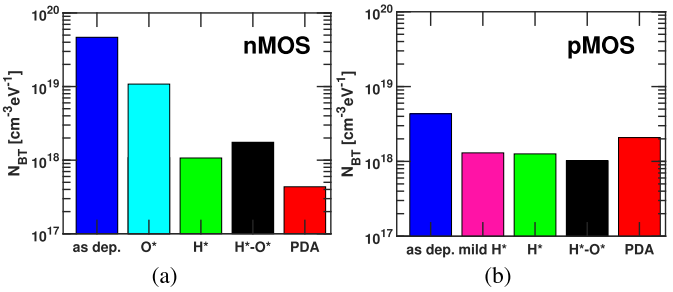

Fig. 4. Equivalent N_{BT} extracted from $1/f$ noise according to (2) versus the different passivation treatments analyzed in this work for (a) nMOSFETs and (b) pMOSFETs.

the H* treatment is applied only on the SiO_2 IL before HKMG deposition, we deduce that the noise in both "as-deposited" nMOS and pMOS is dominated by defects present in the interlayer. This is not surprising for the pMOS since it is expected that the defects in SiO_2 are the main cause for $1/f$ noise [24] and negative bias temperature instabilities (NBTIs) [25]. On the contrary, the noise of nMOS with the standard HKMG stack has been attributed to the O-vacancies in HfO_2 [24] which is also the main cause of positive bias temperature instabilities (PBTIs) [26]. Instead, this study shows that the main cause for $1/f$ noise in nMOSFETs with *low-thermal budget* are the defects in SiO_2, as it is for pMOSFETs.

Fig. 5 shows plots of the equivalent N_{BT} extracted through $1/f$ noise measurements using (2) against the EOT for all the devices in Table I. Fig. 5 reports also the results for reference metal-inserted poly-Si (MIPS) stack (also known as *gate first*) devices with the highest possible thermal budget (note that in this legacy integration scheme, the final gate-stack is fabricated before the S/D implants, and therefore, it is exposed to the doping activation anneal at T in the range of 1000–1100 °C). The MIPS have the best results in terms of scaled EOT and low N_{BT}, as expected [27], since the gate-stack is exposed to an additional high-temperature anneal. However, the low-thermal budget processes with H* give comparable results and even outperform the high-T PDA process. N_{BT} of the combined H*–O* process is very competitive, although the penalty in EOT given by the O* process is large. Further optimization of the process is needed to obtain competitive EOT values.

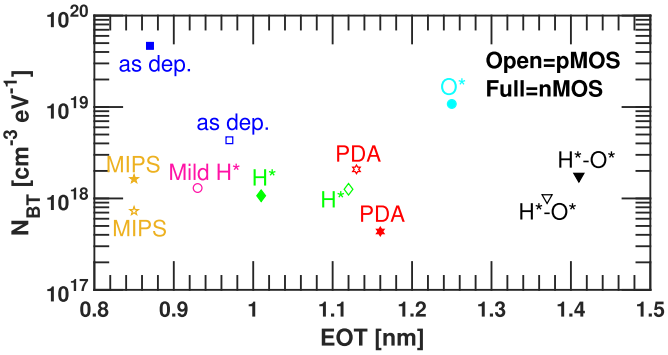

Fig. 5. Equivalent N_{BT} extracted from $1/f$ noise according to (2) versus EOT for the nMOSFETs (full symbols) and pMOSFETs (open symbols) listed in Table I. The stars refer to MIPS stack devices with high-thermal budget process.

IV. Advanced Modeling of Dielectric Defects With $1/f$ Noise

Equation (2), used in the previous section for trap density extraction, is not accurate when applied to thin dielectric gate-stacks. This is due to several approximations, including the neglect of trapping/detrapping events involving the gate metal [20], [21], [22].

In this section, we consider the comprehensive noise model of [20], [21] for S_{vg} to interpret the data and reveal the effect of the low-thermal budget treatments on the defects in the dielectrics. The model implements the complete trapping/de-trapping dynamics for the CNF input-referred drain current noise in MOSFETs biased in the linear region of operation [20], [21]

$$S_{vg} = \frac{q^2}{\mathrm{WLC}_{ox}^2} \iint \frac{4 f_T (1 - f_T)\tau}{1 + (2\pi f \tau)^2} N_{BT} K \, dE_T dz_T \tag{3}$$

where z is the direction perpendicular to the channel, $f_T = f_T(E_T, z_T)$ is the function describing the occupation of the dielectric traps, $\tau = \tau(E_T, z_T)$ is the trapping/detrapping time implemented according to the nonradiative multiphonon (NMP) model [28], $N_{BT} = N_{BT}(E_T, z_T)$ is the dielectric trap density per unit volume and energy, and $K = K(z_T)$ is an electrostatic scaling factor that takes into account the relationship between charges fluctuating in the dielectric and charges fluctuating in the channel [20].

This model can take into account the effect of charge trapping/detrapping with the *gate metal* and the term $K(z_T)$, both very important for thin dielectric gate-stacks [22].

The computation of the trapping/detrapping time τ includes both quantum mechanical tunneling and thermally activated capture/emission processes (see NMP model of [28]). Moreover, it requires information on the alignment between the Fermi levels of the carriers reservoir (channel and gate) with the bands of the dielectrics and the electric field inside the dielectrics. To extract these quantities, we used 2-D TCAD simulations in Synopsys Sdevice [29] of bulk MOSFETs with the density gradient model for the quantization effects and with the technological details of Table I.

The traps' distributions N_{BT} and the relaxation energies used in (3) for SiO_2 and HfO_2 are based on ab initio

calculations [30] and BTI measurements [10], [31]. We use Gaussian distributions in energy to model N_{BT}. Moreover, we consider the traps in HfO_2 uniform in space, while we consider the traps in SiO_2 exponentially decaying starting from the interface with the silicon with a decay length $\sigma_{z_T} = 0.5$ nm. This is done to reproduce the increased number of defects due to the strain at the Si/SiO_2 interface [9]. The expression used for different contributions to N_{BT} is then

$$N_{BT}(E_T, z_T) = N_{BT_0} \exp\left(\frac{-(E_T - \mu_{E_T})^2}{2\sigma_{E_T}^2}\right) \times \exp\left(\frac{-(z_T - z_0)}{\sigma_{z_T}}\right) \quad (4)$$

where $\mu_{E_T}(z)$ is the mean energy of the Gaussian distribution with the midgap of the silicon as a reference at zero band bending, σ_{E_T} is the standard deviation, E_T is the energy of the trap, z_T is the position of the trap, z_0 is the coordinate of the Si/SiO_2 interface, and σ_{z_T} is the exponential decay length in space. In the case of uniform distribution, we have $\sigma_{z_T} \to +\infty$.

According to the measurement results shown in Fig. 4, the noise in both nMOS and pMOS is strongly reduced after H* treatment to the interlayer. This is a strong indication that the dominating defects for $1/f$ noise in the case of dielectrics without any passivation are found in the SiO_2 interlayer. Moreover, we know that the SS of the nMOS is improved with H* treatment, while the SS of the pMOS remains essentially unvaried after the treatments. The variation in SS with different passivation treatments should reflect the variation in near-interface defects with energy going from the midgap to the conduction/valence band.

Following these indications, we inserted two defect bands in SiO_2, one closer to the conduction band and one closer to the valence band with the parameters listed in Table II. The H* treatment reduces the total number of traps in both these defect bands, as shown in Table II and Fig. 6(a). The trap distributions used for SiO_2 shallow and deep traps are in good agreement with the hydroxyl-E' (H-E') defect distributions obtained from ab initio studies [30], which identify the H-E' defect to be more likely present with high concentrations in SiO_2, and its energy distribution could contribute to both NBTI (in pMOS) [10] and $1/f$ noise (in both pMOS and nMOS). An H-E' defect can form in SiO_2 whenever a hydrogen atom attaches to and eventually breaks a strained Si–O bond, forming an hydroxyl group.

For HfO_2, we inserted deep traps that are accessible through the Fermi level of the gate metal with a pWF (therefore, only in the pMOS devices) [31] and an O-vacancies' distribution with a very high concentration based on PBTI model calibrations [10] [see Fig. 6(b)].

The band diagrams of both p-type and n-type MOSFETs with the defect bands of Table II are depicted in Fig. 7. Only traps aligned with the Fermi level of the channel or the gate contribute to $1/f$ noise. Therefore, n-type and p-type MOSFETs are sensitive to different defect bands in the dielectric, and the various passivation treatments will affect their noise in a distinct way. Note that the O-vacancies never contribute to the $1/f$ noise due to energy misalignment with the Fermi levels of the channel and gate metal. The O* treatment should strongly reduce the number of O-vacancies in HfO_2, but this cannot be probed with $1/f$ noise because their energy alignment with the Fermi levels does not allow them to fluctuate during the measurements, not even in the case of dielectrics where only SiO_2 has been passivated. *This is a strong indication that O-vacancies in the HfO_2 (important*

TABLE II

(a) ENERGY DISTRIBUTIONS OF THE DEFECT BANDS IN THE DIELECTRICS. THE SAME ENERGY DISTRIBUTIONS ARE CONSISTENTLY USED TO MODEL THE NOISE RELATIVE TO THE DIFFERENT PASSIVATION TREATMENTS CONSIDERED. ALL ENERGIES ARE REFERRED TO THE SI MIDGAP. NOTE THAT THE DEFECTS IN SiO_2 ARE EXPONENTIALLY DISTRIBUTED IN SPACE WITH THE CENTER AT THE INTERFACE WITH THE CHANNEL AND $\sigma_{z_T} = 0.5$ NM, WHILE THE DEFECTS IN HfO_2 ARE ASSUMED UNIFORM IN SPACE. (b) VALUES OF PEAK TRAP DENSITY N_{BT_0} FOR DIFFERENT TREATMENTS. DIFFERENCES WITH RESPECT TO THE "AS-DEPOSITED" VALUES ARE IN BOLD. NOTE THAT IN THE MODEL THE CONCENTRATION OF O–VACANCIES IN HfO_2 IS NOT VARIED WITH THE TREATMENTS BECAUSE THESE DEFECTS ARE NOT PROBED WITH $1/f$ NOISE SO THE VARIATIONS CANNOT BE ESTIMATED

Defect bands	μ_{E_T} [eV]	σ_{E_T} [eV]
SiO_2 shallow	0.435	0.29
SiO_2 deep	−0.77	0.105
O-vacancies in HfO_2	0.79	0.134
HfO_2 deep	−0.35	0.15

(a)

Treatments	Defect bands	N_{BT} [cm^{-3} eV^{-1}]
"As deposited"	SiO_2 shallow	$1.38 \cdot 10^{20}$
	SiO_2 deep	$3.8 \cdot 10^{20}$
	O-vacancies in HfO_2	$3.2 \cdot 10^{21}$ (not probed by noise)
	HfO_2 deep	$7 \cdot 10^{19}$
H*	**SiO_2 shallow**	$\mathbf{6 \cdot 10^{18}}$
	SiO_2 deep	$\mathbf{1.65 \cdot 10^{19}}$
	O-vacancies in HfO_2	$3.2 \cdot 10^{21}$ (not probed by noise)
	HfO_2 deep	$7 \cdot 10^{19}$
O* treated	**SiO_2 shallow**	$\mathbf{4 \cdot 10^{19}}$
	SiO_2 deep	$3.8 \cdot 10^{20}$
	O-vacancies in HfO_2	$3.2 \cdot 10^{21}$ (not probed by noise)
	HfO_2 deep	$7 \cdot 10^{19}$
H*-O* treated	**SiO_2 shallow**	$\mathbf{6 \cdot 10^{18}}$
	SiO_2 deep	$\mathbf{1.65 \cdot 10^{19}}$
	O-vacancies in HfO_2	$3.2 \cdot 10^{21}$ (not probed by noise)
	HfO_2 deep	$\mathbf{4 \cdot 10^{19}}$
PDA	**SiO_2 shallow**	$\mathbf{1.5 \cdot 10^{19}}$
	SiO_2 deep	$\mathbf{1.65 \cdot 10^{19}}$
	O-vacancies in HfO_2	$3.2 \cdot 10^{21}$ (not probed by noise)
	HfO_2 deep	$\mathbf{4 \cdot 10^{19}}$

(b)

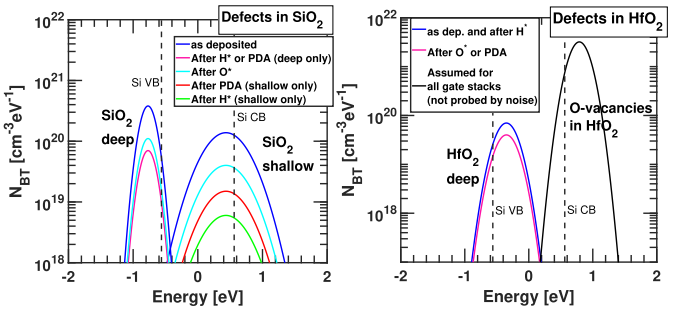

Fig. 6. Plot of the trap energy density distributions N_{BT} in SiO_2 (a) and HfO_2. (b) Energy is referenced to the silicon midgap energy.

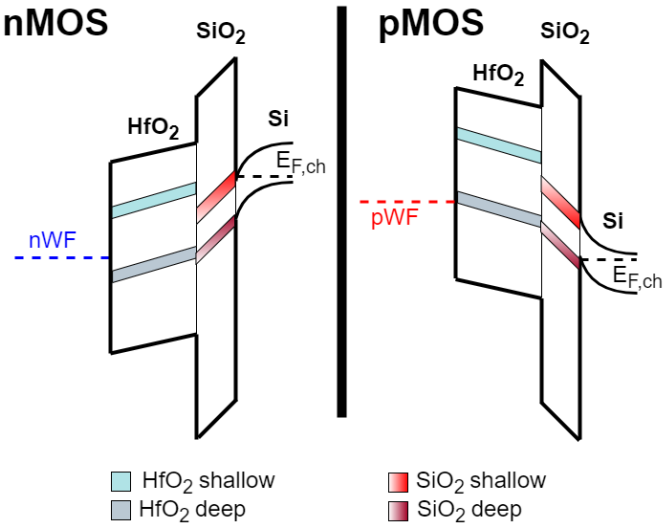

Fig. 7. Sketch of the energy band diagrams of both n-type and p-type MOSFETs with the defect bands of Table II.

for PBTI) are not contributing to 1/f noise in either pMOS or nMOS.

Fig. 8 shows comparison of the predictions of (3) using traps' distributions of Table II to the noise measurements at $V_{ov} = 0$ V. The excellent agreement between (3) and the noise measurements confirms that the proposed defect bands and the reduction in their amplitude with the various treatments assumed in our study are fully consistent with the measured noise spectra.

Note that the noise spectra in Fig. 8 have an uncertainty of a factor 2-3. Therefore, the values in Table II feature similar uncertainties. However, the fitting considers the average value of $S_{vg} \cdot f$ along the measured frequency range. The averaging process over frequency should effectively reduce the uncertainty on the hypothesis that this is equally distributed among points at different frequencies. Moreover, S_{vg} variations observed after applying the passivation treatments are higher than those uncertainties.

The 1/*f* noise of the nMOSFETs after H*–O* or PDA passivation is caused by the residual H-E' defects in the SiO_2. On the other hand, the noise of pMOSFETs after H*–O* or PDA passivation is caused by the deep defect band in HfO_2, because the IL defect density has been suppressed by H* treatment, and the O-vacancy band in HfO_2, passivated by O* anneal, does not contribute to noise. The occupation of deep

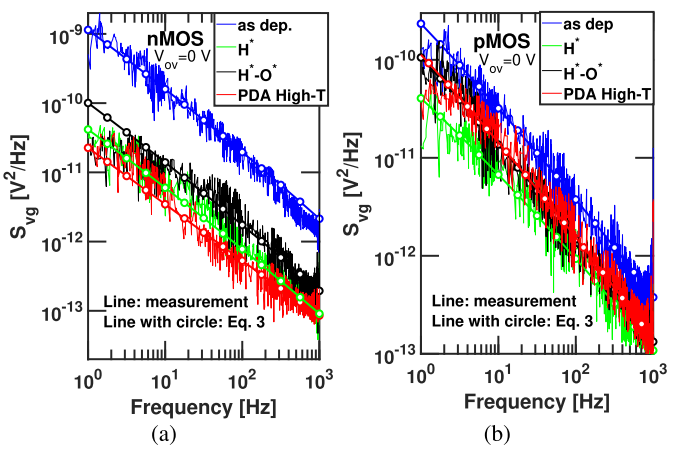

Fig. 8. Comparison between S_{vg} predicted by (3) with the trap distributions of Table II against measurements at $V_{ov} = 0$ V for (a) nMOSFETs and (b) pMOSFETs.

defects in HfO_2 fluctuates through charge trapping/detrapping with the pWF gate electrode. Therefore, their contribution depends on the work function of the gate metal. This explanation is consistent with the asymmetric reduction in noise seen in Fig. 4 (27x for the nMOSFET and 4x for the pMOSFET).

V. Conclusion

We measured planar MOSFETs with low-thermal budget RMG gate-stacks with or without low-temperature treatments using atomic hydrogen (H*) and/or oxygen (O*) and showed their effect on the dc and 1/*f* noise characteristics. We demonstrated that the low-thermal budget passivation treatments with atomic hydrogen (H*) and oxygen (O*) decrease the 1/*f* noise down to a level competitive with high-thermal budget devices. Extensive comparison with an advanced model of 1/*f* noise led us to identify the defects in SiO_2 (identified as H-E' defects) as the main cause of 1/*f* noise in both nMOSFETs and pMOSFETs when the dielectric is not passivated with high-temperature anneals or dedicated radical treatments. After passivation, the noise of the nMOSFETs is still dominated by H-E' defects, while the noise of the pMOSFETs starts to be dominated by deep traps in HfO_2 that are accessible through the pWF gate metal.

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References

[1] W. Rachmady et al., "300 mm heterogeneous 3D integration of record performance layer transfer germanium PMOS with silicon NMOS for low power high performance logic applications," in *IEDM Tech. Dig.*, Dec. 2019, pp. 29.7.1–29.7.4, doi: 10.1109/IEDM19573.2019.8993626.

[2] X. Wu, P. C. H. Chan, S. Zhang, C. Feng, and M. Chan, "A three-dimensional stacked fin-CMOS technology for high-density ULSI circuits," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1998–2003, Sep. 2005, doi: 10.1109/TED.2005.854267.

[3] H. W. Then et al., "3D heterogeneous integration of high performance high-K metal gate GaN NMOS and Si PMOS transistors on 300 mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications," in *IEDM Tech. Dig.*, Dec. 2019, pp. 17.3.1–17.3.4, doi: 10.1109/IEDM19573.2019.8993583.

[4] C. Auth et al., "45nm high-k + metal gate strain-enhanced transistors," in *Proc. Symp. VLSI Technol.*, Jun. 2008, pp. 128–129, doi: 10.1109/VLSIT.2008.4588589.

[5] A. Mallik et al., "The impact of sequential-3D integration on semiconductor scaling roadmap," in *IEDM Tech. Dig.*, Dec. 2017, pp. 32.1.1–31.1.4, doi: 10.1109/IEDM.2017.8268483.

[6] A. Vandooren et al., "Demonstration of 3D sequential FD-SOI on CMOS FinFET stacking featuring low temperature Si layer transfer and top tier device fabrication with tier interconnections," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Jun. 2022, pp. 330–331, doi: 10.1109/VLSITechnologyandCir46769.2022.9830400.

[7] S. Subramanian et al., "First monolithic integration of 3D complementary FET (CFET) on 300 mm wafers," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265073.

[8] B. Ye et al., "NBTI mitigation by optimized HKMG thermal processing in a FinFET technology," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 905–909, Mar. 2022, doi: 10.1109/TED.2021.3139566.

[9] J. Franco et al., "Low-temperature atomic and molecular hydrogen anneals for enhanced chemical SiO_2 IL quality in low thermal budget RMG stacks," in *IEDM Tech. Dig.*, Dec. 2021, pp. 31.4.1–31.4.4, doi: 10.1109/IEDM19574.2021.9720657.

[10] J. Franco et al., "Low thermal budget PBTI and NBTI reliability solutions for multi-V_{th} CMOS RMG stacks based on atomic oxygen and hydrogen treatments," in *IEDM Tech. Dig.*, Dec. 2022, pp. 30.4.1–30.4.4, doi: 10.1109/IEDM45625.2022.10019385.

[11] J. Franco et al., "Novel low thermal budget CMOS RMG: Performance and reliability benchmark against conventional high thermal budget gate stack solutions," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6658–6664, Dec. 2023, doi: 10.1109/TED.2023.3314001.

[12] J. R. Hauser and K. Ahmed, "Characterization of ultra-thin oxides using electrical C–V and I–V measurements," in *Proc. Int. Conf. Characterization Metrol. ULSI Technol.*, 1998, pp. 235–239, doi: 10.1063/1.56801.

[13] M. Karner et al., "A multi-purpose Schrödinger-Poisson solver for TCAD applications," *J. Comput. Electron.*, vol. 6, nos. 1–3, pp. 179–182, Sep. 2007, doi: 10.1007/s10825-006-0077-7.

[14] L. P. B. Lima, H. F. W. Dekkers, J. G. Lisoni, J. A. Diniz, S. Van Elshocht, and S. De Gendt, "Metal gate work function tuning by Al incorporation in TiN," *J. Appl. Phys.*, vol. 115, no. 7, Feb. 2014, Art. no. 074504, doi: 10.1063/1.4866323.

[15] A. Ortiz-Conde, F. J. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 583–596, Apr./May 2002, doi: 10.1016/S0026-2714(02)00027-6.

[16] R. Asanovski, J. Franco, P. Palestri, B. Kaczer, and L. Selmi, "Investigating the correlation between interface and dielectric trap densities in aged p-MOSFETs using current-voltage, charge pumping, and $1/f$ noise characterization techniques," *Solid-State Electron.*, vol. 207, Sep. 2023, Art. no. 108722, doi: 10.1016/j.sse.2023.108722.

[17] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Phys. Status Solidi, A*, vol. 124, no. 2, pp. 571–581, Apr. 1991, doi: 10.1002/pssa.2211240225.

[18] D. M. Fleetwood, "$1/f$ noise and defects in microelectronic materials and devices," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1462–1486, Aug. 2015, doi: 10.1109/TNS.2015.2405852.

[19] L. K. J. Vandamme and F. N. Hooge, "What do we certainly know about $1/f$ noise in MOSTs?" *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3070–3085, Nov. 2008, doi: 10.1109/TED.2008.2005167.

[20] R. Asanovski, P. Palestri, E. Caruso, and L. Selmi, "A comprehensive gate and drain trapping/detrapping noise model and its implications for thin-dielectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4826–4833, Oct. 2021, doi: 10.1109/TED.2021.3104790.

[21] R. Asanovski, P. Palestri, and L. Selmi, "Importance of charge trapping/detrapping involving the gate electrode on the noise currents of scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1313–1320, Mar. 2022, doi: 10.1109/TED.2022.3147158.

[22] R. Asanovski, P. Palestri, and L. Selmi, "On the accuracy of the formula used to extract trap density in MOSFETs from $1/f$ noise," *Solid-State Electron.*, vol. 194, Aug. 2022, Art. no. 108311, doi: 10.1016/j.sse.2022.108311.

[23] E. G. Ioannidis, C. A. Dimitriadis, S. Haendler, R. A. Bianchi, J. Jomaah, and G. Ghibaudo, "Improved analysis and modeling of low-frequency noise in nanoscale MOSFETs," *Solid-State Electron.*, vol. 76, pp. 54–59, Oct. 2012, doi: 10.1016/j.sse.2012.05.035.

[24] K. Li et al., "Low-frequency noise and border traps in irradiated nMOS and pMOS bulk Si FinFETs with SiO_2/HfO_2 gate dielectrics," *IEEE Trans. Nucl. Sci.*, vol. 70, no. 4, pp. 442–448, Apr. 2023, doi: 10.1109/TNS.2023.3239844.

[25] G. Rzepa et al., "Complete extraction of defect bands responsible for instabilities in n and pFinFETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573437.

[26] K. Torii et al., "Physical model of BTI, TDDB and SILC in W_{02}-based high-k gate dielectrics," in *IEDM Tech. Dig.*, 2004, pp. 129–132, doi: 10.1109/IEDM.2004.1419085.

[27] J. Woo Lee et al., "$1/f$ noise analysis of replacement metal gate bulk p-type fin field effect transistor," *Appl. Phys. Lett.*, vol. 102, no. 7, Feb. 2013, Art. no. 073503, doi: 10.1063/1.4793306.

[28] G. Rzepa et al., "Comphy—A compact-physics framework for unified modeling of BTI," *Microelectron. Rel.*, vol. 85, pp. 49–65, Jun. 2018, doi: 10.1016/j.microrel.2018.04.002.

[29] *Sentaurus Device*, Synopsys Inc, Mountain View, CA, USA, 2022.

[30] C. Wilhelmer et al., "Ab initio investigations in amorphous silicon dioxide: Proposing a multi-state defect model for electron and hole capture," *Microelectron. Rel.*, vol. 139, Dec. 2022, Art. no. 114801, doi: 10.1016/j.microrel.2022.114801.

[31] J. Franco et al., "Impact of work function metal stacks on the performance and reliability of multi-V_{th} RMG CMOS technology," *Solid-State Electron.*, 2023.

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