Correlating Interface and Border Traps With Distinctive Features of *C–V* Curves in Vertical Al_2O_3/GaN MOS Capacitors

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***Abstract*— In this article, we present an analysis of the correlation between interface traps (ITs) and border traps (BTs) on distinctive features of *C–V* curves in vertical Al_2O_3/gallium-nitride (GaN) MOS capacitors. First, pulsed *C–V* curves were characterized during the application of quiescent gate bias stresses of different magnitudes and signs. This characterization revealed four main distinctive features: 1) rightward rigid shift; 2) leftward rigid shift; 3) decrease of the ΔC–ΔV slope; and 4) formation of a hump in a gate bias range before the accumulation of electrons at the oxide/semiconductor interface. By means of a combined experimental/simulation analysis, these features were univocally attributed to specific ITs or BTs in the overall trap distribution. The simulation-aided analysis enhances the physical understanding of the *C–V* curves features and increases the dependability of the adopted IT measurement technique, allowing for a more rapid process optimization and device technology development.**

***Index Terms*— Al_2O_3, border traps (BTs), interface traps (ITs), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), vertical gallium-nitride (GaN) metal-oxide-semiconductor capacitor (MOSCAP).**

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I. Introduction

GALLIUM-NITRIDE (GaN) field-effect transistors are currently being developed as switches for efficient power electronic converters. While several lateral GaN HEMT technologies have become commercially available, the achievement of reliable vertical devices is one of the goals that are more intensively pursued at the research level, for their advantages over lateral counterparts in high-power applications [1], [2].

In vertical transistors, the drift region develops through the device depth, so that increasing the maximum blocking voltage does not require the device to be extended laterally and the peak electric field in the OFF-state is far from the device surface. As a result, relatively small-area devices can be designed, which can operate in the kV range and are naturally immune from surface- and buffer-related, current-collapse and dynamic R_{ON} effects, that instead affect lateral device operation [3], [4], [5], [6], [7]. In addition, avalanche capability has been demonstrated in vertical GaN devices [8], [9], [10], [11] allowing for reliable, unclamped inductive switching in converter circuits [10].

As for the possible vertical transistor typologies, Fin MOSFETs [2], [12], vertical planar [13], and Trench MOSFETs [14], [15] are among the most targeted ones, providing feasible solutions for normally-OFF, low gate leakage, and high-voltage operation. Because these device technologies under development still suffer from significant trapping effects related to the MOS stack [16], [17], [18], control of the gate-stack quality is a critical issue that requires careful characterization during the process optimization loop. This calls for appropriate test structures and dependable experimental techniques for the characterization of the interface trap (IT) and border trap (BT) states, the latter being defects located in the oxide at 1–2 nm from the interface that can be easily reached by channel electrons through tunneling [16], [19], [20], [21], [22].

In this work, we present an analysis of the charge-trapping processes in quasi-vertical Al_2O_3/GaN MOS capacitors, extending some of the results presented in [23]. The experimental characterization relies on pulsed *C–V* measurements applied to devices in the fresh state as well as subjected

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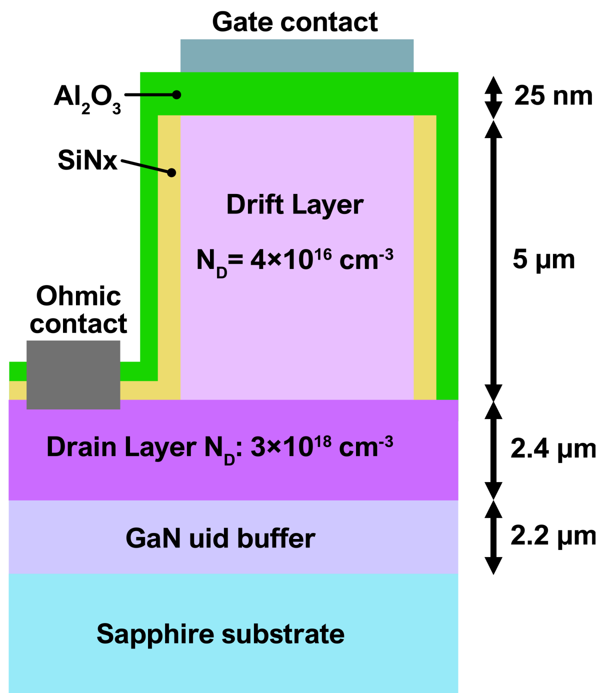

Fig. 1. Schematic cross section of the vertical Al_2O_3/GaN MOSCAP under test. The main dimensions are indicated.

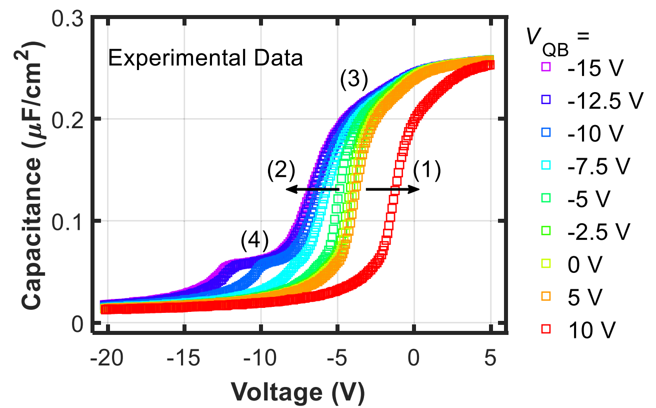

Fig. 2. Pulsed C–V curves extracted at different gate quiescent stress biases (V_{QB}, see legend). (1)–(4) indicate the distinctive features of the C–V curves that are under investigation in this work: rightward rigid shift, leftward rigid shift, decrease of $\Delta C/\Delta V$ slope, and hump formation.

to gate-bias stresses of both signs. The IT density (D_{IT}) is extracted in a wide energy range (>2 eV from the conduction-band edge) of the GaN bandgap. The D_{IT} extraction is performed by means of a modified method based on the photo-assisted C–V technique [24], [25], exploiting a large, negative gate voltage to discharge surface and BTs in place of UV illumination. Furthermore, the impact of ITs and BTs on the C–V curves and the accuracy of the extracted D_{IT} distribution are assessed by means of device simulations. Simulations allow correlating different features of the C–V curves and the effects induced by gate bias stresses with the type (interface or border, donor or acceptor) as well as the energy range of responsible trap states.

The rest of this article is organized as follows. Section II describes the devices under test and the experimental characterization methodology. Section III includes the simulation setup, results, as well as a discussion to compare the experimental and simulation outcomes. Section IV draws the conclusions.

II. Experimental Characterization

Characterized devices are quasi-vertical Al_2O_3/GaN MOS capacitors fabricated as test structures for a vertical GaN-based MOSFET technology [15]. The semiconductor armature of the MOS capacitor corresponds to the n^- drift layer of the Trench MOSFET, with a doping density of 4×10^{16} cm^{-3}. The GaN surface was pretreated with NH_3 plasma before the atomic layer deposition (ALD) of 25-nm Al_2O_3 [26]. A schematic cross section is shown in Fig. 1, while more details on the fabrication process can be found in [11].

The MOS capacitor stability was characterized by monitoring the effects on the C–V curve of gate-quiescent-bias stresses (V_{QB}) of both signs and different magnitudes. Fig. 2 collects the results from these experiments. Acquisition of the C–V curves exploited a variant of the experimental setup described in detail in [15], [16], and [17] and summarized as follows. Each stress voltage V_{QB} is applied to the gate terminal for 100 s (to ensure reaching steady-state conditions), and then, periodically, every 1 s, the voltage is switched from V_{QB} to V_M for 1 ms.

The capacitance value is acquired by an analog *LCR* meter at 1 MHz and 0.1-V ac frequency and amplitude. To improve the signal-to-noise ratio, for each pulse at V_M, capacitance is obtained by averaging the readings for ≈0.5 ms after settlement of the instrument. V_M is swept between −20 and 5 V to characterize a full C–V curve. The sequence is repeated for each V_{QB}, ranging from −15 to +10 V. Total stress time is thus about 350 s for each V_{QB} value. Four distinctive features, (1)–(4), of the C–V curves of the MOS capacitor can be identified in Fig. 2. Specifically: i) for small stress voltages (-2.5 V $< V_{QB} <$ 5 V), regardless of the voltage sign, the C–V curves are stable and almost superimposed one to each other [26]; ii) for larger, positive bias (5 V $< V_{QB} <$ 10 V), the C–V curve is shifted rightward rigidly [feature (1)]; and iii) for larger, negative bias ($-15 < V_{QB} < -2.5$ V), the C–V curve is shifted leftward [feature (2)] with related decrease in the $\Delta C/\Delta V$ slope [feature (3)] and formation of a hump [feature (4)] in the low-voltage end of the curve. It should be stressed that from a practical point of view, stress condition i) corresponds to the typical bias range of the gate terminal of a normally-OFF transistor (i.e., with positive threshold voltage, V_T). In addition, feature (1), i.e., the C–V rightward rigid shift, represents a critical limit to the V_T stability in MOSFETs.

To characterize the Al_2O_3/GaN interface and extract the density of ITs (D_{IT}), a modified version of the photo-assisted C–V method was adopted [23]. The method is based on a careful comparison of the C–V measurements in detrapped and trapped conditions [24], [25]. Different from [24] and [25], however, a long, negative gate bias is used in place of UV illumination to induce the discharging of traps. This modified methodology allows to characterize the C–V curves under different trap filling conditions with a much simpler setup compared to the one required for UV illumination. However, in the latter case, electrons trapped in BTs are emitted thanks to the energy provided by the illumination itself, whereas in the former one, the electrical stress discharges the BTs by electron tunneling into the semiconductor. Regarding ITs, both the

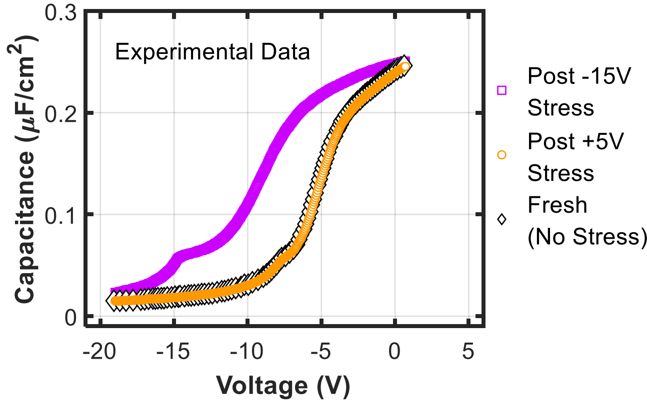

Fig. 3. Fast C–V curves acquired after 1000-s stress at −15 (purple squares) and 5 V (orange circles) used to extract the D_{IT} distribution shown in Fig. 4 with the modified photo-assisted C–V method described in the text. Fresh C–V, i.e., acquired before the stress curve (black diamonds) is also shown for reference.

UV illumination as well as the long negative electrical stress cause detrapping by electron emission to the semiconductor conduction band. This point is further discussed later on.

A strong negative bias of −15 V was applied to the MOS capacitor for 1000 s, and a fast C–V curve was acquired (i.e., with a 10-ms sweep) by using the experimental setup described in [18] and [19]. It is important to observe that while this stress condition was applied with the specific intent of emptying the traps (i.e., donor-like traps become positively charged and acceptor-like become neutral), the C–V acquired after stress is still subjected to trap-related features. As a matter of fact, during the voltage sweep of the measurement itself, ITs change their charge state (i.e., donor-like traps become neutral and acceptor-like traps become negatively charged) due to the capture of electrons at the semiconductor surface. Conversely, the BT state is not altered by the fast C–V measurement.

Additionally, by applying +5 V to the gate for 1000 s, another fast C–V curve is recorded with the same setup as for the negative stress. The two C–V curves are shown in Fig. 3. Fresh C–V curve, i.e., acquired before stress, is also shown for reference. As can be noted from Fig. 3, the post +5-V stress C–V curve almost overlaps with the fresh one, indicating the excellent robustness of the ALD-deposited Al_2O_3 layer against forward bias stress.

D_{IT} is obtained from the slope of the ΔV versus ψ_s curve, where ΔV is the voltage difference obtained at each capacitance value between the "Post −15-V" and "Post +5-V" curves in Fig. 3, and ψ_s is the surface potential obtained as in [23]. That is,

$$D_{IT} = \frac{C_{ox}}{qA}\left(\frac{d\Delta V}{d\psi_s}\right) \quad (1a)$$

$$\psi_s = \frac{q\varepsilon_s N_D A^2}{2C_s(V)^2} \quad (1b)$$

where C_{ox} is the oxide capacitance, A is the area of the metal-oxide-semiconductor capacitor (MOSCAP), q is the elementary charge, ε_s is the dielectric constant of the semiconductor, N_D is the doping of the drift layer, and C_s is the semiconductor capacitance (obtained from the measured gate capacitance C_{meas} as $C_s^{-1} = C_{meas}^{-1} - C_{ox}^{-1}$).

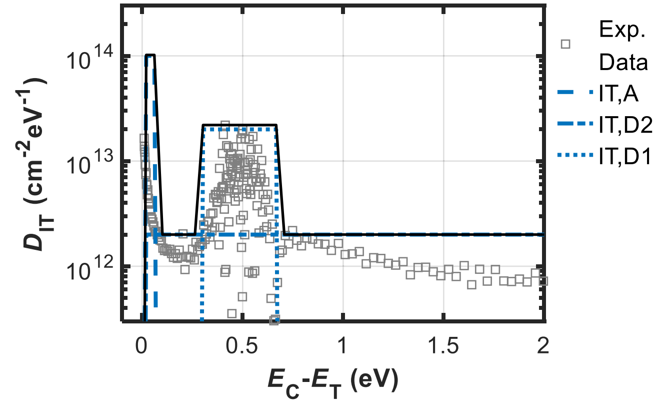

Fig. 4. D_{IT} versus E_C–E_T used in the simulations to reproduce the experimental pulsed C–V curves (see Fig. 6). Black solid line is the IT distribution, and blue dashed, dashed-dotted, and dotted lines are the three single boxes contributing to the overall distribution. Experimental data are reported as gray symbols for comparison.

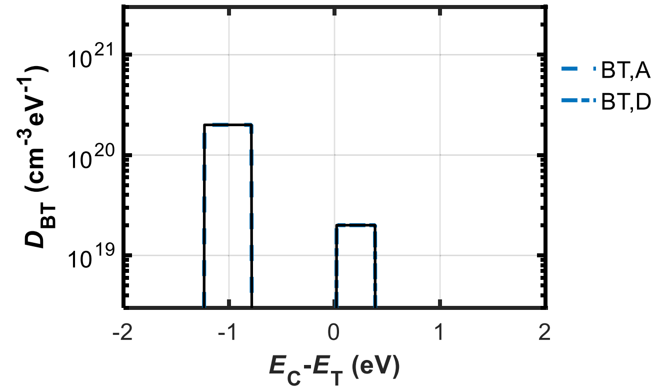

Fig. 5. D_{BT} versus E_C–E_T used in the simulations to reproduce the experimental pulsed C–V curves (see Fig. 6). Black solid line is the BT distribution, and blue dashed and dashed-dotted lines are the single boxes contributing to the overall distribution (see legend).

The trap distribution versus trap energy (with respect to the conduction band edge, E_C) is reported in Fig. 4 for a typical device (gray symbols). As it can be seen, the obtained D_{IT} covers a remarkedly wide range of >2 eV from E_C, and it shows the presence of a 2×10^{13} cm^{-2}·eV^{-1} peak at about 0.5 V below E_C. This peak overlaps with the typical U-shaped continuum of interface states rapidly increasing at the band edges (here, only the portion near E_C can be probed by this method). Deep ITs (i.e., with energies between 1 and 2 eV) extracted in Fig. 4 effectively emit electrons (and can thus be probed by this method). We attribute this to an electric-field-enhancement mechanism reducing emission times (e.g., Poole–Frenkel). The electrical behavior of traps (i.e., acceptor- or donor-like) can only be clarified by calibrated simulations, as discussed in Section III.

III. Device Simulations and Discussion

The 2-D numerical device simulations were performed with the SDevice simulator included in the Synopsys TCAD suite [27] aimed at: 1) analyze the impact of ITs and BTs on the features (1)–(4) induced by positive and negative stresses on the C–V curves discussed in Section II and 2) provide a cross-validity check of the method for D_{IT} extraction proposed in [23]. Simulations account for ITs using a fully dynamic Shockley-Read-Hall (SRH) model (no quasi-static approximation), self-consistently coupled to the drift–diffusion

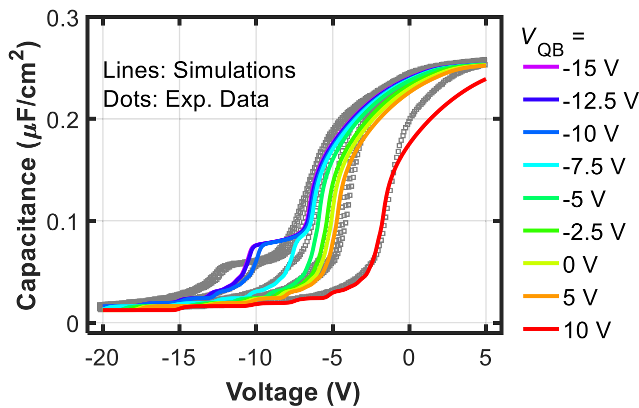

Fig. 6. Simulated C–V curves (colored solid lines) obtained with the same method as the experimental data (gray symbols) with different gate quiescent stress biases (V_{QB}, see legend). Features of the C–V curves observed in the measurements are correctly reproduced by the simulations.

TABLE I
IT AND BTS PARAMETERS USED IN THE SIMULATIONS

Label	Areal Density (D, $cm^{-2}.eV^{-1}$)	Volume Density (D, $cm^{-3}.eV^{-1}$)	Energy Mean (eV)†	Energy Spread (eV)
IT,A	10^{14}	//	0	0.2
IT,D2	2×10^{12}	//	1.7	3.4
IT,D1	2×10^{13}	//	0.5	0.4
BT,A	//	2×10^{20}	–1	0.5
BT,D	//	2×10^{19}	0.2	0.4

†Positive (negative) energy means below (above) E_C.

model. On the other hand, BTs are placed into the Al_2O_3 region and are linked to the semiconductor surface through a Wentzel–Kramer–Brillouin (WKB)-approximation-based nonlocal tunneling model ("tunneling into traps" model in [27]).

The energy distributions of ITs and BTs that were implemented in the simulator are shown in Figs. 4 and 5, respectively. Black solid lines are used for the overall IT and BT distributions yielding the best agreement with experimental data (see Fig. 6), and blue lines with different styles (see legend) are used instead for indicating the various components of the adopted distributions that, as later discussed, can be linked one-to-one with the distinctive features of the C–V curves. Box-like distributions were adopted for easier parametrization. Trap parameters are summarized in Table I.

Fig. 6 shows the C–V curves obtained by simulations incorporating the IT and BT distributions depicted with the black solid line in Figs. 4 and 5. In the simulator, the gate voltage is swept with the same pulse sequence used in the experiments, while the capacitance is obtained through a linearized, small-signal ac analysis. As can be noted from Fig. 6, a good agreement with experimental C–V curves is achieved, specifically, all the (1)–(4) features induced by positive and negative gate bias stresses are successfully captured by simulations. This was achieved by: 1) using an IT distribution that reproduces, within a box-wise approximation, the measured D_{IT} (compare the black and gray solid lines in Fig. 4) and 2) including two BT boxes with density and energy position that have been used as fitting parameters. As will be clarified by the subsequent sensitivity analysis, BTs induce only rigid shifts in the C–V curves (of positive and negative signs for positive and negative gate bias stresses, respectively). However, because the "photo-assisted C–V"-like method described in Section II allows only to determine the differential variations of the post −15-V and post +5-V stress C–V curves in Fig. 3, BT distributions cannot be directly characterized. Thus, the relative parameters are obtained by fitting the simulations with experimental data. On the other hand, simulations confirm that the $\Delta C/\Delta V$ slope as well as the hump centered at about 0.5 eV below E_C is governed solely by ITs.

For these reasons, results in Fig. 6 provide a meaningful, accuracy-validation procedure for the adopted D_{IT} measurement method, indicating also that the energy depth of the IT distribution probed by this technique is sufficient to explain trapping effects occurring in a wide range of gate biases.

With respect to the optimal distributions yielding the results of Fig. 6, simulations with varied IT and BT boxes have been carried out. More specifically, we performed a new set of simulations by selectively setting the concentration of each of the trap boxes in the distribution to 0. By this way, we obtain a one-to-one link between the distinctive features (1)–(4) induced by gate bias stresses on the C–V curves and the single components of the overall trap distribution. For simplicity, we did not include any field-enhancement emission model in the simulation setup. For this reason, IT,D2 traps with energies $>\approx 1$ eV remain always neutral in the simulations.

Results of the sensitivity analysis are reported in Fig. 7. As discussed previously, Fig. 7(a)–(d) allows to immediately identify the correspondence between the observed (1)–(4) features of C–V curves and different components of the overall IT and BT distributions. In fact, Fig. 7 allows observing that removing a specific BT or IT box in the distribution consequently makes the simulations fail to capture one (and only one) distinctive feature in the C–V curves. On the other hand, results in Fig. 7 allow to conclude that feature: (1) that is, the rightward rigid shift, is due to the BTs acting as acceptors, BT,A. This information is critically important for ALD layer optimization achieved through BT reduction; (2) that is, the leftward rigid shift, is due to the BTs acting as donors, BT,D; (3) that is, the decrease of $\Delta C/\Delta V$ slope, is due to the ITs acting as acceptors, IT,A. This is important as subthreshold slope degradation leads to increased switching losses; and (4) that is, the formation of a hump in the gate bias range before the accumulation of channel electrons, is due to the ITs acting as donors, IT,D1.

From a practical point of view, features (1) and (3) are the most relevant ones, as the former leads to positive V_T shift and the latter to switching losses. Therefore, for practical application of the investigated test structures in the epitaxy of GaN vertical transistors, it is of utmost importance to reduce acceptor traps—either at the interface or in the gate oxide—to minimize V_T shift and reduce switching losses.

The role of IT,D1 traps in determining feature (4) is explained as follows. When applying a large negative quiescent bias (e.g., −15 V), the Fermi levels drop below the trap energy levels, thus positively charging these traps as a consequence of electron emission according to the SRH model.

During the capacitance measurement, as the voltage is swept from −20 to +5 V, the position of the Fermi level varies according to the bias and the state of the positively charged donor-like ITs consequently changes. This is illustrated in Fig. 8, showing the neutralized donor density (D^0_{IT})

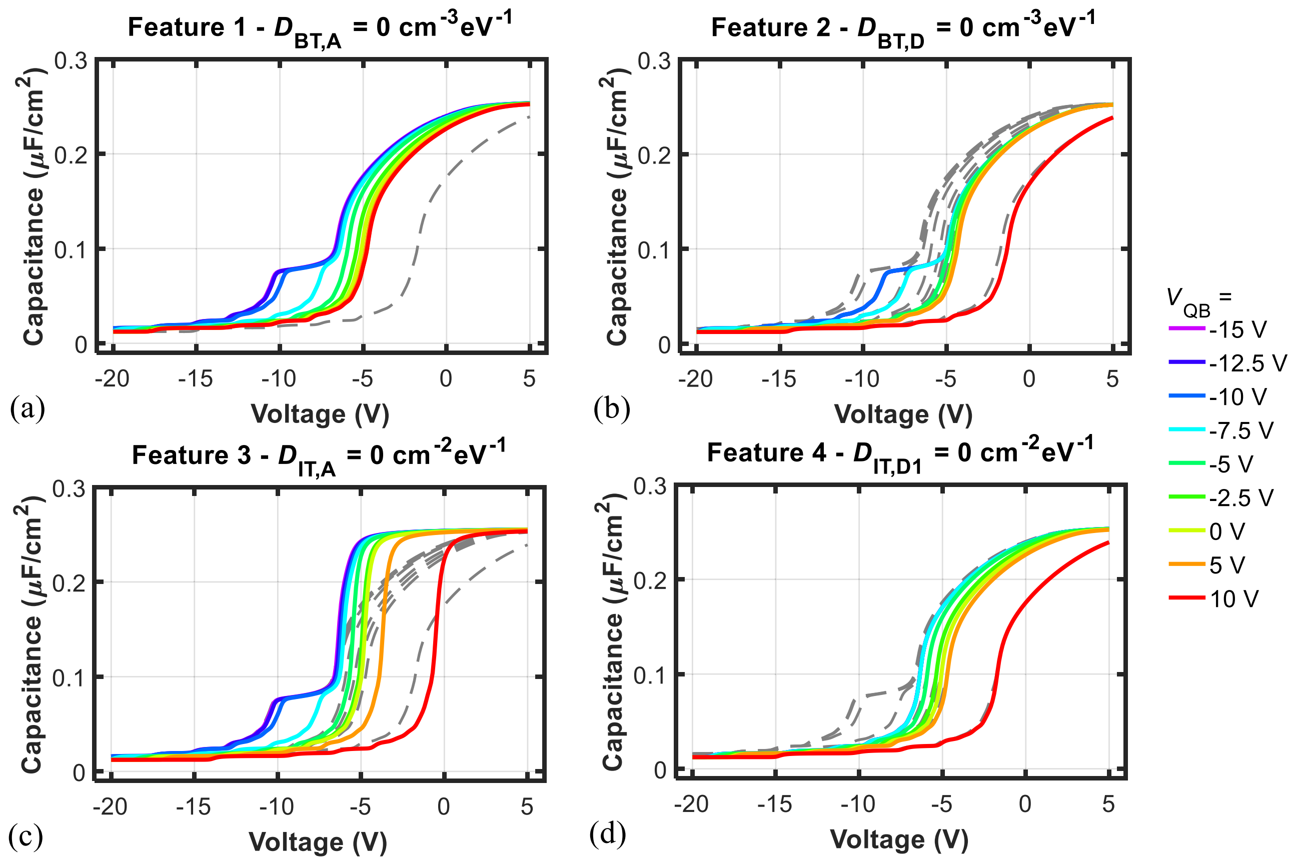

Fig. 7. Simulated C–V curves with different IT and BT concentrations with respect to the calibration setup, the corresponding results of which are reported with dashed lines. The sensitivity analysis highlights the role of different components of the trap distribution on the features (1)–(4) of the C–V curves identified in the text: (a) $D_{BT,A} = 0$ cm^{-3}·eV^{-1} leads to no positive rigid shift; (b) $D_{BT,D} = 0$ cm^{-3}·eV^{-1} leads to no negative rigid shift; (c) $D_{IT,A} = 0$ cm^{-2}·eV^{-1} leads to sharp $\Delta C/\Delta V$ slope; and (d) $D_{IT,D1} = 0$ cm^{-2}·eV^{-1} leads to no hump formation for negative V_{QB}.

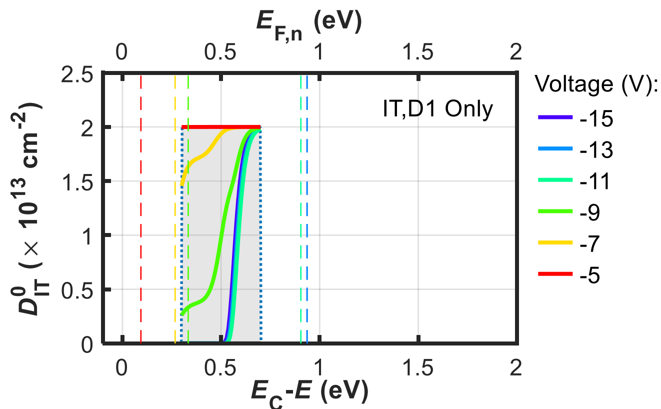

Fig. 8. Ionized trapped charge (D^0_{IT}) due to IT,D1 only versus energy referred to GaN conduction band edge (E_C) for different voltage bias (see legend) extracted from the simulation of the C–V curve with $V_{QB} = -15$ V. The box-like distribution of IT,D1 defined in Table I is reported for reference (shaded region). The electron quasi-Fermi level ($E_{F,n}$) for each bias is also shown (dashed lines).

versus energy referred to E_C as in Fig. 4 for the bias range between -15 and -5 V extracted from the simulation of the C–V curve with $V_{QB} = -15$ V (see Fig. 6). To focus on the understanding of feature (4), the D^0_{IT} extracted from the simulations is the one relative to IT,D1 only. The "box-like" IT,D1 distribution defined in Table I is also reported for reference. Fig. 8 also shows the position of the electron quasi-Fermi level ($E_{F,n}$) extracted from the simulator for the same bias range. Clearly from Fig. 8, it is possible to observe how D^0_{IT} increases as the bias is increased, and therefore, $E_{F,n}$ moves closer to E_C. This correlates with the reduced positive charge at the origin of the ledge. Specifically, these traps get neutralized as they progressively capture electrons coming from the bulk of the drift layer and accumulating at the Al_2O_3/GaN interface. The reducing positive charge progressively shifts the accumulation towards more positive bias (i.e., it is necessary to apply a more positive voltage to increase the accumulation capacitance), and this is appreciated in the C–V curves as feature (4).

Feature (4) can also be understood from the band diagrams shown in Fig. 9 taken at different biases and extracted from the simulation of the C–V curves with $V_{QB} = -15$ V. The shaded energy region in Fig. 9 is plotted in the energy range of IT,D1 distribution (see Figs. 4 and 8). From Fig. 9, one can observe that at $V = -15$ V, ITD,1 is above $E_{F,n}$, and thus, it is empty of electrons. Conversely, at $V = -5$ V, ITD,1 is below $E_{F,n}$, and thus, it is full of electrons. This correlates with the results shown in Fig. 8 and further explains the formation of the hump in Fig. 6 as due to the modulation of IT,D1 trap occupation.

The combined experimental/simulation analysis carried out in this work allows clearly pinpointing the single trap contributions responsible for each of the distinctive features of the pulsed C–V curves. While the simulated IT distribution

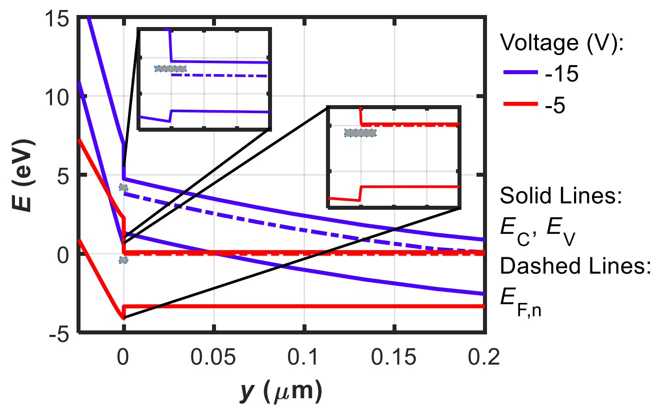

Fig. 9. Band diagrams along device depth (y) at different voltages (see legend) extracted from the simulation of the C–V curves with $V_{QB} = -15$ V. The gray-shaded region is plotted in the energy range of the ITD,1 distribution (see Figs. 4 and 8). At $V = -15$ V (-5 V), ITD,1 is above (below) $E_{F,n}$, and thus, it is empty (full) of electrons (see insets).

reproduces the one extracted from the modified photo-assisted C–V measurements, providing a means to validate the adopted method, the setup also includes the BTs responsible for the observed rightward/leftward shifts of the C–V curves, which cannot be extracted with the previous method, thus also augmenting the information obtained from the experiments.

IV. Conclusion

Vertical Al_2O_3/GaN MOSCAPs were characterized by means of pulsed C–V curves extracted while stressing at both negative and positive quiescent gate biases. The characterization revealed four main distinctive features of the C–V curves induced by different stress biases, namely, rightward and leftward rigid shifts, decrease of the $\Delta C/\Delta V$ slope, and formation of a hump. By means of a combined experimental and simulation analysis, these features were attributed to either ITs or BTs (i.e., in the Al_2O_3 within few nanometers from the interface). The enhanced physical understanding of the distinctive features of the C–V curves and the increased dependability of the adopted D_{IT} measurement technique obtained with the simulations is instrumental for a more rapid process optimization and device technology development. In this sense, for proper operation of these test structures in GaN normally-OFF vertical transistors, it is primarily important to reduce acceptor traps—either at the interface or in the gate oxide—to minimize V_T instability and reduce switching losses.

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