First Evidence of SET-Like Behavior of 3-D NAND Flash Cells in the Deep-Cryogenic Regime

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Abstract—**In this article, we report the first experimental investigation of the behavior of the 3-D NAND Flash memory technology in the deep-cryogenic regime (temperature $T < 50$ K). Clear evidence is provided to demonstrate that, in that T regime, the reduction of the Read bitline voltage gives rise to a paradigm shift in the current–voltage characteristics of the memory cells, consisting of the appearance of single-electron transistor (SET)-like conduction schemes. The phenomenon is traced back to nonuniformities in the electrostatic inversion of cell channel, producing, at that deep-cryogenic T, a landscape of conductive quantum dots separated by energy barriers where electron transport is affected by Coulomb blockade. The results represent a first step toward innovative applications of 3-D NAND Flash memories.**

Index Terms—**3-D array, NAND Flash memory, polysilicon, semiconductor device modeling, single-electron transistor (SET).**

I. INTRODUCTION

QUANTUM computing is stimulating widespread research interest in the operation of CMOS technologies in the deep-cryogenic regime. This interest is motivated by the twofold target of conceiving new solid-state device structures for qubits compatible with mainstream integration flows [1], [2], [3], [4] and of designing the control electronics needed to drive the qubits with an as small as possible temperature (T) gradient from them [5], [6], [7]. In spite of its relevance in the semiconductor arena, the potential of the 3-D NAND Flash memory technology in such application field is still unexplored. In particular, the research on the cryogenic operation of 3-D NAND Flash memories has been limited so far to a minimum temperature of 77 K [8], [9], [10],

leaving completely uncharted the T range below 50 K. The latter T range, however, is the most interesting for quantum computing applications. Moreover, it has already been shown to trigger some noteworthy changes in the behavior of other CMOS devices with respect to what predicted by room temperature (RT) analyses [3], [7], [11], [12], [13], [14], suggesting that something similar may also happen for 3-D NAND Flash cells.

In this article, we address for the first time the behavior of 3-D NAND Flash cells in the deep-cryogenic regime ($T < 50$ K). Through detailed experimental analyses, we show that, in that T regime, single-electron transistor (SET)-like conduction traces emerge from the current–voltage characteristics of the memory cells when the Read bitline voltage (V_{BL}) is reduced. The phenomenon is explained in terms of nonuniform channel inversion, leading to conductive quantum dots isolated by energy barriers through which electron transport may be significantly affected by Coulomb blockade. The results pave the way to new potential applications of 3-D NAND Flash memories.

II. EXPERIMENTAL SAMPLES AND SETUP

The samples investigated in this work are test elements for 3-D NAND Flash memory arrays featuring vertical polysilicon channels and 50 stacked wordline layers. The test elements offer direct access to the contact of 11 wordlines, two string select lines, and two bitlines of a NAND mini-array through independent pads. The contacts of all the remaining wordlines are short-circuited and can be accessed through a single pad for proper string biasing during array operation. The cells connected to the string select lines and bitlines, which cannot be independently addressed, can be considered as dummy cells in the mini-array. Cells dimensions correspond to the state-of-the-art for the NAND technology. To carry out electrical measurements at cryogenic T, the silicon die of the test element was encapsulated in a ceramic package which was mounted on the cold head of a closed-cycle helium-operated cryostat. Fig. 1 shows an overview of the experimental setup. A semiconductor parameter analyzer and an arbitrary waveform generator (AWG) were used to apply the electrical signals to the sample under test needed to collect
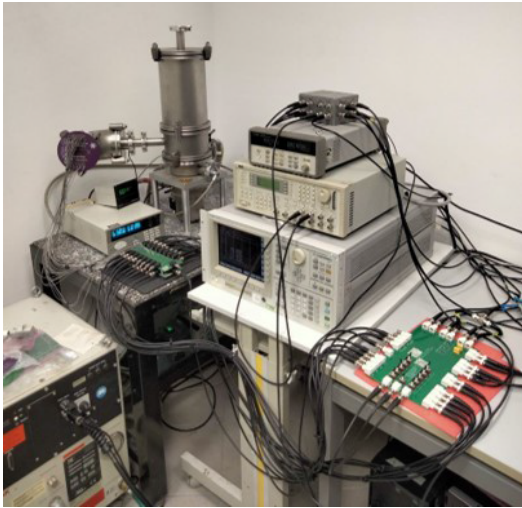
Fig. 1. Overview of the experimental setup used in this work to investigate 3-D NAND Flash cells down to the deep-cryogenic regime.
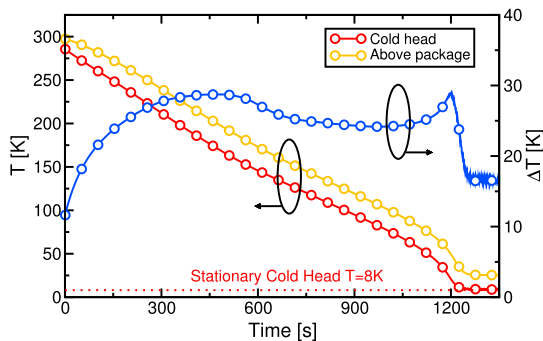

Fig. 2. Transient of T measured on the cold head of the cryostat and on the top surface of the package mounted inside it during a cooling cycle. ΔT is the difference between the two T values.

the trans-characteristics of a selected cell and to perform the Program/Erase operations on it. A switching matrix and some ad hoc printed circuit boards (PCB) were used to configure the connection of the measurement instruments to the pins of the package in the cryostat. T of the die under test was estimated through two sensors connected, respectively, to the cold head of the cryostat and to the top surface of the package mounted on it. Fig. 2 shows a representative example of the T transient detected by the two sensors over a cooling cycle of the cryostat. The results show that the cold head (red curve) reaches a minimum T nearly equal to 8 K in the test. The T value measured on the top surface of the package (yellow curve) approximately follows the transient of the cold head but with an offset ΔT in-between 15 and 30 K (blue line). This offset can be traced back to the thermal resistance of the package and of its contact with the cold head of the cryostat. It is worth pointing out, anyway, that when the cold head reaches its stationary T, ΔT reduces to about 15 K. This corresponds to a T of the die under test in the range between 8 and 23 K at that point of the test. Provided that a more careful assessment of T of the die under test is not required to support the results and conclusions reported in this work, we roughly evaluated that T to be $\simeq 15$ K, that is, the average value of its uncertainty interval.
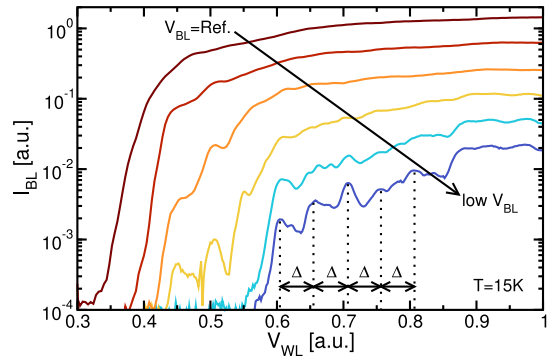

Fig. 3. Representative example highlighting the impact of the reduction of the Read V_{BL} on the trans-characteristic of a 3-D NAND Flash cell at $T = 15$ K. Δ represents the period of the oscillations appearing at the lowest V_{BL}. Note that all the voltages reported in this article are shown normalized to the same arbitrary constant; the same holds for all the currents.

III. EXPERIMENTAL RESULTS

Fig. 3 shows a representative example for the transcharacteristic of the 3-D NAND cells investigated in this work, measured at $T \simeq 15$ K. The curve was obtained by sweeping the wordline voltage (V_{WL}) of the monitored cell while reading its corresponding bitline current (I_{BL}) under different V_{BL}, with the source grounded and all the other wordlines and select lines under pass condition. The data clearly reveal that the decrease in the Read V_{BL} results not only in the expected general reduction of the current through the cell polysilicon channel but also in the appearance of clear humps and oscillations in the $I_{BL}-V_{WL}$ trans-characteristic. This behavior was observed in the vast majority of the cells that were experimentally investigated (a few tens) with, of course, variability in the number, position, and amplitude of the humps and oscillations. In this regard, it is worth mentioning that the results shown in the figures of this section were obtained on different cells, except where otherwise noted.

The oscillations observed in the $I_{BL}-V_{WL}$ transcharacteristic at low V_{BL} can hardly be attributed to the modulation of current transport through cell channel by the capture/emission of charge carriers in microscopic defects in the cell gate stack or at the polysilicon grain boundaries [15], [16], [17], [18], [19], [20], [21]. To rule out this possibility, we sampled I_{BL} at low V_{BL} using V_{WL} values in the range corresponding to an oscillation in the trans-characteristic. As shown in Fig. 4, the results of this test reveal that I_{BL} is perfectly stable over time for all the V_{WL} values, with no signs of the time fluctuations typically arising from the change in the occupancy of microscopic defects [15], [17], [19]. The stability of I_{BL} over time suggests, therefore, that the oscillations in the trans-characteristics appearing at low V_{BL} in Fig. 3 are the outcome of the stationary conduction mechanism of cell channel. This is further proved by the fact that no change in the oscillations appears when modifying the direction and speed of the sweep of V_{WL} used to measure the cell trans-characteristic and when introducing idle periods in-between repeated measurements. This is demonstrated in Fig. 5, where the results obtained when increasing the sweep time by a factor 10 and when introducing idle periods
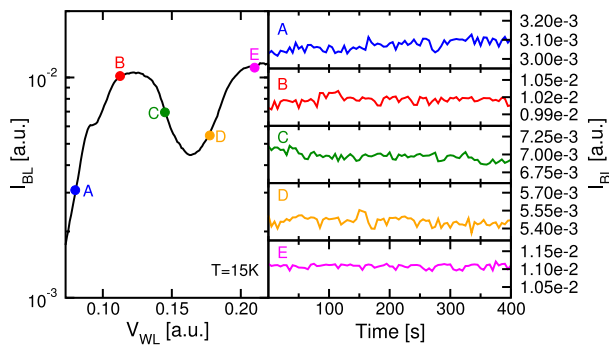
Fig. 4. Left: I_{BL}−V_{WL} trans-characteristic of a cell read with a low V_{BL} at $T = 15$ K. Right: I_{BL} sampled over time at the constant V_{WL} values highlighted with letters from A to E in the left part of the figure.
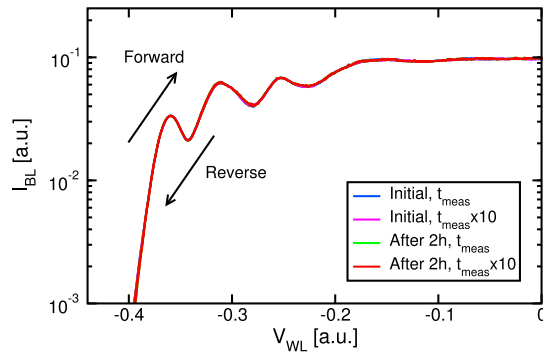

Fig. 5. I_{BL}−V_{WL} trans-characteristic of a cell measured with a low V_{BL} at $T = 15$ K with a forward and reverse sweeps of V_{WL}, different measurement times t_{meas} and after a 2h idle time.
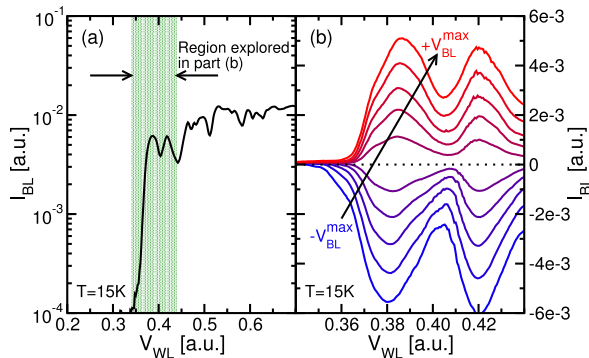

Fig. 6. (a) I_{BL}−V_{WL} trans-characteristic of a cell measured with a low V_{BL} at $T = 15$ K. (b) Same as in (a), but using a linear scale for I_{BL} and for small and closely spaced Read V_{BL} centered around 0 V; the curves were measured only over the V_{WL} interval highlighted in (a).

Fig. 7. Colormap for I_{BL} as a function of V_{WL} and V_{BL} of the cell explored in Fig. 6, at $T = 15$ K. Dashed lines are guidelines highlighting low-conductivity diamonds. The four V_{WL} values marked as 1-4, are those corresponding to the I_{BL}−V_{BL} curves shown in Fig. 8.

Fig. 8. I_{BL}−V_{BL} curves obtained at $T = 15$ K for the four V_{WL} values highlighted in Fig. 7. CB region is the Coulomb blockade region, see Section IV.

between measurements as long as 2h are reported. Finally, it is worth pointing out that the marked periodicity exhibited by some oscillations over the V_{WL} axis (see Fig. 3) is another aspect that can be hardly explained as the outcome of carrier capture/emission in microscopic defects.

To gain further insight into the phenomenology of I_{BL} oscillations, we measured the I_{BL}−V_{WL} trans-characteristic of a monitored cell for a set of small and closely spaced Read V_{BL} centered about 0 V (that is, positive and negative V_{BL} were applied in the test). Fig. 6 shows an example of the curves obtained from the experiment, clearly displaying a couple of I_{BL} oscillations of comparable amplitude over a narrow
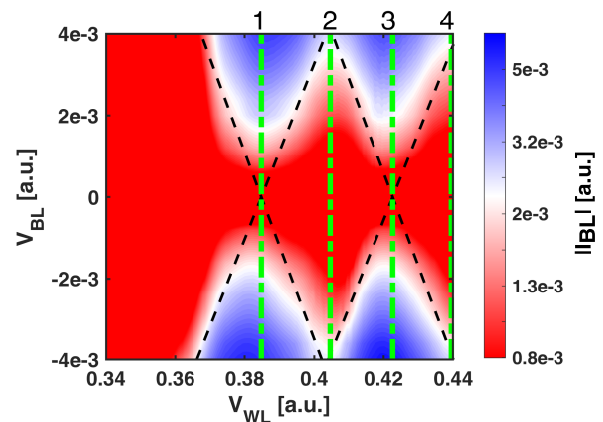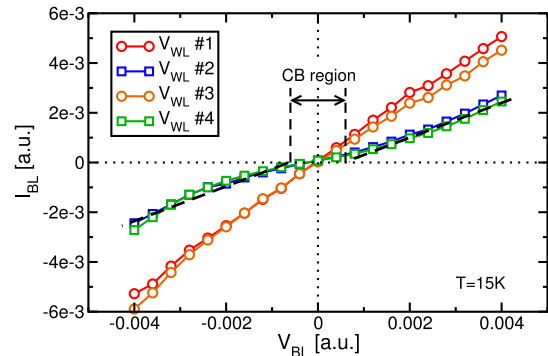
V_{WL} interval for all of the explored V_{BL} values. Fig. 7 reveals that, when I_{BL} is reported as a function of V_{WL} and V_{BL}, such oscillations turn into multiple low-conductivity diamonds. As shown in Fig. 8, values of V_{WL} corresponding to the peak of a diamond result in I_{BL} versus V_{BL} relations featuring an evident turn-on voltage, while that does not happen for values of V_{WL} halfway between the peaks of two consecutive diamonds. Fig. 8 proves, besides, that the I_{BL} versus V_{BL} relations display a monotonic growth with V_{BL}, with no traces of oscillations.

Fig. 9 shows that oscillations in the I_{BL}−V_{WL} trans-characteristic and low-conductivity diamonds more complex than those reported in Figs. 6 and 7 were observed on some cells, pointing out some relevant variability in the explored phenomenology. In this regard, it is worth mentioning that oscillations rising in current and decreasing their peak-to-valley amplitude with the increase in V_{WL} were the most typical observation. Such oscillations result in low-conductivity diamonds reducing their peak over the V_{WL} axis, as shown in Fig. 9. In spite of variability, however, no oscillations were ever detected in the cell I_{BL}−V_{BL} curve.

To complete the picture, we explored the dependence of the reported oscillations on some major parameters of the Read test. Fig. 10 shows, first of all, that varying the pass
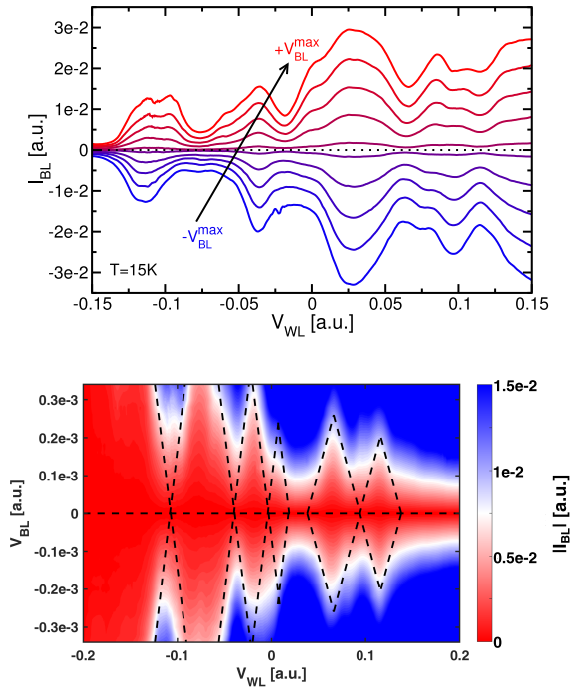
Fig. 9. $I_{BL}-V_{WL}$ trans-characteristic of a cell showing complex oscillations when measured with a low V_{BL} at $T = 15$ K (top) and corresponding colormap for I_{BL} as a function of V_{WL} and V_{BL} (bottom).
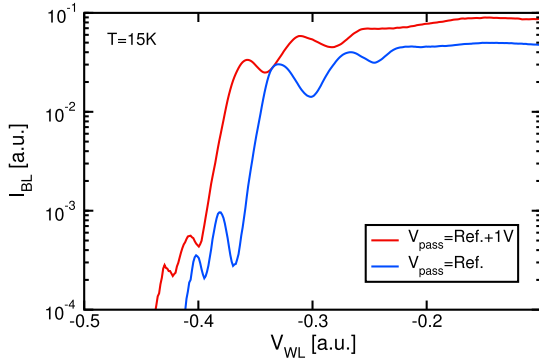

Fig. 10. $I_{BL}-V_{WL}$ trans-characteristic of a cell measured with a low V_{BL} under different V_{pass}, at $T = 15$ K.

Fig. 11. $I_{BL}-V_{WL}$ trans-characteristic of a cell measured with a low V_{BL} in its initial state and after weak and strong program operations, at $T = 15$ K.

Fig. 12. $I_{BL}-V_{WL}$ trans-characteristic of a cell measured with a low V_{BL} at a different T.

voltage (V_{pass}) applied to the unselected cells of the string may nonnegligibly affect the shape of the oscillations. In particular, the impact of V_{pass} on the results occurs through a change in both the saturation current of the string (resistance of the unselected cells) and the low-current region of the $I_{BL}-V_{WL}$ curve (fringing electric fields exerted by the wordlines adjacent to the cell under Read on its channel electrostatics). Fig. 11 highlights, moreover, that oscillations can be clearly observed for different V_T levels of the cell under Read, meaning that their origin is not related to a specific charge state of the cell storage layer. Finally, Fig. 12 demonstrates that oscillations rapidly disappear moving from 15 to 50 K, proving that T has a fundamental role in their phenomenology.

IV. PHYSICAL PICTURE

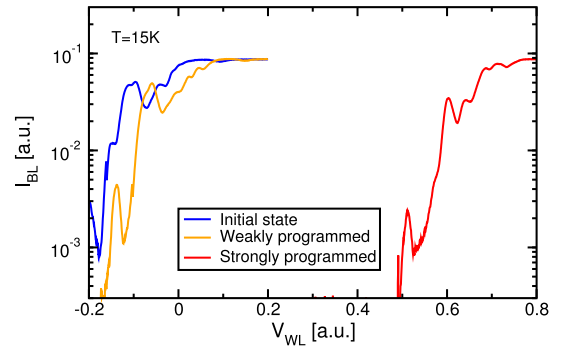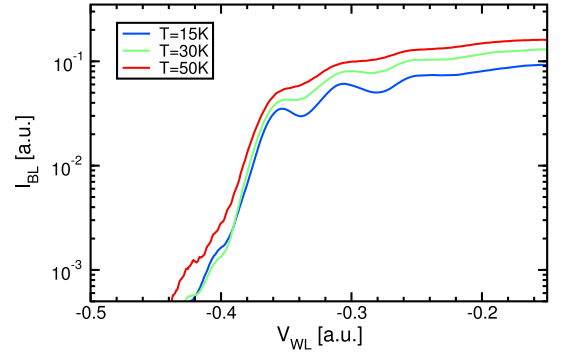The experimental evidence presented in Section III can be explained in terms of a single-electron transistor-like behavior

of the memory cells emerging from their current–voltage curves, when V_{BL} is reduced in the deep-cryogenic regime. The low-conductivity diamonds in Figs. 7 and 9 and the turn-on voltage appearing over the V_{BL} axis for some V_{WL} in Fig. 8 reproduce, in fact, the outcome of Coulomb blockade effects constraining electron transport through cell channel [22]. In this regard, it is worth mentioning that traces of SET-like conduction schemes have been recently detected also on different types of MOSFETs operated at low drain voltage in the deep-cryogenic regime [3], [7], [13], [14]. The origin of those conduction schemes has been attributed to the presence of quantum dots in device channel, exchanging charge carriers with source and drain by tunneling and under the constraints of Coulomb blockade [3], [7], [13], [14].

In the case of 3-D NAND Flash memories, the decrease in T down to the deep-cryogenic regime may give rise to quantum dots in cell channel as a result of the strengthening of the nonuniformities in channel inversion created by spatially localized trapped charge in different regions of the device. To address this point, we referred to the case of electrostatic nonuniformities in cell channel created by polysilicon grain boundaries [18], [23], [24], [25]. Through a commercial tool for device simulation [26], we carried out TCAD analyses of channel inversion and current transport on a template NAND string implementing polysilicon grain boundaries with a high-density of trap states (see [27], [28], [29] for string parameters and [25] for trap parameters). In the simulations, electron transport was modeled as a mix of intra-grain
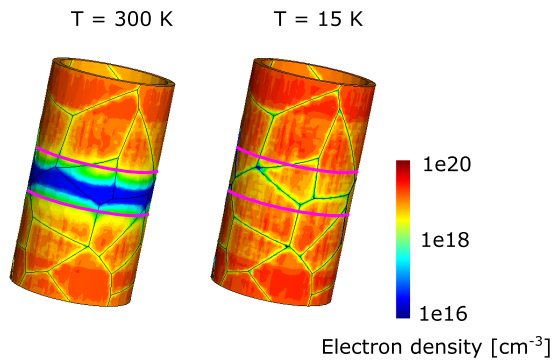
Fig. 13. TCAD simulation results showing the electron density at the surface of the investigated template 3-D NAND string at $T = 300$ K and 15 K, under the same Read conditions but with V_{WL} leading to equal I_{BL}. The magenta lines delimit the position of the wordline of the cell under Read.
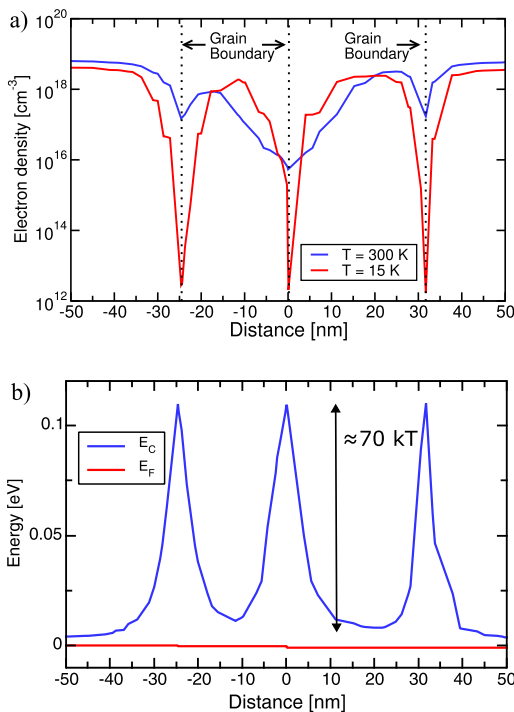

Fig. 14. Simulation results for (a) electron concentration at $T = 300$ and 15 K and (b) E_C and E_{Fn} at $T = 15$ K along a cut of the 3-D NAND string taken in the source-to-bitline direction.

drift–diffusion (mechanism I), inter-grain thermionic emission (mechanism II), and tunneling through the energy barriers created by grain boundaries (mechanism III). Fig. 13 shows that, at constant I_{BL}, the reduction of T from 300 to 15 K strongly modifies the inversion profile in the channel region of the cell under Read. In particular, the decrease in T makes channel inversion stronger in the intragrain regions and much weaker at the grain boundaries. This can also be clearly seen from Fig. 14(a), where a cut along the longitudinal string direction is considered. In this figure, the ratio between the electron concentration in the intragrain regions and at the grain boundaries is shown to increase by orders of magnitude when moving from $T = 300$ to 15 K. This effect can be traced back to quantum-mechanical tunneling becoming the dominant transport mechanism through the grain boundaries of the polysilicon channel in the deep-cryogenic regime. Note,
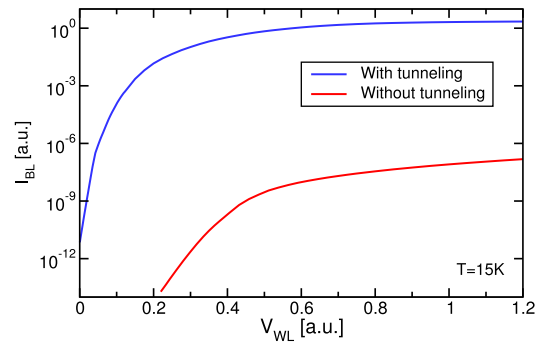

Fig. 15. Simulated I_{BL} versus V_{WL} curve of the investigated template NAND string with and without the tunneling contribution through the energy barriers created by the polysilicon grain boundaries, at $T = 15$ K. Note that, differently from the experimental results reported in Section III, no oscillations appear from the curves since the impact of Coulomb blockade on electron transport between adjacent polysilicon grains is not accounted for.

in fact, that the reduction of T would result in a general decrease in the electron concentration both in the intragrain regions and at the grain boundaries at constant V_{WL}, leading to a reduction of I_{BL}. To reach the same I_{BL}, as assumed in Figs. 13 and 14(a), V_{WL} must be increased to compensate for that decrease in the electron concentration. The increase in V_{WL} is what makes the inversion in the intragrain regions stronger at $T = 15$ K than at 300 K. Inversion at the grain boundaries at the former T, instead, remains much weaker than at the latter because the dominant transport mechanism through the energy barriers created by the grain boundaries switches from thermionic emission to tunneling. This allows to reach the selected I_{BL} even with an electron concentration at the grain boundary positions that is much lower at $T = 15$ K than at 300 K. This point is proved by the fact that the energy barriers at the grain boundaries remain much higher than the thermal energy kT at $T = 15$ K, as shown in Fig. 14(b). This means that the electron concentration at those positions cannot be involved in the dominant transport mechanism through the device. A further proof of that is given in Fig. 15, where the I_{BL} versus V_{WL} relation at $T = 15$ K simulated accounting for quantum-mechanical tunneling is much higher than the curve neglecting it.

The simulation results presented in Figs. 13–15 point out that the intragrain regions in the polysilicon channel of 3-D NAND cells turn into quantum dots isolated by tunneling barriers in the deep-cryogenic regime. This is a possible reason why SET-like conduction schemes emerge from the cell electrical characteristics in that regime. The small dimension of the polysilicon grains makes, in fact, their charging energy comparable or larger than kT at deep-cryogenic T. This makes, in turn, the transfer of electrons between adjacent grains subjected to the constraints of Coulomb blockade, giving rise to the SET-like transport schemes. Within this picture, the relevant variability in the phenomenology of oscillations in the $I_{BL}-V_{WL}$ trans-characteristic of the memory cells observed in Section III may be attributed to the haphazardness in the landscape of quantum dots in the string polysilicon channel.

As a final remark, it is worth mentioning that attributing the quantum-dot behavior of cell channel to polysilicon grains is just a first attempt to explain the SET-like behavior appearing

in the electrical characteristics of 3-D NAND cells in the deep-cryogenic regime. This attempt will need further modeling efforts and a more detailed comparison between simulation and experimental results, which are beyond the scope of this article. At the present stage, however, other possible origins of the phenomenon, e.g., related to impurities or trapped charge in positions other than polysilicon, should not be fully excluded.

V. CONCLUSION

In this article, we reported the first analysis of the operation of the 3-D NAND Flash technology in the deep-cryogenic regime. Clear experimental evidence was provided showing that SET-like conduction schemes emerge from the cell current–voltage characteristics in that T regime, when V_{BL} is reduced. A physical picture explaining the phenomenon was proposed, based on nonuniform channel inversion giving rise to a landscape of isolated quantum dots, where electron transport is impacted by the Coulomb blockade. The results represent a first step toward new potential applications of 3-D NAND Flash memories.

ACKNOWLEDGMENT

REFERENCES

[1] R. Maurand et al., "A CMOS silicon spin qubit," *Nature Commun.*, vol. 7, no. 1, Nov. 2016, Art. no. 13575, doi: 10.1038/ncomms13575.

[2] M. Vinet et al., "Towards scalable silicon quantum computing," in *Proc. 76th Device Res. Conf. (DRC)*, Jun. 2018, pp. 1–2, doi: 10.1109/DRC.2018.8442198.

[3] S. Bonen et al., "Cryogenic characterization of 22-nm FDSOI CMOS technology for quantum computing ICs," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 127–130, Jan. 2019, doi: 10.1109/LED.2018.2880303.

[4] A. M. J. Zwerver et al., "Qubits made by advanced semiconductor manufacturing," *Nature Electron.*, vol. 5, no. 3, pp. 184–190, Mar. 2022, doi: 10.1038/s41928-022-00727-9.

[5] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018, doi: 10.1109/JSSC.2017.2737549.

[6] M. F. Gonzalez-Zalba, S. de Franceschi, E. Charbon, T. Meunier, M. Vinet, and A. S. Dzurak, "Scaling silicon-based quantum computing using CMOS technology," *Nature Electron.*, vol. 4, no. 12, pp. 872–884, Dec. 2021, doi: 10.1038/s41928-021-00681-y.

[7] S. K. Singh, D. Sharma, R. A. Vega, and A. Dixit, "Compact model of a bulk FinFET quantum dot toward single chip integration of qubits and control electronics for quantum computing applications," *IEEE Trans. Electron Devices*, vol. 70, no. 6, pp. 2911–2918, Jun. 2023, doi: 10.1109/TED.2023.3265943.

[8] Y. Aiba et al., "Bringing in cryogenics to storage: Characteristics and performance improvement of 3D Flash memory," in *Proc. IMW*, May 2021, pp. 1–4, doi: 10.1109/IMW51353.2021.9439594.

[9] T. Sanuki et al., "Cryogenic operation of 3-D flash memory for storage performance improvement and bit cost scaling," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 7, no. 2, pp. 159–167, Dec. 2021, doi: 10.1109/JXCDC.2021.3123783.

[10] H. Tanaka et al., "Toward 7 bits per cell: Synergistic improvement of 3D flash memory by combination of single-crystal channel and cryogenic operation," in *Proc. IMW*, May 2022, pp. 1–4, doi: 10.1109/IMW52921.2022.9779301.

[11] H. Bohuslavskyi et al., "Cryogenic subthreshold swing saturation in FD-SOI MOSFETs described with band broadening," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 784–787, May 2019, doi: 10.1109/led.2019.2903111.

[12] A. Beckers, F. Jazaeri, and C. Enz, "Theoretical limit of low temperature subthreshold swing in field-effect transistors," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 276–279, Feb. 2020, doi: 10.1109/LED.2019.2963379.

[13] T.-Y. Yang, A. Ruffino, J. Michniewicz, Y. Peng, E. Charbon, and M. F. Gonzalez-Zalba, "Quantum transport in 40-nm MOSFETs at deep-cryogenic temperatures," *IEEE Electron Device Lett.*, vol. 41, no. 7, pp. 981–984, Jul. 2020, doi: 10.1109/LED.2020.2995645.

[14] S. P. Tripathi et al., "Characterization and modeling of quantum dot behavior in FDSOI devices," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 600–610, 2022, doi: 10.1109/JEDS.2022.3176205.

[15] M. Toledano-Luque et al., "Statistical spectroscopy of switching traps in deeply scaled vertical poly-Si channel for 3D memories," in *IEDM Tech. Dig.*, Dec. 2013, pp. 21.3.1–21.3.4, doi: 10.1109/IEDM.2013.6724676.

[16] A. Goda, C. Miccoli, and C. Monzio Compagnoni, "Time dependent threshold-voltage fluctuations in NAND flash memories: From basic physics to impact on array operation," in *IEDM Tech. Dig.*, Dec. 2015, pp. 14.7.1–14.7.4, doi: 10.1109/IEDM.2015.7409699.

[17] A. Ghetti, C. Monzio Compagnoni, A. S. Spinelli, and A. Visconti, "Comprehensive analysis of random telegraph noise instability and its scaling in deca–nanometer flash memories," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1746–1752, Aug. 2009, doi: 10.1109/TED.2009.2024031.

[18] D. Resnati et al., "Characterization and modeling of temperature effects in 3-D NAND flash arrays—Part I: Polysilicon-induced variability," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3199–3206, Aug. 2018, doi: 10.1109/TED.2018.2838524.

[19] G. Nicosia et al., "Characterization and modeling of temperature effects in 3-D NAND flash arrays—Part II: Random telegraph noise," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3207–3213, Aug. 2018, doi: 10.1109/TED.2018.2839904.

[20] C. Monzio Compagnoni and A. S. Spinelli, "Reliability of NAND flash arrays: A review of what the 2-D–to–3-D transition meant," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4504–4516, Nov. 2019, doi: 10.1109/TED.2019.2917785.

[21] G. Malavena, M. Giulianini, L. Chiavarone, A. S. Spinelli, and C. Monzio Compagnoni, "Random telegraph noise intensification after high-temperature phases in 3-D NAND flash arrays," *IEEE Electron Device Lett.*, vol. 43, no. 4, pp. 557–560, Apr. 2022, doi: 10.1109/led.2022.3154432.

[22] R. Waser, *Nanoelectronics and Information Technology.*, Berlin, Germany: Wiley-VCH, 2012.

[23] R. Degraeve et al., "Statistical poly-Si grain boundary model with discrete charging defects and its 2D and 3D implementation for vertical 3D NAND channels," in *IEDM Tech. Dig.*, Dec. 2015, pp. 5.6.1–5.6.4, doi: 10.1109/IEDM.2015.7409636.

[24] C.-W. Yang and P. Su, "Simulation and investigation of random grain-boundary-induced variabilities for stackable NAND flash using 3-D Voronoi grain patterns," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1211–1214, Apr. 2014, doi: 10.1109/TED.2014.2308951.

[25] A. Mannara, G. Malavena, A. S. Spinelli, and C. Monzio Compagnoni, "A comparison of modeling approaches for current transport in polysilicon-channel nanowire and macaroni GAA MOSFETs," *J. Comput. Electron.*, vol. 20, no. 1, pp. 537–544, Feb. 2021, doi: 10.1007/s10825-020-01598-z.

[26] *TCAD Sentaurus Device*, Synopsys, Mountain View, CA, USA, 9th ed., 2017.

[27] G. Malavena, A. L. Lacaita, A. S. Spinelli, and C. Monzio Compagnoni, "Investigation and compact modeling of the time dynamics of the GIDL-assisted increase of the string potential in 3-D NAND flash arrays," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2804–2811, Jul. 2018, doi: 10.1109/TED.2018.2831902.

[28] G. Malavena, A. Mannara, A. L. Lacaita, A. Sottocornola Spinelli, and C. Monzio Compagnoni, "Compact modeling of GIDL-assisted erase in 3-D NAND flash strings," *J. Comput. Electron.*, vol. 18, no. 2, pp. 561–568, Jun. 2019, doi: 10.1007/s10825-019-01328-0.

[29] M. Giulianini, G. Malavena, C. Monzio Compagnoni, and A. S. Spinelli, "Time dynamics of the down-coupling phenomenon in 3-D NAND strings," *IEEE Trans. Electron Devices*, vol. 69, no. 12, pp. 6757–6762, Dec. 2022, doi: 10.1109/TED.2022.3217718.