Complex Design of CMOS Logic With Tolerance to Particle and Cumulative Radiation

Minwoong Lee

***Abstract*— Silicon-based electronic components exposed to the radiation environment experience transient and cumulative damage, which causes performance degradation, malfunction, and burnout of the entire electronic system. In this study, the silicon-on-insulator (SOI) process technology was applied to enhance the single event effect (SEE) tolerance of bulk complementary metal–oxide–semiconductor (CMOS)-based logic circuits, which are vulnerable to space particle radiation. SOI CMOS processes are susceptible to total ionizing dose (TID) effects because of an additional oxide layer. A layout-modification technique (LMT) was proposed to overcome this problem. The SEE tolerance characteristics of the SOI process logic were verified in advance using radiation response modeling and simulation. The proposed radiation-hardened (RH) SOI CMOS logic was designed and implemented on a chip using a 0.5-μm CMOS test process. Radiation tests were conducted on the proposed logic chip to validate its SEE resistance to 50- and 25-MeV proton particles and its tolerance to TID effects for a total dose of 15-kGy(Si) gamma rays. The proposed SOI CMOS logic with the LMT can mitigate the atypical effects caused by radiation particles in semiconductor devices in radiation environments, such as space and nuclear power plants, thereby ensuring sufficient survival time under cumulative effects.**

***Index Terms*— Gamma ray, layout modification technique (LMT), proton particle, radiation particle, radiation tolerance, silicon-on-insulator (SOI), single event effect (SEE), total ionizing dose (TID) effects.**

I. Introduction

COMPLEMENTARY metal–oxide–semiconductor (CMOS) devices are exposed to various types of radiation in space environments and a flux of charged particles [approximately 85% protons, 14% alpha particles (helium), and 1% heavy ions] in Earth's magnetosphere, which can cause damage. These radiation particles can induce single event effects (SEEs) in semiconductors. Among the types of SEEs, a single event upset (SEU) is caused by undesirable charge collection owing to radiation, resulting in digital circuit errors or soft errors, where the intended states of 0 and 1 are flipped. A single event latch-up (SEL) occurs because of the momentary generation of charged particles, leading to changes in energy levels and causing overcurrent in a semiconductor. This results in permanent damage or hard errors, such as burnout. A total ionizing dose (TID) effect involves the accumulation of positive charges generated by radiation in a metal–oxide–semiconductor structure, and these charges are trapped at a silicon–oxide interface. This can lead to performance degradation and malfunctions, ranging from electronic device performance degradation to failure. These atypical phenomena are crucial factors that determine the lifespan of electronic equipment used in space, particularly for high-cost satellites utilized in long-duration missions. In an actual space radiation environment, electronic devices are simultaneously exposed to two main forms of radiation, i.e., SEEs and TID effects. Consequently, considering the current global situation faced by the space industry, it is imperative to conduct research on radiation hardening to address these issues and prevent critical problems [1], [2], [3].

The silicon-on-insulator (SOI) process technology is employed to reduce the damage caused by SEEs in bulk CMOS logic. SOI CMOS devices are used in high-performance and low-power applications owing to their low leakage current, low threshold voltage, high switching speed, and low power consumption. Additionally, a buried oxide (BOX) layer in the middle of a silicon wafer in SOI CMOS devices mitigates particle-induced effects by blocking the ion track path that is created when radiation particles penetrate silicon. However, the addition of a BOX layer to insulating oxide films in the existing bulk CMOS processes makes them vulnerable to TID effects, where unexpected charges become trapped in the films. In particular, n-type metal–oxide–semiconductor field-effect transistors (MOSFETs) are structurally susceptible to TID effects. To overcome this, a layout modification technique (LMT) is applied to prevent trapped charges from reaching the oxide film. This technique is applicable in the widely used CMOS process without constraints, such as additional circuit or logic (which can result in a decrease in speed or increase in area) or process masks [4], [5].

In this study, the impact of the SEE caused by proton particles in space radiation was modeled for bulk and SOI CMOS logic. Radiation tolerance was predicted by simulating

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The author is with the Korea Atomic Energy Research Institute, Deajeon 34057, South Korea (e-mail: minwoong@kaeri.re.kr).

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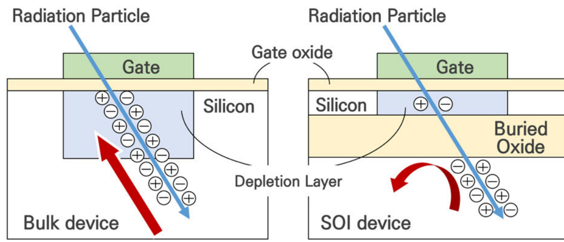

Fig. 1. Effects of particle radiation on SOI and bulk device structures.

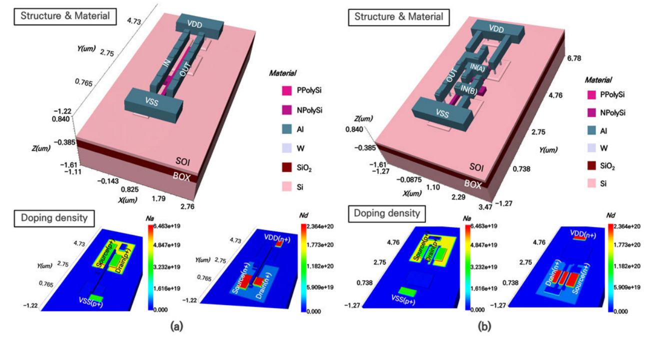

Fig. 2. Three-dimensional characteristic model of radiation-tolerant SOI CMOS logic. (a) Inverter and (b) NAND.

the changes in the electrical characteristic of the logic due to particle interactions. An LMT was applied during the SOI process design phase for chip fabrication to mitigate TID effects. The fabricated chips were subjected to SEE (proton beam) and TID (gamma ray) testing to analyze and validate their tolerance characteristics.

II. Modeling and Simulation of Radiation Particle Effect in CMOS Logic

A. SEE-Induced Transient Damage and Its Mitigation

A semiconductor device operates by precisely controlling the movement of charges within the device. Radiation particles can generate instantaneous undesirable charges within an electronic circuit, leading to the formation of ionized charge tracks. Radiation particles can simultaneously occur across the entire area. The simultaneous occurrence of current pulses at numerous locations within complex electronic circuits can have different effects on the circuits or final output. Therefore, devices and circuits must be analyzed to understand these effects. SEUs and SELs are two significant issues, and unlike recoverable soft errors (SEUs) in logic or memory, SELs can induce irreversible hardware failures, such as a burn-out [6], [7], [8], [9].

Various resistance and mitigation techniques are being investigated to address the SEE (SEUs and SELs) in semiconductors caused by radiation particles, which can lead to excessive damage. These techniques include materials, processes, and circuitry/system-level approaches [10]. This study employs a robust technology based on SOI wafers, which are resistant to the particle-induced SEE. As shown in Fig. 1, SOI-based devices contain a structure, where a silicon layer is placed on top of a BOX layer. Compared to bulk processes based on silicon, this configuration provides a smaller responsive volume to radiation and a reduced amount of charge collection along particle trajectories, resulting in enhanced tolerance to the SEE.

In this study, CMOS logic was designed using the SOI process by utilizing the high resistance of the depletion layer caused by the BOX layer to enhance the resistance to SEUs and SELs [11], [12].

B. Three-Dimensional Model and Design of SEE-Tolerant SOI Logic

The SOI process is resistant to particle radiation, and it can be classified into two types on the basis of the thickness of the silicon body, which is the channel region: partially depleted (PD) and fully depleted (FD). In the PD SOI process, the thicknesses of the silicon body and BOX layer are 50–90 nm and 100–200 nm, respectively. As the thickness of the silicon body is larger than that of the adjacent silicon depletion region in the channel, it is not FD, resulting in the presence of a floating charge region. This region reduces the potential barrier of the channel, allowing more current to flow through the channel. The current increases owing to the floating-body effect; this is known as the kink effect [13]. The technique to reduce this problem is discussed in Section III-A.

In this study, CMOS logic circuits were fabricated using the PD SOI process, which was relatively easy to implement, to evaluate the SEE tolerances of the bulk and SOI processes. Prior to the fabrication process, the 3-D modeling of the SOI process logic (inverter and NAND) was performed to simulate radiation particle damage and compare the tolerance. The 3-D characteristic model of the SOI CMOS logic was designed by optimizing the size, power supply voltage, layer composition, and other factors to examine the simulation time. The 3-D structure was formed by adjusting the size and concentration of the silicon, oxide, and doping regions in a 0.18-μm CMOS SOI process. The geometry information and doping concentration used in the 3-D characteristic model of the SOI CMOS logic are summarized in Table I. Fig. 2 shows the 3-D model of the radiation-tolerant SOI CMOS logic. The functional simulation results of the SOI logic model confirmed the signal inversion functionality of the inverter and the correct output of 0 from the NAND logic when inputs A and B were high.

C. SEE Tolerance Mechanism in CMOS Logic

New mechanisms were established for the SEU and SEL caused by radiation particles in the bulk and SOI processes by considering current and resistance components. In conventional bulk CMOS processes, the current gain (β) of structurally formed parasitic transistors (p-n-p and n-p-n) and the resistance between their base emitters play important roles. An SEL occurs when there is a significant change in charge due to a large variation in current at the bases of these transistors, specifically when a substantial amount of charge are generated by radiation particles.

In Fig. 3, the resistances (R_{DP1}, R_{DP2}, and R_{DP3}) of the depletion regions are infinite in the normal state; thus, the parasitic transistors are nonfunctional. However, in CMOS

TABLE I
GEOMETRY AND DOPING PROFILE OF 3-D CHARACTERIZATION MODEL OF RADIATION-TOLERANT SOI CMOS LOGIC

Parameter	SOI CMOS Logic Geometry	
	n-MOSFET	p-MOSFET
Width/Length [um/um]	0.5/0.18	1/0.18
Body thickness [um]	1	1
BOX thickness [um]	0.2	0.2
SOI thickness [um]	0.1	0.1
Gate oxide thickness [nm]	3.3	3.3
Sidewall oxide thickness [um]	0.1	0.1

Parameter	SOI CMOS Logic Doping Density [#/cm^3]			
	n-MOSFET		p-MOSFET	
Drain&Source	n+	1×10^{20}	p+	6×10^{19}
Body	p+	1×10^{15}	p+	1×10^{15}
Channel	p+	1.12×10^{17}	n+	1.55×10^{17}
Well	p+	1×10^{17}	n+	1×10^{17}

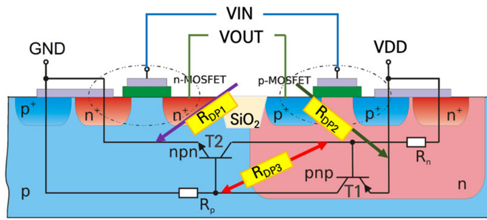

Fig. 3. Depletion resistance and radiation particle paths in bulk CMOS structure.

bulk processes, the paths through which radiation particles enter can significantly reduce these resistances.

In the first case, when the input of the inverter is 1, if a radiation particle enters the p-substrate from the drain (GND), R_{DP1} gradually decreases from ∞. This causes momentary current and can potentially lead to an SEU. However, the drain has VDD voltage when the input of the inverter is 0. This gradually increases the base voltage of parasitic transistor T2. An SEL is triggered when a certain threshold of momentary current is reached and T2 is turned on.

In the second case, when the input of the inverter is 0, if a radiation particle enters the n-well (VDD) from the p-MOSFET drain (VDD), R_{DP2} gradually decreases from ∞. This causes momentary current and may lead to an SEU. However, when the input of the inverter is 1, the p-MOSFET drain has GND voltage. The resistance decreases owing to the particles in the R_{DP2} path, and the generated momentary current reduces the base voltage (VDD) of parasitic transistor T1. If this reduction is sufficiently large to turn T1 on, it can trigger an SEL through the positive feedback of the two parasitic transistors.

When particles enter between the n-well (VDD) and p-substrate (GND), R_{DP3} gradually decreases, causing a voltage variation at the base of either T1 or T2. An SEL occurs if T1 or T2 is turned on, resulting in excessive current flow. In the case of actual CMOS processes on a p-substrate, the n-well resistance (Rn) is several tens of kilohms, and the p-substrate resistance (Rp) is several tens of megaohms. Considering this, if R_{DP3} decreases from ∞ to several tens of megaohms, the voltage distribution causes the turn-on voltage to be first applied to the base of T2. As a result, the base of T1 decreases to GND, causing current to flow until the power supply is cut off.

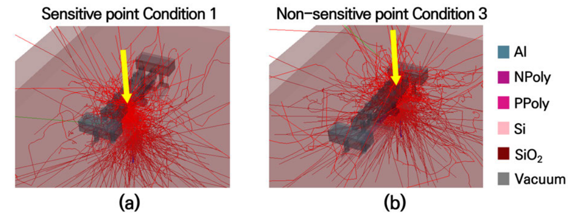

Fig. 4. Proton particle injection model of CMOS bulk inverter. (a) Condition 1. (b) Condition 3 (50 MeV, beam on 10 000).

Therefore, although the R_{DP3} path can be considered as the most sensitive path, the location and angle of radiation particle incidence are probabilistic, making an SEL extremely unlikely. Furthermore, in current semiconductor processes, the amplification parameter (β) of current ($I_C = \beta I_B$) due to an SEL is designed to be less than 1. Consequently, research on semiconductor damage caused by radiation particles focuses on SEUs rather than SELs.

The radiation-hardened (RH) SOI process exhibits strong resistance to SEEs owing to its extremely small silicon volume capable of generating electron–hole pairs (EHPs) upon radiation particle incidence. In addition, the charge generation energy of SiO_2 (17 eV) is significantly higher than that of EHPs (3.6 eV) in silicon. Furthermore, from the perspective of the depletion resistance caused by the junction structure mentioned earlier, the junction region of the SOI process can be neglected. As there is no conventional n-well or p-substrate, resistances Rn and Rp are almost 0 Ω. Therefore, an SEE can occur only if the resistance, which is almost infinite between the n or p channels and p-substrate, decreases to a few ohms because of momentary current. This demonstrates the radiation-induced SEU and SEL tolerance characteristics of the SOI process.

D. Modeling and Simulation of Radiation Particle Injection in SOI Logic

The radiation damage in the CMOS bulk logic was predicted by creating a model that incorporated radiation-induced physical responses including ionizing track paths involving secondary particles. A radiation injection model was specifically developed for the 3-D model of a standard bulk CMOS logic inverter, considering the most dominant proton particles in space radiation. A sensitive point (SP) was anticipated by fixing the bias conditions of the logic in a vulnerable state and conducting layout analysis. We performed the modeling for different incidence positions, i.e., the p-cell source (condition 1), n-cell drain (condition 2), and n-cell source (condition 3), with a particle incidence angle of 90°. Proton energies of 25–100 MeV were modeled according to the conditions of a proton beam facility for subsequent measurements. An energy of 50 MeV [14] was used for SP prediction simulations, and the resulting SP was simulated to assess the extent of damage for each energy level. Fig. 4 presents an example of the proton injection model for a representative CMOS inverter.

The Gseat module (Cogenda) was used for radiation injection modeling and simulation. This tool incorporated Geant4

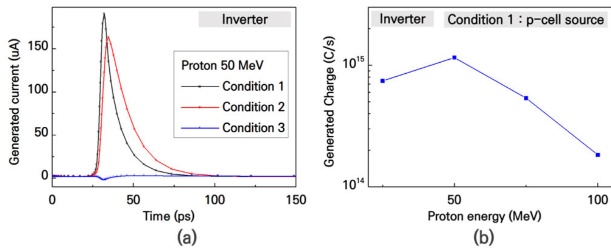

Fig. 5. CMOS inverter logic simulation results. (a) Change in electrical properties for each proton particle condition. (b) Charge generated at different proton energies.

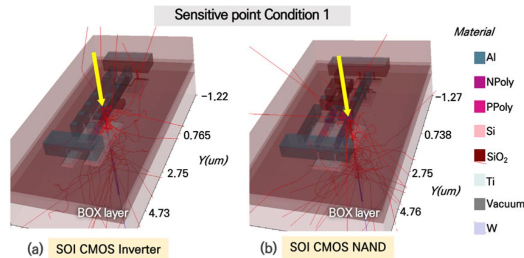

Fig. 6. Proton particle injection model on radiation-tolerant SOI process. (a) Inverter. (b) NAND (50 MeV, condition1, beam on 1000).

for the physical interpretation of particle radiation. Particle radiation and injection simulations were performed using the logic, and the conditions with a high cross section (number of events/fluence) for proton interaction were determined, specifically the conditions that resulted in the highest instantaneous current [15].

The operational state of the logic was defined by the supplied power, i.e., VDD (source of p-type cells), VSS (source of n-type cells), and the output (drain of n-type and p-type cells) that was always in the HIGH state. Initially, simulations were conducted by injecting identical 50-MeV protons into the inverter at each position. The resulting SEE was characterized by instantaneous voltage and current variations. Fig. 5(a) illustrates that the source position of the pMOS cell, specifically condition 1, was the most vulnerable point. Furthermore, simulations were performed to examine the variation in electrical characteristics caused by the proton energy at SP condition 1. The inverter logic exhibited a peak momentary current of approximately 0.19 mA, which corresponded to the highest amount of charge generated by the SEE at 50 MeV, as shown in Fig. 5(b).

The simulation results showed that the damage level at different energies increased in the order of 50, 25, 75, and 100 MeV. This was attributed to the overall structural considerations, including the doping state of impurities inside the silicon semiconductor, material characteristics of the metal, polymer, and contact, and secondary particle effects resulting from proton–particle reactions. In Fig. 6, the SOI process logic represents a structure where the actual semiconductor active region is confined within the SOI layer, which has a thickness of 140 nm. This indicated that the volume available for proton particles to transfer energy was extremely small. Additionally, the BOX layer effectively blocked the ion-track path from reaching the p-substrate, thereby providing a protective barrier.

To verify the radiation tolerance of the digital logic implemented with the SOI semiconductor structure, simulations

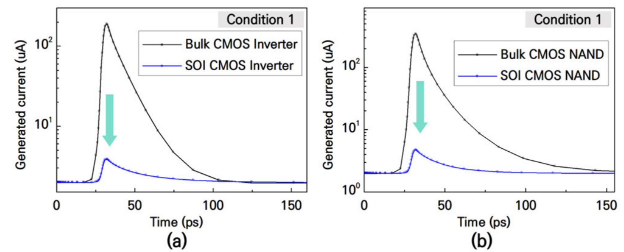

Fig. 7. Simulation results of change in electrical characteristics caused by proton particles in CMOS bulk and SOI logic. (a) Inverter and (b) NAND.

were performed under the same conditions as those used for the bulk CMOS logic. The simulation combined a characteristic model that incorporated the design conditions of the semiconductor SOI process with a proton particle injection model designed for the most vulnerable condition (condition 1). The electrical characteristics were analyzed over time.

Fig. 7 shows the simulation results of the SOI inverter and NAND. The momentary current generated by 50-MeV protons was approximately 2 μA. This was approximately 1% of the momentary current generated by the SEE in the conventional bulk inverter ($\sim$194 μA). This implied that, compared to the SEE in the bulk inverter, a significant change in the same circuit would require approximately 97 simultaneous SEEs to occur in the SOI inverter. Similarly, a momentary current of 3.5 μA was generated in the SOI NAND logic, which was approximately 1% of the momentary current generated by the SEE in the conventional bulk NAND logic ($\sim$349 μA).

The results of the radiation-induced particle injection modeling and simulation performed using the conventional bulk CMOS logic provided the worst case condition, in which proton particles in a space radiation environment can have the strongest impact. We validated the improved SEE tolerance of the RH SOI process logic compared to the conventional bulk process under this condition.

III. Fabrication and Radiation Test Results of the Proposed SOI Logic Chip

A. Proposed TID Tolerant LMT for SOI Process

We proposed a new layout structure for MOSFETs to enhance their tolerance to TID effects and minimize the floating-body effect in the PD SOI process. The BOX layer in the SOI structure acts as a barrier against momentary SEEs. However, the oxide (SiO_2) region is susceptible to TID effects owing to the accumulation of ionized charges generated by radiation. This can result in more damage when combined with the TID effects of the isolated oxide in conventional CMOS processes [16], [17]. The layout was modified to mitigate the damage. Fig. 8 shows a body contact (p^+) region introduced within the active region (SOI layer) in the n-MOSFET structure, which was susceptible to TID effects.

Generally, the CMOS process form an isolation oxide layer between components for electrical isolation. However, within this thick oxide layer, TID-induced fixed charges (+) are generated. This charge creates an issue by forming non-ideal leakage current paths between the drain and source

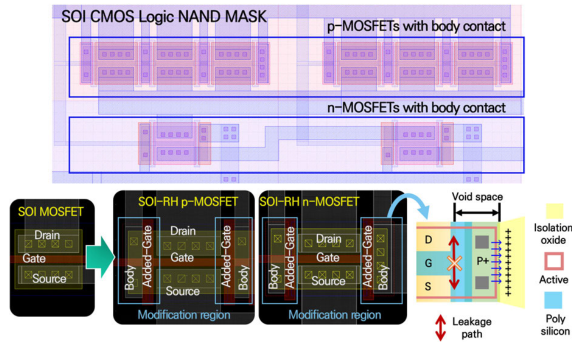

Fig. 8. Layout of the proposed SOI NAND logic with body contact.

TABLE II
CHARACTERISTIC SIMULATION RESULTS OF SOI MOSFETS ACCORDING TO BODY CONTACT

Type	VT implant	Body	V_{th} (V)	I_{dsat} (uA)	V_{BR} (V)
n-type Tsi=140nm Lg=1um	BF2, 80keV, 6×10^{12}	Floating	0.74	667	4.4
		Contact	0.76	635	16
p-type Tsi=140nm Lg=1um	Skip	Floating	0.85	362	11
		Contact	0.87	355	16

of n-MOSFETs. Since this isolation oxide layer is formed in areas excluding the active region, the proposed structure expanded the active region to create a void space between the actual channel and the isolation oxide layer. The p^+ doping of the expanded active region induces stress on the radiation-induced positive charges in the oxide layer to ensure that it has no effect on the transistors.

Additionally, an added-gate poly was included to address the conduction issue between the body (p^+), source, and drain (n^+). The application of this RH LMT to the MOSFET structure in the SOI logic design prevented the SEE damage caused by the BOX layer and improved the tolerance to TID effects. The same approach was applied to the p-MOSFET but with the opposite polarity.

An additional body contact region was designed in the proposed structure to allow for the separate biasing of the body. This addressed the floating-body effect and allowed for the application of a negative voltage to the body, thereby increasing V_{th} and V_{BR}. Fig. 8 illustrates the layout mask drawing of the NAND logic circuit with the proposed MOSFET structure. Table II lists the final conditions for the RH MOSFET in the submicrometer SOI CMOS test process.

An SOI logic chip was fabricated using the proposed mask on a 6-in SOI wafer. The overall mask size was 7 × 7 mm, and it included various test patterns. Individual package chips and a device under test (DUT) board were produced for the radiation testing of each logic, as shown in Fig. 9.

B. Proton-Induced SEE in the Proposed Logic Chip

The SEE tests of the fabricated SOI logic were conducted using the cyclotron at the Jeongeup Advanced Radiation Research Institute (ARTI) [18] and the proton linear accelerator at the Gyeongju Korea Multi-Purpose Accelerator Complex (KOMAC) [19] in South Korea. Proton beams with energies of 25 MeV (test condition 1) and 55 MeV (test condition 2) were utilized. The details of each test condition are presented in Table III.

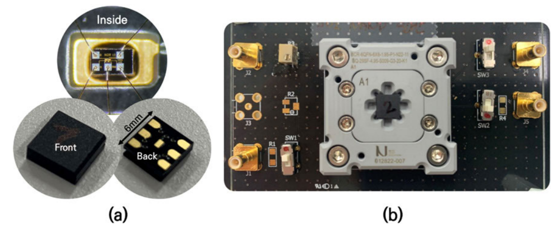

Fig. 9. Proposed SOI CMOS logic chip for radiation test. (a) Package chip and (b) DUT board.

TABLE III
PROTON BEAM TEST CONDITIONS AT FACILITIES

Test Facility	Cyclotron (ARTI) Test condition1	Linear Accelerators (KOMAC) Test condition2
Energy(MeV)	25 MeV	55 MeV
Beam current(uA)	~15uA	0.055 uA
Flux	~5.0×10^{12} pulse/cm^2·s	5.0×10^9 pulse/cm^2·s
Dose	~ 3×10^4 Gy(Si)/s	3×10^1 Gy(Si)/s
Beam Pulse width	2 ms (Duty 20%)	50 us
Beam Frequency	100 Hz	1 Hz
Beam spot	13 mm	30 mm

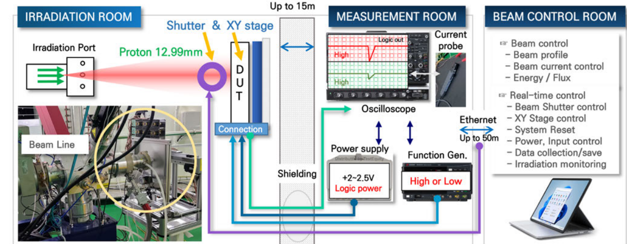

Fig. 10. Configuration diagram of real-time remote control environment of proton beam irradiation test.

Fig. 10 shows the experimental setup in the test performed using the cyclotron under test condition 1 for the real-time measurement of signal variations in the logic chip during proton beam irradiation. The DUT board of the logic chip, which acted as the target for the proton beam, was located in the irradiation room and connected to the measurement control room via a 15-m-long cable. The measurement control room contained equipment to directly measure the analog signals. The measurement and beam control rooms were connected via an Ethernet network, allowing for the real-time acquisition of data for various beam conditions from the beam control room.

An XY stage that could simultaneously measure up to 20 DUTs was employed to overcome the time, cost, and safety limitations associated with individual sample investigations. Considering the characteristics of the beam-irradiation device, which could output 100 beams per second, a single beam control shutter and aluminum shielding film were added in front of the DUT. The XY stage and shutter were controlled from the beam control room, allowing for the repositioning of the test samples. These movements were monitored in real time using network cameras. In the proton beam test of the digital logic chip, the bias conditions were set to maintain the outputs of the inverter and NAND logic in a constant HIGH

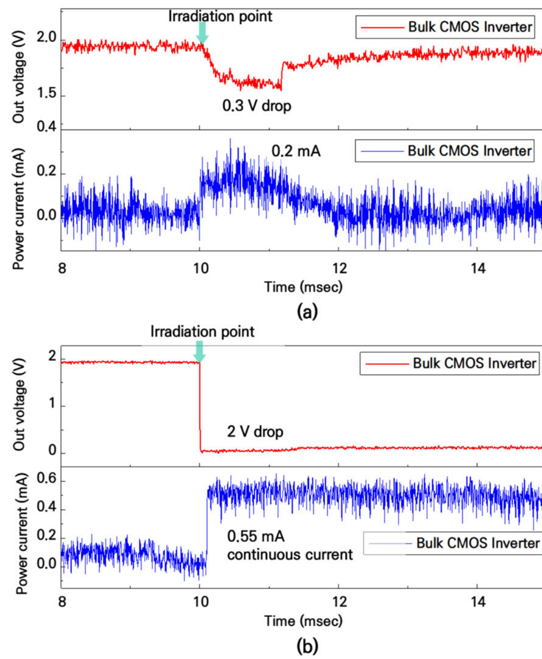

Fig. 11. Test results for bulk CMOS inverter using 25-MeV proton beam irradiation (test condition 1). (a) Flux: 2.5 × 10^{12} p/cm^2·s. (b) Flux: 4 × 10^{12} p/cm^2·s.

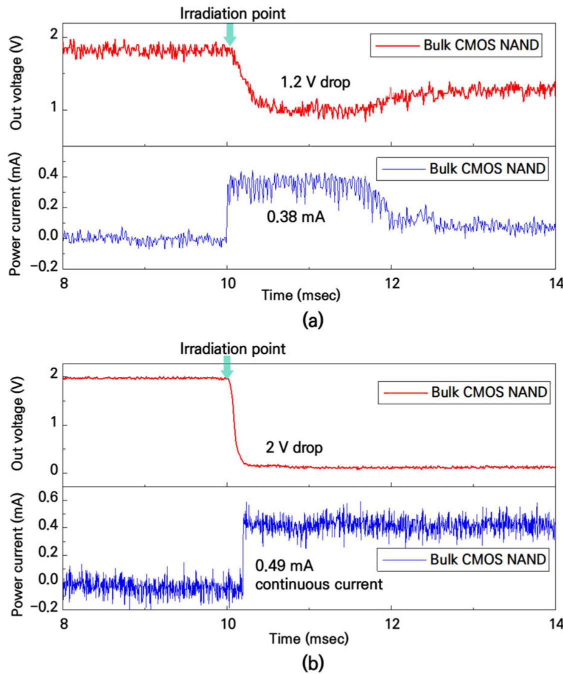

Fig. 12. Test results for bulk CMOS NAND using 25-MeV proton beam irradiation (test condition 1). (a) Flux: 2.8 × 10^{12} p/cm^2·s. (b) Flux: 4 × 10^{12} p/cm^2·s.

(VDD) state. VDD (source of p-type cells) and VSS (source of n-type cells) were supplied, and inputs IN, A, and B were set as LOW.

The results of the proton beam test under test condition 1 are shown in Figs. 11 and 12. The general bulk inverter exhibited an output voltage upset starting from a flux of 2.5 × 10^{12} p/cm^2·s or higher. The output voltage dropped by approximately 0.3 V, resulting in a momentary current of approximately 0.2 mA. The beam current was increased up to 10 μA for the investigation. At a flux of 4 × 10^{12} p/cm^2·s, the momentary current of the power stage increased to approximately 0.55 mA, reaching a sustained state of flow. The previously maintained HIGH output voltage transitioned to LOW during this period. This result represents the initial stage of an SEL, where current is drawn until the power is disconnected. Current can increase if this state persists; this can potentially lead to chip burnout.

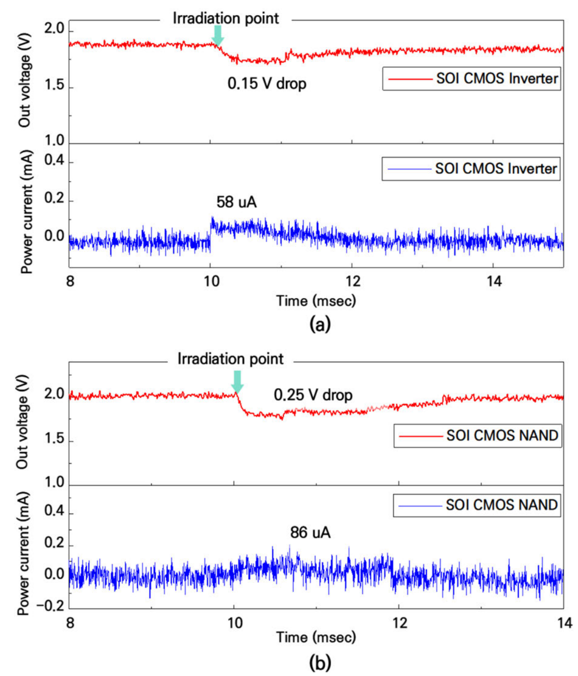

Fig. 13. Test results for the proposed SOI CMOS logic using 25-MeV proton beam irradiation (test condition 1). (a) Inverter, flux: 4.1 × 10^{12} p/cm^2·s. (b) NAND, flux: 4.5 × 10^{12} p/cm^2·s.

Similar trends were observed in the proton beam test results for the general bulk CMOS NAND logic. SEUs were observed at a flux of 2.8 × 10^{12} p/cm^2·s, and the initial SEL state was confirmed at a flux of 4 × 10^{12} p/cm^2·s. The momentary current during the SEL increased with flux, and the initial SEL damage occurred in the digital logic NAND chip when the current exceeded 0.49 mA. The SEU can recover to a normal state after a momentary error. However, the SEL cannot return to a normal state, potentially causing significant damage to the entire system.

Beam tests were performed under test condition 1 to verify the radiation tolerance of the proposed SOI CMOS logic chip, and the results are shown in Fig. 13. The SOI inverter exhibited a decrease of approximately 0.15 V in the output voltage and a slight increase in momentary current to approximately 58 μA, even at a flux of 4.1 × 10^{12} p/cm^2·s. The flux was increased up to 4.5 × 10^{12} p/cm^2·s for the SOI NAND logic.

However, it maintained a normal high logic state with a decrease of only 0.25 V in the output voltage and an increase in the momentary current to 86 μA. Therefore, the proposed SOI CMOS logic ensured radiation tolerance up to a flux of 4.5 × 10^{12} p/cm^2·s [or an equivalent absorbed dose rate of 3 × 10^6 rad(Si)/s] under test condition 1.

The SEE tolerance of the proposed SOI CMOS logic was evaluated by performing tests using the linear accelerator under test condition 2. Although the proton beam energy at

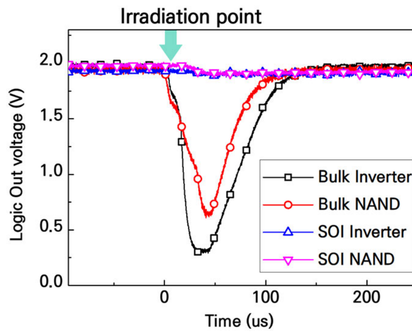

Fig. 14. Test results for bulk CMOS logic using 55-MeV proton beam irradiation (test condition 2) (flux: ~5 × 10^9 p/cm^2·s).

this facility was variable, tests were conducted using 33- and 100-MeV beams to assess the characteristics. However, the logic output was weak or absent. Therefore, based on the existing literature, we observed the changes in the logic output and momentary current of the power stage at the highest SEU cross-sectional energy of 55 MeV [14]. The same environment as that used in test condition 1 was configured to obtain data in real time.

An SEU occurred at a maximum flux of approximately 5.4 × 10^9 p/cm^2·s, where the output voltage dropped by approximately 1.7 V. This was caused by a single-pulse proton beam, as shown in Fig. 14. A momentary current of 0.3 mA was generated during this event, which confirmed the SEU damage characteristic induced by protons. Similar SEUs were observed in the bulk NAND logic, where the output voltage dropped by approximately 1.4 V and a momentary current of approximately 0.28 mA was measured at a beam flux of approximately 4.5 × 10^9 p/cm^2·s. Therefore, the dose required for the occurrence of an SEU for the general bulk CMOS logic under test condition 2 at this linear accelerator facility was estimated to be approximately 4 × 10^9 p/cm^2·s or higher. However, only the occurrence of the SEU was confirmed owing to the difficulty in inducing an SEL under the applied conditions.

In contrast, the SOI inverter exhibited an extremely small output voltage drop of 0.015 V at a maximum flux of approximately 5.4 × 10^9 p/cm^2·s. The momentary current generated during this event was approximately 68 μA. Similarly, the SOI NAND logic maintained its high state with an output voltage drop of 0.02 V and a momentary current of 84 μA at a flux of approximately 5.2 × 10^9 p/cm^2·s. Therefore, the SEE tolerance of the SOI logic was compared to that of the general bulk logic in terms of the occurrence of an SEU under the single-beam condition of 55 MeV, pulsewidth of 50 μs, and flux of approximately 5.4 × 10^9 p/cm^2·s.

The SEE test results showed that under test condition 1, the bulk logic experienced SEUs and SELs because of an increase in the internal momentary current caused by the increase in flux. In contrast, the proposed RH SOI logic exhibited minimal current variation and maintained a normal state. Under test condition 2, the bulk logic experienced SEUs owing to a momentary current of approximately 0.3 mA, whereas the SOI logic showed only slight current fluctuations. The current generated under the same conditions was reduced by approximately 70%–90%; this confirmed the tolerance of the proposed SOI logic to particle radiation. Table IV summarizes the radiation damage and tolerance characteristics of the bulk and SOI process logic for each test condition.

TABLE IV
COMPARISON OF SEE DAMAGE AND TOLERANCE CHARACTERISTICS OF BULK AND SOI LOGIC ACCORDING TO PROTON BEAM CONDITIONS

Beam Test Condition	25 MeV Condition1		55 MeV Condition2
bulk CMOS Logic device			
SEE damage type	Upset	Latch-up	Upset
Beam current [uA]	> 5	> 10	0.055
Flux [p/cm^2·s]	> 2.0×10^{12}	> 2.8×10^{12}	> 5.0×10^9
SOI CMOS Logic device			
SEE damage type	SEE Tolerance (Normal operation)		
Beam current [uA]	> 10		0.055
Flux [p/cm^2·s]	> 4.5×10^{12}		> 5.0×10^9

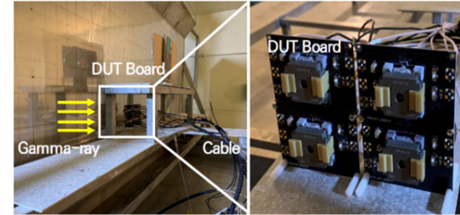

Fig. 15. Test configuration for TID effects for SOI and bulk logic.

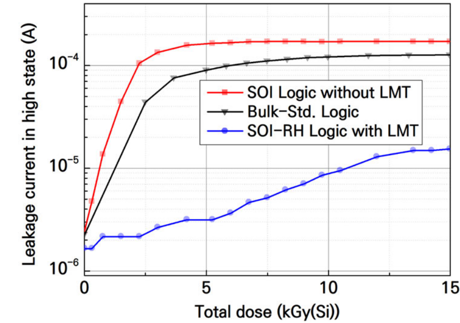

Fig. 16. Leakage current measured at different total cumulative doses for the proposed SOI with LMT and standard bulk logic [15 kGy(Si)].

C. Gamma-Ray-Induced TID Effect in the Proposed SOI Logic Chip

The TID effect test was conducted at the gamma-ray irradiation facility at Jeongeup ARTI. The test environment is shown in Fig. 15. The distance between the cobalt source and DUT board was adjusted to achieve a dose rate of 5 kGy/h(Si), resulting in a total cumulative dose of 15 kGy(Si), where the DUT board and source were located in the test rom. Additionally, the measurement equipment in the test and control rooms was connected using 250m-long cables to measure the electrical characteristics of the logic in real time.

The test results are shown in Fig. 16. The leakage current of the SOI logic without the LMT rapidly increased with the cumulative dose and reached approximately 171 μA. This value was higher than the leakage current of the bulk logic (127 μA). The leakage current increased because of the additional trapped charges in the BOX layer, which could lead to performance degradation and malfunction. The proposed RH SOI logic demonstrated a leakage current of approximately

15.4 μA, which was 91% and 88% lower than that of the SOI logic without the LMT and bulk logic, respectively. Therefore, the survival rate of the chips increased by more than tenfold in the cumulative radiation environment.

IV. Conclusion

The particle-radiation-induced SEE tolerance of SOI CMOS logic was prevalidated using modeling and simulation, and an RH LMT was proposed to mitigate the cumulative radiation-induced TID effect. The proposed RH SOI logic chip with the LMT demonstrated SEE tolerance under proton beam conditions (test conditions 1 and 2). The momentary current generation and output voltage variation improved by up to 90%. Additionally, the proposed RH logic mitigated the TID effects up to a cumulative dose of 15 kGy(Si) through gamma-ray irradiation. Consequently, this study implemented and validated chip design techniques that not only ensured tolerance to particle-radiation-induced SEEs in CMOS logic but also addressed the structural vulnerabilities to TID effects.

Currently, the impact of radiation on semiconductors has a tradeoff relationship between the SEE and the TID effect, and recently, based on simulations, research has been actively conducted on tolerance technologies of these two effects for advanced transistors in nanoscale process [12], [20]. This article proposed a technology that can simultaneously ensure resistance to two types of radiation effects in a submicrometer process that can be fabricated on a chip and verified its feasibility. In the future, we will enhance this technology for application and implementation in advanced transistors. It is essential to ensure versatility in extending the tolerance technology of these transistors to the IC level. To achieve this, we need to develop tolerance design techniques through layout modifications and layer rearrangements without altering the process conditions (materials, doping concentration, and geometry) used in manufacturing high-performance advanced transistors.

These research results can contribute to the development of special purpose electronic systems that can maintain long-term reliability under accumulated and particle radiation in environments, such as nuclear power plants or space.

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