Average Temperature Determination of AlGaN/GaN HEMT Utilizing Pinch-Off Voltage Biasing

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***Abstract*— In this article, pinch-off voltage biasing was utilized for the first time to determine the average channel temperature of the AlGaN/GaN HEMT, which made it possible to exclude the device's electrical parameters dependence in the linear operating mode. The theoretical part is focused on the thermal model with temperature-dependent thermal resistance utilization for active area average temperature determination of the HEMT under quasi-static operation. The experimental part deals with drain-to-source current comparison utilizing quasi-static and pinch-off voltage-biased short-pulse output *I–V* characteristics and additional isothermal trapping phenomena determined from the threshold voltage shift. The appropriate use and combination of methods for the active area average temperature determination utilizing constant isothermal saturation current or short-pulse current were discussed.**

***Index Terms*— AlGaN, average temperature, field effect transistor (FET), gallium nitride (GaN), HEMT, power dissipation, thermal model.**

I. Introduction

THE presence of 2-D electron gas (2DEG) in gallium nitride (GaN)-based structure brings the potential to fabricate high electron mobility transistors (HEMTs) and Schottky diodes employed as excellent devices for application in the microwave and power conversion [1], [2], [3]. High thermal conductance substrates, e.g., silicon carbide (SiC), are utilized to lower operating temperature caused by high power density along the device's active area [4], [5].

Although thermal simulations clear up thermal processes inside the structure, numerous experimental methods were developed to determine the temperature inside and nearby active device areas like Raman spectroscopy or interferometric mapping [6], [7] where special test assemblies are usually required. Various methods taking advantage of specific electro-thermal device properties are utilized [8], [9], [10], [11].

The HEMT average temperature determination methods are based on drain-to-source current comparison acquired by investigated pulsed or quasi-static process and short-pulsed operation at various ambient temperatures [11], [12]. Other methods employ temperature dependence of major device electric parameters like the source resistance and threshold voltage [10], additionally saturation velocity and electron gas concentration.

The introduced method employs pinch-off voltage biasing possibly to be applied to field effect transistor (FET) to reduce drain-to-source pulsed current part [8] to avoid determination of device electrical parameters dependencies in linear operating regime [10] or to eliminate device overheating in saturation operating regime [11]. A short drain–source voltage pulse superimposed to dc pinch-off voltage is utilized to incorporate pinch-off area length and leakage current variation. Additional trapped charge influence in the saturation operating regime is possible to be included as demonstrated in the experimental part. The obtained results are supportive of the consolidation of methodologies utilizing drain-to-source current comparison and major device electric parameters.

II. Theory

The theoretical part is focused on the FET operating under applied drain–source voltage V_{DS}, gate–source voltage V_{GS}, and drain-to-source current I_{DS} resulting in power dissipation $P = V_{DS}I_{DS}$ at ambient temperature T_0 and active area average temperature T_A. Output I–V characteristics and corresponding T_A versus P dependencies obtained for the same V_{GS} are shown in Figs. 1 and 2, respectively. Quasi-static V_{DS} application at $T_0 = T_{00}$ brings I–V characteristics (green solid curve)

Manuscript received 28 July 2023; accepted 14 September 2023. Date of publication 2 October 2023; date of current version 24 October 2023. This work was supported in part by the Electronics Components and Systems for European Leadership Joint Undertaking (ECSEL) JU through Project 5G_GaN2 under Grant 783274; and in part by the Projects 1/0733/20 of Vedecká Grantová Agentúra (VEGA) Grant Agency and APVV-21-0365 of Slovak Research and Development Agency through the Ministry of Education, Science, Research and Sport of the Slovak Republic. The review of this article was arranged by Editor S. Choi. *(Corresponding author: M. Florovič.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3317811.

Digital Object Identifier 10.1109/TED.2023.3317811

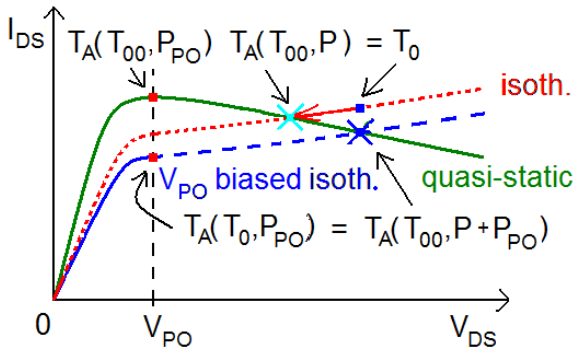

Fig. 1. FET quasi-static measured (green solid curve), zero biased isothermal (red dashed curve), and V_{PO}-biased isothermal (blue dashed curve) output I–V characteristics at the same V_{GS}. The intersections correspond to operating points at depicted active area average temperature T_A.

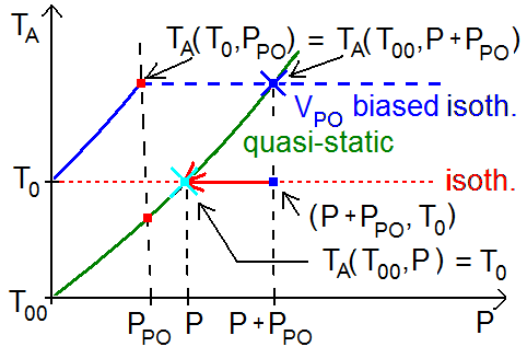

Fig. 2. FET active area average temperature T_A versus dissipated power P dependencies and intersections corresponding to the output I–V characteristics depicted in Fig. 1.

exhibiting pinch-off voltage V_{PO} depicted in Fig. 1 resulting in power dissipation and T_A increase (green solid curve) as shown in Fig. 2. On the other hand, the isothermal I–V characteristic (red dashed curve) in Fig. 1 can be obtained by short-pulsed zero biased V_{DS} application corrected by isothermal trapped charge contribution mentioned in experimental part, exhibiting constant $T_A = T_0$ (red dashed curve) as shown in Fig. 2.

The expression $T_A(T_0, P)$ means active area average temperature reached at ambient temperature T_0 and quasi-static power dissipation P. The intersection (cyan cross) in Figs. 1 and 2 points on active area average temperature $T_A(T_{00}, P) = T_0$ reached by quasi-static device self-heating by P at ambient temperature T_{00}.

The proposed method is based on the quasi-static V_{DS} voltage application (blue solid curve) in Figs. 1 and 2 to find V_{PO} and corresponding $P_{PO} = V_{PO}I_{DS}$ and $T_A(T_0, P_{PO})$. Subsequently, the V_{DS} application at T_0 as short-pulsed and biased by V_{PO}, corrected by trapped charge contribution, results in isothermal I_{DS} versus V_{DS} and T_A versus P and dependencies (blue dashed curve) shown in Figs. 1 and 2, respectively, of constant $T_A(T_0, P_{PO})$ for $V_{DS} > V_{PO}$. The intersection (blue cross) of V_{PO}-biased isothermal (blue dashed) and quasi-static (green solid curve) dependencies measured at T_0 and T_{00}, respectively, corresponds to $T_A(T_0, P_{PO}) = T_A(T_{00}, P + P_{PO})$.

For T_A determination purposes, available methods [10], [11], [12] are based on the concept of infinite thermal conductance and the same temperature along the device's active area. Therefore, power density distribution along the active area plays no role. In this case, a quasi-static thermal model [13] was employed utilizing active area thermal resistance $R_{TH}(T_A) = dT_A/dP$ dependent on T_A, but independent on P and T_0, resulting in $T_0 = T_A(T_0, P = 0\ \text{W}) = T_A(T_{00}, P)$ and $T_A(T_0, P_{PO}) = T_A(T_{00}, P + P_{PO})$ as depicted in Fig. 2.

The determined intersection (blue cross) in Fig. 1 gives the opportunity to calculate $P + P_{PO} = V_{DS}I_{DS}$ in this operating point, but the value $T_A(T_{00}, P + P_{PO})$ and corresponding intersection (blue cross) in Fig. 2 are unknown. However, the point $(P + P_{PO}, T_0)$ (blue dot) can be determined as shown in Fig. 2, this point shifted by P_{PO} (red arrow) brings the point (P, T_0) (cyan cross). Plotting multiple points (P, T_0) gives the opportunity to obtain T_A versus P dependence at T_{00}. The explicit $T_A(T_0, P_{PO})$ acquisition at $V_{DS} = V_{PO}$ is not required.

The minor variation of pinch-off area length and negligible trapped charge contribution result in constant isothermal output I–V characteristics for $V_{DS} > V_{PO}$. Widely utilized methods [10], [11] are coming out from this assumption.

III. Experimental

A. Structure Design and Experimental Setup

The investigated $Al_{0.25}Ga_{0.75}N$/GaN HEMT structure, including 14 nm $Al_{0.25}Ga_{0.75}N$/1.5 nm AlN/1700 nm GaN/75 nm thermal boundary resistance layer (TBR) heterostructure was grown by MOVPE on a 70 μm thick 4H-SiC substrate, containing the backside Au contact, which was soldered to 1 mm thick CuMo leadframe using a 60 μm thick AuSn solder. The top ohmic drain–source and gate contacts were created via standard Au-based metallization. A gated transmission line model (GTLM) HEMT of the width $w \approx 100\ \mu$m, the gate length $d_G \approx 0.15\ \mu$m, the source-to-gate gap length $d_{GS} \approx 0.75\ \mu$m, and the drain-to-gate gap length $d_{GS} \approx 1.5\ \mu$m was investigated [14]. The device was placed in an open package located on the Al thermal chuck and maintained at a constant temperature.

A semiconductor parameter analyzer Agilent 4155C and controlled thermal chuck were utilized to acquire the pulsed output I–V characteristics of short-pulselength $t_P \approx 100$ ns at zero V_{GS} and V_{DS} biased by $V_{PO} \approx 5.5$ V superimposed by short-pulsed voltage varied from 0 up to 22 V. The chuck temperature was set in the range 25 °C $< T_0 <$ 185 °C. The quasi-static output I–V characteristic utilizing 0 V $< V_{DS} <$ 27.5 V for gate–source voltage $V_{GS} = 0$ V at ambient temperature $T_{00} = 25$ °C was acquired followed by the device trapping level reset via white LED illumination for one minute after the measurements.

The 3-D model incorporating device geometry, layout, and thicknesses of individual layers was created using the 3-D thermal FEM simulations performed by Synopsys TCAD Sentaurus [15]. The material thermal conductivity and capacity values were obtained and calibrated from the previous work [16], [17]. The constant ambient temperature boundary condition was set to the structure backside, assuming an ideal heat transfer between the leadframe and heatsink. The self-heating is simulated by three thermal contacts placed along 2DEG, between the drain and source, representing heat contribution

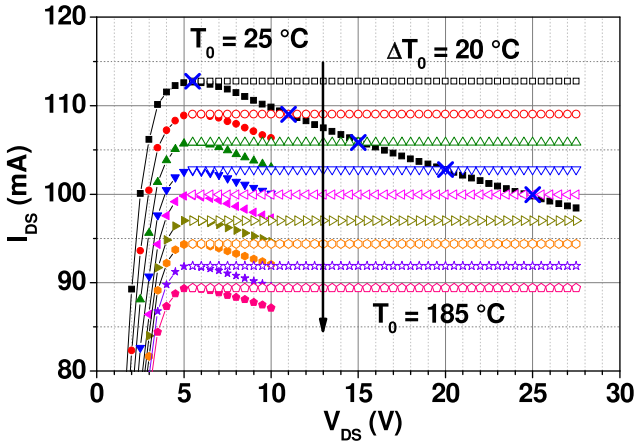

Fig. 3. Measured quasi-static output I–V characteristics (solid dots) and isothermal constant I_{DS} (blank dots) acquired by step 1) resulting in intersections (blue cross) utilized to plot T_0 versus $P + P_{PO}$ dependence.

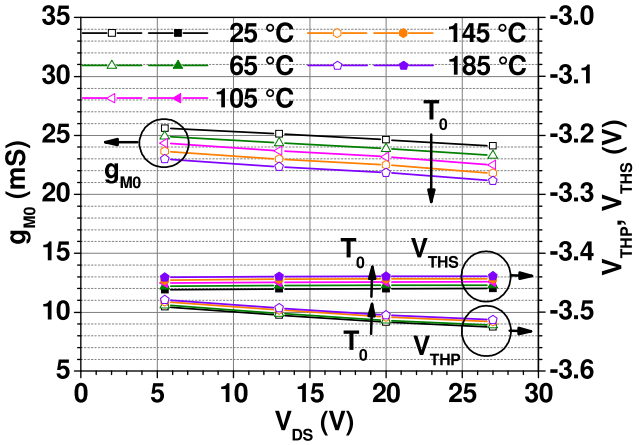

Fig. 4. Transconductance g_{MO} at $V_{GS} = 0$ V acquired in step 3a) and threshold voltage V_{THP} and V_{THS} acquired in the step 3b) at various V_{DS} and T_0.

from the drain to the source access region, under the gate electrode, and the pinch-off region located at the drain side gate edge [16].

B. Isothermal Drain-to-Source Current Acquisition

The isothermal output I–V characteristics for $V_{DS} > V_{PO}$ were acquired with the step sequence explained as follows for ambient temperature set at 25 °C $< T_0 <$ 185 °C with step $\Delta T_0 \approx 20$ °C:

1) Quasi-static output I–V characteristics for 0 V $< V_{DS} <$ 10 V and $V_{GS} = 0$ V were obtained to determine $V_{PO} \approx 5.5$ V of the minor temperature variation. The experimental procedure is completed, no pulse measurements are required if the pinch-off area length variation and the trapping centers alteration for $V_{DS} > V_{PO}$ play a minor role. In this case, the constant isothermal I–V characteristics assumption (blank dots) as depicted in Fig. 3 is employed and isothermal I_{DS} is V_{DS}-independent for $V_{DS} > V_{PO}$.
2) For inaccurate results brought by isothermal I_{DS} expectations for $V_{DS} > V_{PO}$, pulsed output I–V characteristics, $V_{PO} \approx 5.5$ V biased and superimposed by short-pulsed V_{DS} part in the range 0–22 V, at $V_{GS} = 0$ V in the T_0 range were measured. In this case, isothermal I_{DS} values are V_{DS}-dependent. The experimental procedure is terminated here for negligible additional charge trapping caused by $V_{DS} > V_{PO}$.
3) Temperature-dependent charge trapping is already included in steps 1) and 2) thanks to quasi-static V_{PO} biasing. Despite advanced GaN-based material growth technologies, V_{DS}-dependent charge trapping occurs. The proposed method allows incorporating these phenomena as the approximation by FET transconductance multiplied by threshold voltage shift. The sequence of how to obtain isothermal current contribution caused by trapped charge ΔI_{TE} is shown as follows:
   a) Pulsed output I–V characteristics at various T_0 biased by $V_{PO} \approx 5.5$ V superimposed by short-pulsed V_{DS} part in the range 0–22 V with synchronously pulsed V_{GS} at ~0 and ~0.5 V were acquired to obtain HEMT transconductance g_{M0} at $V_{GS} = 0$ and 5.5 V $< V_{DS} <$ 27.5 V at $T_A(T_0, P_{PO})$ as shown in Fig. 4.
   b) Zero V_{DS} and V_{GS} biased pulsed transfer I–V characteristics and quasi-static transfer I–V characteristics, all measured at -4 V $< V_{GS} < -2$ V and 5.5 V $< V_{DS} <$ 27.5 V at various T_0, result in threshold voltage V_{THP} and V_{THS} corresponding to pulsed and quasi-static operation, respectively, as shown in Fig. 4.
   c) The isothermal current contribution $\Delta I_{TE} = -g_{M0}\Delta V_{TH}(V_{DS})$ at V_{DS} proportional to $\Delta V_{TH}(V_{DS}) = V_{THS}(V_{DS}) - V_{THP}(V_{DS})$ is caused by a trapped charge [12]. Whereas V_{PO} biasing causes charge trapping related to $\Delta V_{TH}(V_{PO}) = V_{THS}(V_{PO}) - V_{THP}(V_{PO})$, the approximation of trapped charge contribution to I_{DS} acquired from V_{PO}-biased pulsed output I–V characteristics is $\Delta I_{TE}(V_{DS}) \approx g_{M0}(V_{PO})\Delta V_{TH}(V_{PO}) - g_{M0}(V_{DS})\Delta V_{TH}(V_{DS})$.

The isothermal output I–V characteristics (blank dots) and V_{PO}-biased and including $\Delta I_{TE}(V_{DS})$, are depicted in Fig. 5.

C. Average Channel Temperature Determination

As described in the theoretical section, the intersections of V_{PO}-biased isothermal and quasi-static output I–V characteristics correspond to active area average temperature $T_A(T_{00}, P + P_{PO}) = T_A(T_0, P_{PO})$. In the equation, $T_A(T_{00}, P + P_{PO})$ means T_A reached quasi-static power dissipation $P + P_{PO}$ at ambient temperature $T_{00} = 25$ °C, whereas $T_A(T_0, P)$ is defined as T_A reached for quasi-static power dissipation P_{PO} applied at ambient temperature 25 °C $< T_0 <$ 185 °C.

The intersections (blue cross) in Fig. 3 obtained by sequence 1) correspond to $T_A(T_{00}, P + P_{PO})$ and $T_A(T_0, P)$ making available to plot the points $(P + P_{PO}, T_0)$ (blue blank dots) shown in Fig. 6. The T_A versus P dependence (blue solid dots) at T_{00} as depicted in Fig. 6 is obtained by the P_{PO} shift

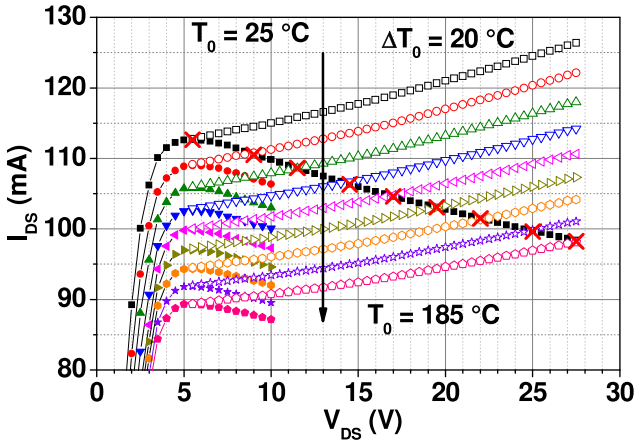

Fig. 5. Measured quasi-static output I–V characteristics (solid dots) and isothermal varying I_{DS} (blank dots) acquired by steps 1)–3) resulting in intersections (red cross) utilized to plot T_0 versus $P + P_{PO}$ dependence.

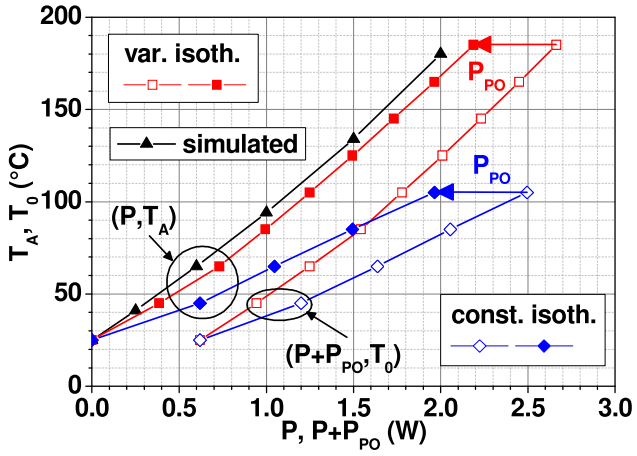

Fig. 6. Average temperature T_A versus dissipated power P dependence obtained by thermal FEM simulation (black solid dots) and acquired by comparison of V_{PO}-biased isothermal and quasi-static output I–V characteristics utilizing isothermal constant I_{DS} (blue solid dots) and isothermal varying I_{DS} (red solid dots). The T_0 versus $P + P_{PO}$ dependencies (blue and red blank dots) are utilized to plot T_A versus P dependencies (blue and red solid dots).

(blue arrow) at T_0. Despite widely utilized methods counting on constant isothermal current for $V_{DS} > V_{PO}$ especially for long channel HEMTs [10], [11], the investigated device exhibits a notable isothermal current increase, therefore, the constant I_{DS} assumption in Fig. 3 utilized to plot T_A versus P dependence (blue solid dots) in Fig. 6 is shown for illustration purposes only.

The intersections (red cross) in Fig. 5 acquired by sequences 1)–3) taking an isothermal current increase into account correspond to $T_A(T_{00}, P + P_{PO})$ and $T_A(T_0, P)$ giving the opportunity to plot the points $(P+P_{PO}, T_0)$ (red blank dots) shown in Fig. 6. The T_A versus P dependence (red solid dots) at T_{00} as depicted in Fig. 6 is obtained by the P_{PO} shift (red arrow) at T_0 exhibiting a good correspondence with simulated T_A versus P dependence (black solid dots).

IV. Conclusion

Quasi-static thermal model and pinch-off voltage biasing were utilized for the first time to refine the average channel temperature determination applied to the $Al_{0.25}Ga_{0.75}N$/GaN HEMT. Pulsed I–V characteristics and threshold voltage variation above pinch-off voltage were employed to correct the isothermal pinch-off drain-to-source current. The pinch-off voltage biasing gives a possibility to eliminate significant drain-to-source pulsed current increase under pinch-off voltage and to avoid the device electrical parameters acquisition. Therefore, the active area average temperature is possible to be in situ determined.

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