β-Ga_2O_3 Pseudo-CMOS Monolithic Inverters

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***Abstract*— In this article, we report on the fabrication of β-Ga_2O_3 pseudo-CMOS inverters using enhancement-mode (E-mode) β-Ga_2O_3 single-finger (S_F) and multifinger (M_F) thin-film transistors (TFTs). Initially, single-stage monolithic inverter ICs were fabricated using TFTs having threshold voltages $V_{th}^{SF} = 0.6$ V and $V_{th}^{MF} = 0.1$ V. However, the single-stage inverter yielded poorer gain (4.50 at V_{DD}, supply voltage = 3 V). Alternatively, a pseudo-CMOS (double-stage) inverter was designed and fabricated, yielding a maximum gain of 6.45 but with a poor noise margin (NM). To improve the NM, the pseudo-CMOS circuit was tested using TFTs having higher threshold voltages ($V_{th}^{SF} = 1.85$ V and $V_{th}^{MF} = 1.75$ V). Notably, the optimized pseudo-CMOS circuit exhibited the least peak power consumption (0.2 nW) and the maximum gain of 8 at $V_{DD} = 3$ V. The monolithically integrated devices' performance and IC highlight this technology's remarkable potential for application in the emerging sector of power electronics and extreme-environment electronics.**

***Index Terms*— β-Ga_2O_3 heteroepitaxy, β-Ga_2O_3 thin-film transistors (TFTs), inverter logic circuits, pseudo-CMOS.**

I. Introduction

β-Ga_2O_3, an emerging ultrawide-bandgap (UWBG) material with a bandgap of 4.8 eV and a large breakdown field of 8 MV/cm, is a promising candidate for high-power electronics [1]. Furthermore, the availability of high-quality β-Ga_2O_3 substrates promoted the entry of β-Ga_2O_3 electronics into the market [2]. In addition to power electronics, UWBG CMOS circuits are highly desirable for extreme-environment applications [3]. Integrating a high-power β-Ga_2O_3 module and an efficient β-Ga_2O_3 logic circuit is desirable for the miniaturization of power electronics modules. So far, high-power MOSFETs have been extensively researched [4], [5]. β-Ga_2O_3 metal–semiconductor field-effect transistors [6] and vertical and lateral MOSFETs have also been reported [7], [8].

It is possible to obtain n-type β-Ga_2O_3 by doping Si and Sn impurities; however, producing p-type β-Ga_2O_3 is difficult due to the large activation energy (>1 eV) of p-dopants, such as Mg and Fe in β-Ga_2O_3 [9]. First-principles calculations show that the activation energy of p-dopants can be reduced via codoping; however, efficient p-type β-Ga_2O_3 has not yet been demonstrated experimentally [10]. Thus, the unavailability of efficient p-type doping in β-Ga_2O_3 hampers the development of β-Ga_2O_3 CMOS circuits. Nevertheless, it is possible to design logic circuits, e.g., an inverter with a unipolar n-MOS circuit. Various topologies are available for building unipolar inverters, and each design has certain advantages and limitations. The commonly used unipolar inverters include the diode-load type implementing two enhancement-mode (E-mode) thin-film transistors (TFTs) [11]. The other design includes the enhancement–depletion mode TFTs, which have higher gain and better power dissipation than the E-mode TFTs but increases the fabrication cost and complexity as both E-mode and D-mode TFTs are needed [11], [12]. Furthermore, pseudo-CMOS was first introduced by Huang et al. [13] demonstrating pseudo-CMOS inverters having comparable performances with CMOS counterparts. In addition, compared to conventional n-MOS logic, pseudo-CMOS gives better noise immunity, and its circuit could be implemented using either just E-mode or only D-mode TFTs [14], [15].

Demonstration of a β-Ga_2O_3 inverter circuit using a combination of D-mode and E-mode β-Ga_2O_3 transistors is previously reported [16], [17]. Furthermore, based on first-principles analysis, Ma et al. [18] reported that a monolayer Ga_2O_3 MOSFET exhibited superior characteristics compared with most other reported 2-D materials. However, we would like to emphasize that many challenges remain with respect to the development, integration, and device application of β-Ga_2O_3 logic circuits. Furthermore, notably, research on β-Ga_2O_3 logic/driver circuits is limited. Hence, this study focuses on the fabrication and characterization of β-Ga_2O_3 pseudo-CMOS inverters. Different topologies of single- and dual-stage inverters are fabricated, utilizing

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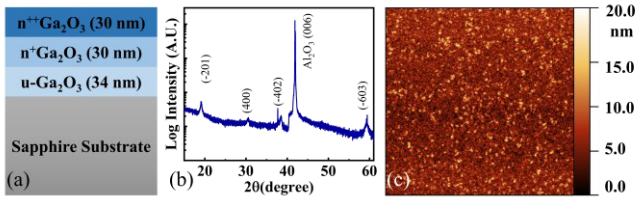

Fig. 1. β-Ga_2O_3 layers grown on a sapphire substrate via PLD. (a) Schematic, (b) X-ray diffraction spectrum, and (c) atomic force microscopy image (5 × 5 μm) of the as-grown β-Ga_2O_3.

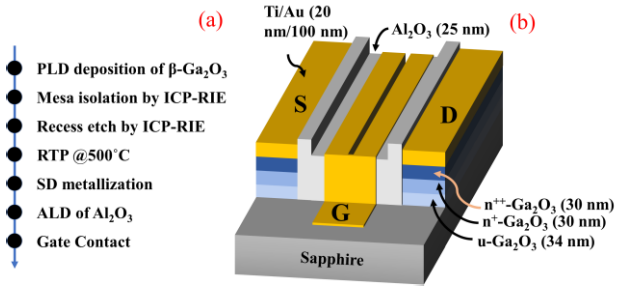

Fig. 2. (a) Process flow and (b) schematic of the standard S_F device.

β-Ga_2O_3 TFTs with different threshold voltages. The performance parameters, including gain, voltage transfer characteristics (VTCs), noise margin (NM), and power consumption, are thoroughly examined.

II. Material Growth and Device Fabrication

A. Material Growth and Characterizations

β-Ga_2O_3 thin films were grown on a single-side polished, c-plane sapphire substrate using the pulsed laser deposition (PLD) technique. Before PLD, the sapphire substrate was diced into 1 × 1 cm and cleaned in an ultrasonication bath of acetone followed by immersion in isopropyl alcohol for 5 min; the squares were rinsed with deionized (DI) water and dried with N_2 gun and finally loaded into the PLD chamber. Three PLD targets were used: target 1 was undoped Ga_2O_3, target 2 was Si-doped (SiO_2 0.1 wt%) Ga_2O_3, and target 3 was Si-doped (SiO_2 0.001 wt%) Ga_2O_3. Each target was irradiated using a KrF excimer laser ($\lambda = 248$ nm) at 100 mJ (on the target) for 1000 pulses at a frequency of 5 Hz and O_2 pressure of 4 mTorr at different temperatures of 600 °C for unintentionally doped, u-Ga_2O_3 and 700 °C for n-Ga_2O_3. Through this process, ∼34-nm u-Ga_2O_3 and two types of ∼30-nm Si-doped Ga_2O_3 with carrier concentrations of 4×10^{18} and 6×10^{19}/cm^3, respectively, were obtained as a stack of films [Fig. 1(a)]. The thickness of the film was determined by filmetrics. The X-ray diffraction spectrum depicted in Fig. 1(b) shows a low-intensity (400) peak of β-Ga_2O_3 along with a prominent (−201) peak. The atomic force microscopy surface morphology shows a root-mean-squared roughness value of 2.36 nm, as shown in Fig. 1(c).

B. Device Fabrication

Fig. 2(a) and (b) shows the fabrication flow of the device and the 3-D view of the single-finger TFT device (device S_F). For the purpose of device isolation, the sample was patterned using a photoresist and mesa etched via inductively coupled plasma reactive ion etching (ICP-RIE); this process was performed using BCl_3 and Ar plasmas. After isolation, using ICP-RIE for the gate recess depth of 30 nm was etched to engineer the threshold voltage (V_{th}) of the TFT close to zero. ICP-RIE is known to damage the surface of the target [19]. Hence, the sample was annealed in a N_2 environment at 500 °C for 5 min to heal the damage caused by the plasma [20].

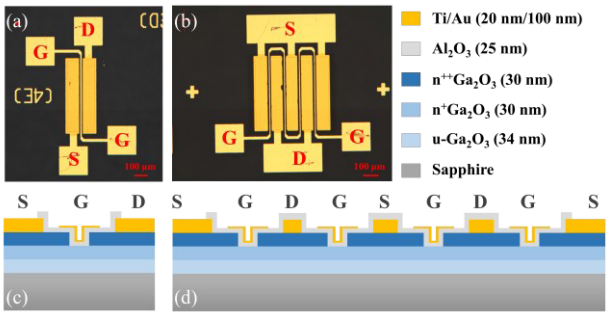

Fig. 3. Microscopy images of (a) S_F device and (b) M_F device. Schematics of the cross sections of (c) device S_F and (d) device M_F.

Ti/Au (20/100 nm) was deposited as the source–drain (SD) ohmic contact via dc magnetron sputtering. Furthermore, a 25-nm-thick Al_2O_3 layer was grown via atomic layer deposition (ALD) at 300 °C using $(CH_3)_3Al$ and O_2 plasmas as the Al and O precursors, respectively; this layer functioned as a gate dielectric. After ALD, Al_2O_3 was patterned and etched via ICP-RIE. Finally, Ti/Au (20/100 nm) layer was deposited via dc magnetron sputtering as a gate electrode. In addition to the standard design (device S_F) shown in Fig. 3(a), we also fabricated a multifinger (M_F) device [Fig. 3(b)]. Both devices have an identical source-to-drain distance (L_{sd}) of 25 μm and a gate length (L_g) of 7 μm. Along with the recess depths of 30 nm and Al_2O_3 gate dielectric thickness of 25 nm. The S_F and M_F devices only differed in their channel widths: the channel width W_S (device S_F) and W_M (device M_F) were 400 and 1600 μm (i.e., $W_M = 4 \times W_S$), respectively. The cross-sectional schematic of device S_F and M_F is given in Fig. 3(c) and (d), respectively.

III. Results and Discussion

In this section, the characteristics of transistors and the performances of the single- and dual-stage logic inverters are discussed. The devices were characterized for dc performance using a Keithley 4200 SCS parameter analyzer.

A. Transistor Characteristics

The top-gate β-Ga_2O_3 shows the typical transistor characteristics (Fig. 4). The transfer characteristics of S_F and M_F devices are shown in Fig. 4(a) and (b) respectively. The ON-current of M_F devices is higher than that of the S_F device because the M_F devices have a larger channel width-to-length ratio (W/L) and the drain current is directly proportional to the gate width ($I_D \propto W$). The V_{th} values for S_F and M_F devices are 0.6 and 0.1 V, respectively. The I_{on} and I_{off} ratios for S_F and M_F devices are 7.1×10^3 and 1.5×10^4, respectively. Furthermore, the S_F device has a higher subthreshold slope (SS) of 586 mV/dec compared with that of the M_F device (400 mV/dec), which is ∼32% less than the former.

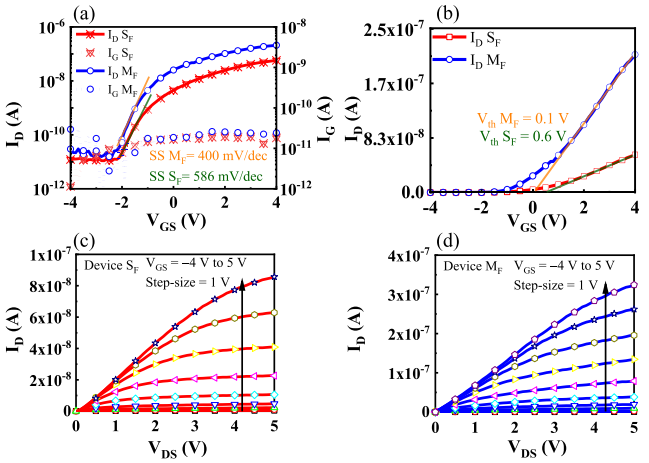

Fig. 4. Transfer characteristics of the S_F and M_F devices at drain voltage = 3 V in (a) log scale and (b) linear scale. Output characteristics of (c) S_F device and (d) M_F device.

The higher SS in the fabricated devices may result from the potential degradation of the channel–gate dielectric interface. Despite annealing to recover from plasma damage during recess formation, the gate interface quality might remain poor, contributing to the higher SS. The SS is given as follows [21]:

$$\mathrm{SS} = \ln(10)\left(\frac{kT}{q}\right)\left(1 + \frac{C_\mathrm{d} + q\,D_\mathrm{it}}{C_\mathrm{ox}}\right) \tag{1}$$

where C_d, D_it, and C_ox are the depletion capacitance, interface trap density, and oxide capacitance, respectively. In the M_F device, SS decreases due to decreased C_d as a result of charge sharing. Similar SS improvements are observed in nano transistors with an M_F structure [21]. Plasma-free wet chemical etching, such as metal-assisted chemical etching (MacEtch), could further enhance SS [22].

Fig. 4(c) and (d) shows the output characteristics of S_F and M_F devices, respectively. The drain current of the M_F device is approximately four times that of the S_F device as the channel width of the former is four times that of the latter. The ON-resistance (R_on) is very large for both devices: 43.3 MΩ·m for the S_F device and 14 MΩ·m for the M_F device. The effective mobility is calculated using the following equation [23]:

$$\mu_\mathrm{eff} = \frac{L_\mathrm{ch}}{W.C_\mathrm{ox}.(V_\mathrm{GS} - V_\mathrm{th})}\frac{d\left(I_\mathrm{D,lin}\right)}{d(V_\mathrm{DS})} \tag{2}$$

where L_ch denotes the channel length (source-to-drain distance), W denotes the channel width, and V_GS denotes the gate-to-source voltage. C_ox is the oxide capacitance per unit area, given by the following equation:

$$C_\mathrm{ox} = \frac{\varepsilon_0\varepsilon_\mathrm{r}}{t_\mathrm{ox}} \tag{3}$$

where ε_0 and ε_r denote the absolute permittivity of air and relative permittivity of the gate dielectric (Al_2O_3), respectively, and t_ox denotes the dielectric thickness. The effective mobilities of the S_F and M_F devices were calculated to be 1.02×10^{-3} and 7.35×10^{-3} cm^2/Vs, respectively, which are considerably lower than the values reported in [5] and [24]. The low mobility is mainly caused by the relatively poor film quality of heteroepitaxially grown β-Ga_2O_3 on the sapphire substrate because of the lattice mismatch between the sapphire substrate and the β-Ga_2O_3 thin film [25].

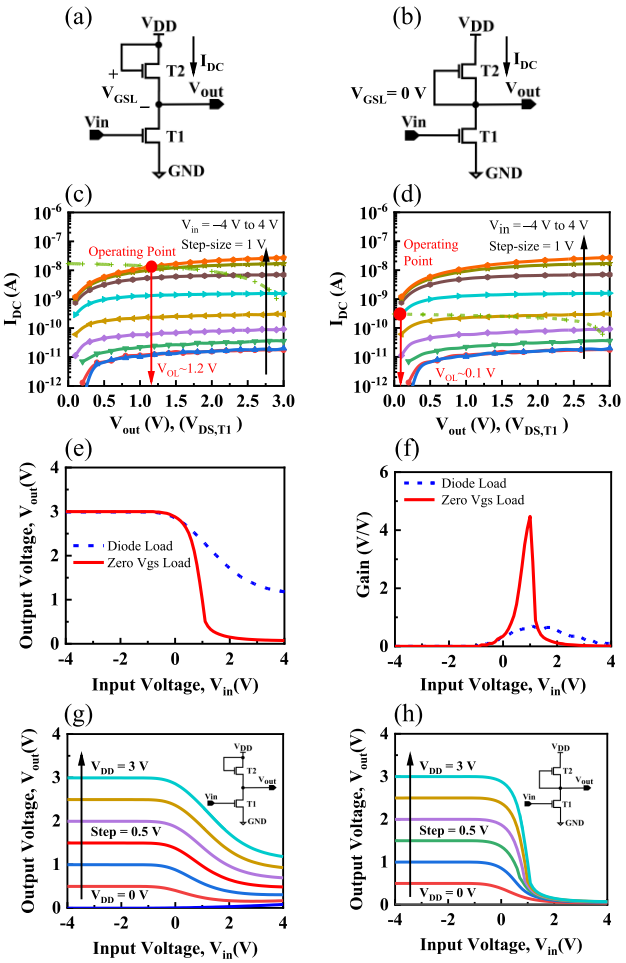

Fig. 5. Schematic of single-stage inverters (using S_F load and driver TFT). (a) Diode-load inverter. (b) Zero-V_GS load inverter. Output characteristics of driver TFT (T1) with load curves (dotted line) imposed by load TFT (T2) for (c) diode-load inverter and (d) zero-V_GS load inverter. (e) VTC and (f) gain versus input voltage of diode-load and zero-V_GS load inverters at V_DD = 3 V. VTC of (g) diode-load inverter and (h) zero-V_GS load inverter at different V_DD's.

B. Single-Stage Inverter Characteristics

The schematic of the diode-load inverter and zero-V_GS load [13] inverter is shown in Fig. 5(a) and (b). Fig. 5(c) shows the output characteristics of the driver TFT (T1) of the diode-load inverter with load curve imposed by the load TFT (T2) to show the operating point and achieved output voltage low (V_OL) of ~1.2 V. Similarly, Fig. 5(d) shows the output characteristics of the driver TFT (T1) of zero-V_GS load inverter with load curve imposed by load TFT (T2) to show the operating point, which shows that it can achieve the V_OL of ~0.1 V. Fig. 5(e) and (f) shows VTCs and gains curves of the diode-load inverter and zero-V_GS load inverter.

The K ratio (KR) [26], estimated using (4), determines the transfer characteristics of the inverter. The inverter gain improves with increasing KR, but it also contributes to increase the power consumption as a higher KR implies a larger driver transistor, which in turn indicates a higher ON-current of the

device

$$\mathrm{KR} = \frac{\mu_{n\,\mathrm{driver\,TFT}} \times C_{\mathrm{ox}} \left(\frac{W}{L}\right)_{\mathrm{driver}}}{\mu_{n\,\mathrm{load\,TFT}} \times C_{\mathrm{ox}} \left(\frac{W}{L}\right)_{\mathrm{load}}}. \tag{4}$$

The gain of the inverter module can be approximated by the product of the transconductance (g_{m}) of the driver transistor and a parallel combination of the driver transistor resistance (R_{D}) and load resistance (R_{L}), as shown in (5). From this expression, we can infer that for the inverter to have a higher gain, g_{m} of the driver TFT should be high. In addition, the resistance offered by the driver and load TFT should be high

$$\mathrm{gain} = g_{\mathrm{m}} \times \left(\frac{R_{\mathrm{D}} R_{\mathrm{L}}}{R_{\mathrm{D}} + R_{\mathrm{L}}}\right). \tag{5}$$

In the subthreshold region, the transconductance is given as [27]

$$g_{\mathrm{m}} = \frac{\ln 10}{\mathrm{SS}} I_{\mathrm{DS}} \tag{6}$$

where I_{DS} is the subthreshold drain-to-source current. From (6), we can infer that the lower the SS, the higher are g_{m} and gain; however, a lower SS indicates sensitivity to bias variation [27]. Both $\mathrm{S_F}$ and $\mathrm{M_F}$ TFTs have high SS (an SS of 586 mV/dec for $\mathrm{S_F}$ and 400 mV/dec for $\mathrm{M_F}$). As pointed out by (6), higher SS decreases g_{m} but as discussed in [27], the high SS gives stability over the bias variation. This stability for bias variation for diode-load inverter and zero-V_{GS} load inverter is evident by the VTC curves shown in Fig. 5(g) and (h), respectively.

The gain of the zero-V_{GS} load inverter is 4.5, which is four times that of the diode-load inverter, as shown in Fig. 5(f). The reason for the higher gain can be understood from the load line plot shown in Fig. 5(c) and (d). For the diode-load inverter load curve, we observe that the load TFT and driver TFT are not saturated at the same instant of time. To realize the maximum inverter gain, the load and driver TFTs should provide the maximum small-signal resistance, which is possible when the current is saturated. In other words, because the gain depends on the parallel resistance offered by the driver and load TFTs, if either the driver TFT or load TFT has low resistance, the effective resistance is close to the lower resistance (i.e., a parallel combination). This results in a decrease in the gain of the diode-load inverter.

Furthermore, Fig. 5(d) shows that although the load and driver TFTs [refer to Fig. 5(b)] operate in the subthreshold region, the current passing through devices in the zero-V_{GS} load inverter saturates when V_{DS} across driver TFT (T1) approaches 1 V and load TFT (T2) is close to 2 V (V_{DD}–V_{out}). This implies that both load and driver TFTs offer a huge resistance; hence, the gain is greater than that of the diode-load inverter.

The power consumption (P_{DC}) in this study is calculated as the product of the total current (I_{DC}) drawn by the inverter module from the supply rail and the supply voltage (V_{DD}) (i.e., $P_{\mathrm{DC}} = I_{\mathrm{DC}} \times V_{\mathrm{DD}}$). The maximum power consumption of the zero-V_{GS} load inverter was 7.5 nW (at $V_{\mathrm{DD}} = 3$ V), which is 9.5 times less than that of the diode-load inverter as the zero-V_{GS} inverter's load transistor operates in a subthreshold region where the current flowing through the circuit is in the order of nanoamperes. Such low power consumption is the major advantage of using a subthreshold-load TFT (zero-V_{GS} TFT). Ideally, the static power consumption must be zero, but a small current is present in the subthreshold region of the Ga_2O_3 TFT used in the circuit as the channel is not fully depleted at 0 V. In addition, as the threshold is close to zero, the subthreshold current is of the order of a few nanoamperes. Thus, power dissipation occurs when the driver TFT operates above the threshold voltage.

The transfer characteristics curve shows that the output voltage high (V_{OH}) values of both inverters are equal to V_{DD}, but V_{OL} of the diode-load inverter is 1.2 V and that of the zero-V_{GS} inverter is 0.3 V. This is because the load curve intersects the output characteristics of the driver at a higher voltage for the diode-load inverter than that for the zero-V_{GS} load inverter, as shown in Fig. 5(c) and (d). The transfer characteristics and gain were further improved by developing a pseudo-CMOS inverter as described in Section III-C.

C. Dual-Stage Inverter Characteristics

The performance of the CMOS inverter is well reported [14], and ideally, this type of inverter does not dissipate any static power [13]. The single-stage inverters in Section III-B lack full CMOS-like behavior due to incomplete turn-off of the load TFT when the driver TFT is on. Hence, to ensure proper turn-off of the load TFT during pull-down and the driver TFT during pull-up, pseudo-CMOS topologies were fabricated using n-type Ga_2O_3 TFT. The most common inverter topologies are pseudo-R (resistor-load inverter first stage), pseudo-E (diode-load inverter first stage) [13], [15], and pseudo-D (zero-V_{GS} load inverter first stage) inverters [13], as shown in Fig. 6(a)–(c), respectively. The load resistance in the first stage of pseudo-R circuit was realized monolithically using n-type β-Ga_2O_3 itself giving a resistance of about 666 MΩ. The optical images of all the fabricated inverters, namely, pseudo-R, pseudo-D, and pseudo-E with KR = 1, are shown in Fig. 6(d)–(f), respectively. Furthermore, Fig. 6(g)–(i) shows the optical images of inverters with KR = 28.8.

The VTC, dc power consumption, and gain are shown in Fig. 7(a)–(c), respectively. With an increase in KR, the gain increases and the transfer characteristics improve. However, power consumption also increases as the size of the driver transistor increases. This can be clearly observed in Fig. 7(b). The power consumption of pseudo-R and pseudo-E inverters increases by 3 and 1.5 times, respectively, with a fourfold increase in the drive transistor channel width. However, there is almost no significant increase in the power consumption (∼16 nW) of the pseudo-D inverter [Fig. 7(d)] because all the transistors work in the subthreshold region.

In integrated logic circuits, the inverters should be cascaded and should be able to drive consecutive stages. Therefore, each inverter should have a gain higher than unity. Thus, logic inverters with high gain are desirable. The zero-V_{GS} load inverter and pseudo-D inverter with KR = 28.8 have high gains of 5.5 and 6.5 compared with other inverter topologies,

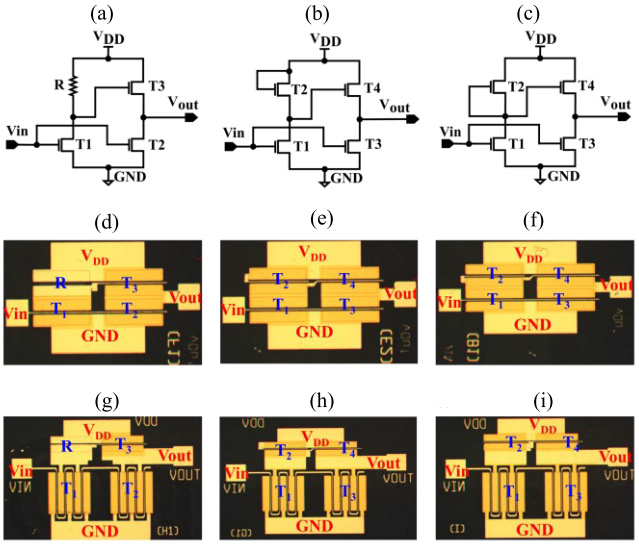

Fig. 6. Dual-stage inverter circuits and fabricated devices. (a) Pseudo-R, (b) pseudo-E, and (c) pseudo-D schematics. Fabricated devices with KR = 1. (d) Pseudo-R. (e) Pseudo-E. (f) Pseudo-D. Fabricated devices with KR = 28.8. (g) Pseudo-R. (h) Pseudo-E. (i) Pseudo-D.

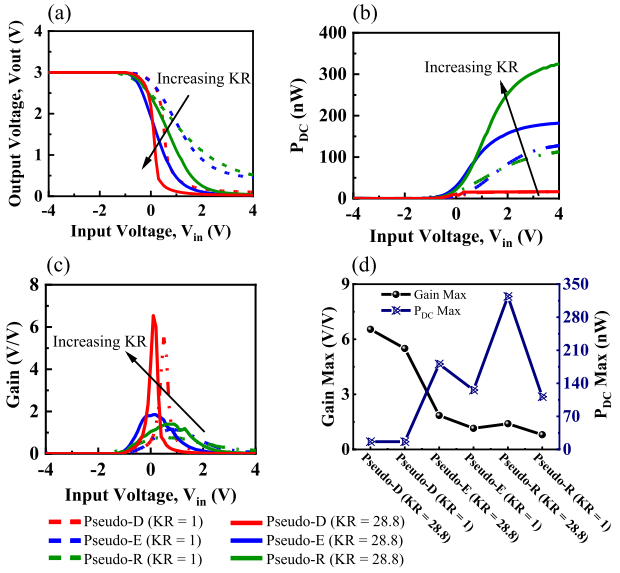

Fig. 7. Comparison of the dual-stage inverters with KR = 1 and 28.8. (a) VTC. (b) Power consumption. (c) Gain. (d) Gain and peak power consumption. Note that legends are common for (a)–(c).

respectively. This occurs because the threshold voltage of the transistor used in the zero-V_{GS} load inverter and the first stage of pseudo-D inverter is close to 0 V (0.1 V for S_F and 0.6 V for M_F), which will ensure that the load TFT is in the saturation region offering the highest load impedance resulting in an increase in the gain.

Although zero-V_{GS} and pseudo-D inverters have considerable gain, the NM offered by these topologies near zero V_{th} is poor. In the pseudo-R and pseudo-E configurations as shown in Fig. 6(a) and (b), respectively, the output of the first stage connects to the gate of the pull-up TFT in the second stage. Considering the higher V_{OL} exhibited by resistive and diode-load topologies, careful consideration of V_{th} is crucial. Choosing a very large V_{th} (much greater than the output high of the first stage) will result in the pull-up

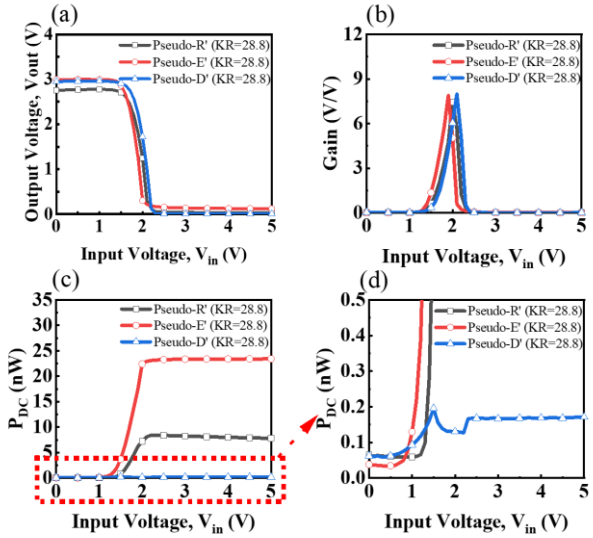

Fig. 8. For topologies pseudo-R', pseudo-E', and pseudo-D'. (a) VTC, (b) gain, (c) dc power consumption, and (d) scaled version of (c) to illustrate the dc power consumption of the pseudo-D' inverter.

TABLE I
COMPARISON OF FABRICATED PSEUDO-CMOS INVERTERS WITH THE REPORTED LOGIC INVERTER

Logic Inverters	Material	V_{DD} (V)	NMH (V)/NML (V)	Gain Max (V/V)	P_{DC} Max (nW)
Pseudo-D [14]	ZnO	5	3.57/1.37	230	~ 25
E-D [28]	IGZO	3	-	40	-
E-D [16]	Ga_2O_3	1.4	-	2.6	-
E-D [17]	Ga_2O_3	3.0	-	< 0.5	-
***Pseudo-D'**	Ga_2O_3	3.0	0.66/1.63	8.0	0.19
***Pseudo-E'**	Ga_2O_3	3.0	0.91/1.32	7.9	23.10
***Pseudo-R'**	Ga_2O_3	3.0	0.55/1.53	7.5	8.38

E-D= Enhancement-Depletion n-MOS inverter, *This work, V_{DD} = Supply Voltage, NMH/NML = Noise Margin High/Noise Margin Low, Gain Max = Maximum Gain, P_{DC} Max = dc peak power consumption.

TFT being OFF. Similarly, in the pseudo-D circuit, increasing V_{th} shifts the load TFT (T2) toward the deep subthreshold region, eventually turning it OFF. Hence, the driver and load TFTs with optimal V_{th} (S_F ~1.85 V and M_F ~1.75 V) were fabricated to improve the inverter's NM. The threshold voltage was increased by deepening the recess etch to ~35 nm. The pseudo-topologies with increased V_{th} are referred to as pseudo-R', pseudo-E', and pseudo-D', which are implemented with KR = 28.8. Fig. 8 shows their VTC, gain, and dc power consumptions.

Moreover, because the gate voltage of the load TFT in the second stage is derived from the output of the first stage, the source terminal of the second-stage load switches like V_{out} of the first stage. Hence, V_{GS} of the load TFT in the second stage is less than its V_{th} in all three pseudo-topologies. Consequently, the load TFT is in a subthreshold region, and it limits the current through it. Thus, the second stage of pseudo-topologies is in the subthreshold region. Hence, the gain of all pseudo-topologies improved and is almost equal, as shown in Fig. 8(b). Alternatively, the power consumption is <0.2 nW

for the pseudo-D' design, as shown in Fig. 8(c) and (d), because of the subthreshold region of operation in both stages.

Table I lists V_{DD}, NM high (NMH), NM low (NML), gain, and dc peak power consumption of the reported ZnO, IGZO, and Ga_2O_3 inverters along with our reported Ga_2O_3 pseudo inverters for comparison. The fabricated topologies can be considered robust with NMH of >0.5 V and NML of ∼1.5 V. The slight variations in the NM values among the pseudo-CMOS topologies originate from the small variations in V_{OH} and V_{OL} among the inverters, as seen from the VTCs in Fig. 8(a). To the best of our knowledge, this is the first pseudo inverter with a unipolar Ga_2O_3 TFT on a sapphire substrate with substantially low power consumption resulting from operation in the subthreshold region.

IV. Conclusion

In this study, we demonstrated a single-stage inverter and dual-stage pseudo-CMOS inverters using heteroepitaxial grown β-Ga_2O_3 TFTs. Various β-Ga_2O_3 logic inverters topologies were demonstrated, and their performance, including gain, VTCs, NM, and power consumption, was examined to highlight their merits and demerits. All the TFTs in the inverters were monolithically integrated on the same wafer. The threshold voltage of the TFT was tuned by tuning the recess depths of the gate during fabrication. TFTs of different sizes should be used to improve the gain; this can be achieved by using an M_F design. An ultralow power consumption inverter was realized by operating the TFTs in the subthreshold regions. Power consumption as low as 0.2 nW was achieved in the case of the pseudo-D' inverter. A gain of ∼8 V/V for V_{DD} of 3 V was achieved in the case of the pseudo-D' inverter. The NML and NMH values for all pseudo-CMOS inverters at higher threshold voltages were ∼1.5 and ∼ 0.5 V, respectively, demonstrating their robust design.

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