Role of the GaN-on-Si Epi-Stack on ΔR_{ON} Caused by Back-Gating Stress

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***Abstract*—This article reports an in-depth analysis of the ON-resistance drift (ΔR_{ON}) induced by storage/release mechanisms occurring in the buffer of GaN-on-Si power devices. The role of both stress condition (bias, temperature, and stress time) and buffer's epi-stack composition on ΔR_{ON} has been analyzed by means of back-gating current deep-level transient spectroscopy (I-DLTS). The results reveal two competing mechanisms: 1) a faster one related to acceptor defects and sensitive to the thickness of the carbon-doped GaN back-barrier (C:GaN) and superlattice (SL) layers and 2) a slower one ascribed to hole accumulation at the C:GaN/SL interface, independent of the thickness of the epi-stack. The temperature, stress bias, and stress time dependence of such mechanisms, often overlapping, have been investigated by adopting a genetic algorithm.**

***Index Terms*—AlGaN/GaN HEMT, back-gating current deep-level transient spectroscopy (I-DLTS), buffer trapping, R_{ON} drift, stretched exponential.**

I. INTRODUCTION

IT IS well-known that the deposition of GaN and its compounds (AlGaN, AlN, etc.) on a foreign substrate (e.g., silicon) implies the presence of defects/dislocations along the entire buffer up to the device surface [1]. Even though, process engineering is at an advanced stage, and GaN-on-Si devices demonstrate a good capability of withstanding relatively high drain biases [2], [3], [4], [5], charge storage and release from buffer traps or in the overall stack is still one of the dominant mechanisms causing static and/or dynamic ΔR_{ON} [6], [7], [8], [9], [10], [11], [12], [13]. Therefore, more effort is required to understand the origin of such mechanisms and how to optimize the buffer stack to minimize their effects.

In most cases, the C:GaN layer plays a key role in ΔR_{ON} since it can lead to charge storage and release during high-voltage OFF-state operation. According to the "leaky dielectric" model [6], when the buffer stack is exposed to a vertical electric field, two mechanisms show up: 1) the ionization of carbon-related acceptor traps (C_N), promoting the storage of negative charge in the C:GaN layer, inducing R_{ON} increase and 2) electron band-to-band tunneling from C:GaN valence band (VB) to two-dimensional electron gas (2DEG) through defects and dislocations, inducing hole accumulation at the C:GaN/superlattice (SL) interface, increasing the 2DEG density (R_{ON} decrease). In [13], it is shown that charge propagation through the C:GaN and the unintentional doped (uid)-GaN are assisted by 1-D and 3-D variable range hopping, respectively.

Many experimental techniques have been developed to investigate charging and discharging processes in the AlGaN/GaN buffers of power devices [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. Among them, one of the most adopted is the back-gating current deep-level transient spectroscopy (I-DLTS) [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], which consists in monitoring the recovery of R_{ON} after a negative substrate voltage stress. The latter induces different charge storage mechanisms which may compete with each other making it difficult to distinguish and quantify their effect separately [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27]. In fact, the choice of the test conditions and the transient analysis technique can strongly impact the extracted parameters (e.g., activation energy) that characterize the kind of traps or the involved physical mechanisms [12]. The most accurate method consists in fitting the ΔR_{ON} as a sum of stretched exponentials, providing useful information to understand and quantify the role of the stress conditions on the trapping and storage mechanisms and their features [24], [25], [26], [27].

In this work, we adopted the back-gating I-DLTS technique to explore how the test conditions (substrate bias, stress time, and temperature) and the thickness of the layers composing

Manuscript received 17 July 2023; accepted 7 August 2023. Date of publication 21 August 2023; date of current version 22 September 2023. This work was supported in part by Intelligent Reliability 4.0 (iRel40), iRel40 is a European co-funded innovation project that has been granted by the Electronics Components and Systems for European Leadership (ECSEL) Joint Undertaking (JU) under Grant 876659; in part by the Horizon 2020 Research Programme and participating countries; and in part by National Funding which is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, The Netherlands, Slovakia, Spain, Sweden, and Turkey. The review of this article was arranged by Editor W. Saito. *(Corresponding author: M. Millesimo.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3304272.

Digital Object Identifier 10.1109/TED.2023.3304272

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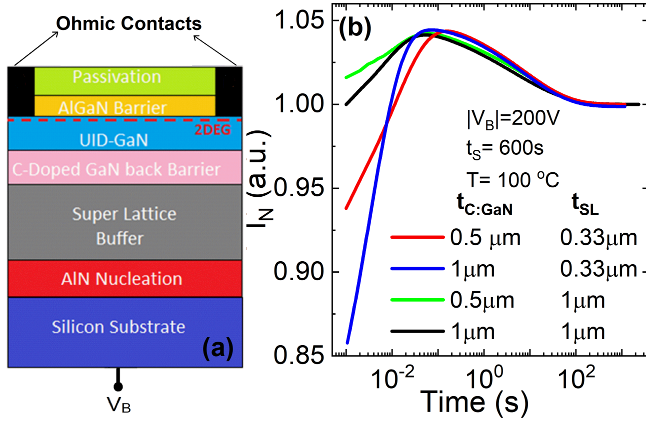

Fig. 1. Sketch (not to scale) of the device under test and the epi-structure. (a) Recovery current transient for different buffer configurations. (b) Stressing phase has been performed for 600 s with $|V_B| = 200$ V at $T = 100$ °C.

the buffer epi-stack impacts on ΔR_{ON}. The latter is fitted with a stretched exponential model by means of a mathematical approach, based on the study of the derivative, combined with a genetic algorithm to minimize the fitting error.

II. Experimental Details

A sketch of the devices under test (DUTs), fabricated by IMEC on 200-mm Si substrate for low-voltage HEMTs (<100 V), is shown in Fig. 1(a). The main difference with respect to GaN HEMT lies in the absence of the gate region. In this case, a passivation region is deposited on top of the AlGaN barrier and two ohmic contacts are created. Such a structure allows focusing the analysis directly on the buffer region, avoiding possible gate overdrive-dependent trapping mechanisms. The process splits on layers' thicknesses have been analyzed. The reference structure features an epi-stack composed of a 200-nm-thick AlN nucleation layer grown on top of Si-substrate, 330-nm-thick SL layer, 500-nm-thick C:GaN layer, 200-nm-thick uid-GaN channel layer, and 11-nm-thick $Al_{0.23}GaN_{0.77}$ barrier layer.

The back-gating I-DLTS test consists of three consecutive steps: 1) the fresh current (I_0) between the two ohmic contacts [see Fig. 1(a)] is measured with an applied voltage drop of 0.7 V and $V_B = 0$ V; 2) a negative substrate stress voltage (V_B) is applied for a fixed stress time (t_S); and 3) the current between the two ohmic contacts is monitored under the same electrical conditions reported in 1) until the recovery is completed. Finally, the current monitored during step 3) is normalized (I_N) with respect to the fresh value measured in 1). The reason why the current is monitored during the recovery rather than the stress phase is related to 2DEG depletion, which occurs for $|V_B| > 50$ V, making the current monitoring difficult and noisy. Experiments have been performed at different temperatures, stress times, and V_B.

III. Brief Physical Background

Fig. 1(b) reports I_N after a stress phase of 600 s with $|V_B| = 200$ V and $T = 100$ °C for all the process splits considered in this work. The current features two consecutive transients, i.e., I_N increase followed by a decrease toward the prestress value. For the sake of clarity, from here on, the faster (first) transient and the slower one (second) will be referred to as TR1 and TR2, respectively. In [11], the I_N increase is ascribed to electron detrapping from acceptor states in the C:GaN layer, which leads to a gradual increase of the 2DEG density (Ron decrease), whereas TR2 is associated with recombination of holes accumulated at the C:GaN/SL heterointerface, inducing an R_{ON} increase (2DEG decrease). More details on the physical mechanisms can be found in [6], [7], [8], [9], [10], and [11]. It is worth noting that this description refers to the recovery phase; exactly the opposite occurs during the stress phase, i.e., electron trapping in acceptor states and hole accumulation at the C:GaN/SL interface, leading to R_{ON} increase and decrease, respectively.

IV. Transients Analysis Methodology

The adopted methodology is based on the stretched exponential fitting law [24], by approximating I_N as follows:

$$I_{\text{fit}}(t) = 1 + \sum_{i=1}^{N} f_i(t) = 1 + \sum_{i=1}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (1)$$

$f_i(t)$ is the ith stretched exponential, N is the number of involved charge/discharge processes, A_i is the transient amplitude representing the amount of stored/released charge, τ_i is the charge emission time constant, and β_i is a stretching term representing the "slope" of the transient. The ith derivative is

$$f_i'(t) = -\frac{A_i \beta_i}{t}\left(\frac{t}{\tau_i}\right)^{\beta_i} e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}}. \quad (2)$$

To estimate τ_i and simplify the computation, we define $\psi_i(t)$ as

$$\psi_i(t) = \ln(10) t f_i'(t) = -\ln(10) A_i \beta_i \left(\frac{t}{\tau_i}\right)^{\beta_i} e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (3)$$

to verify that maxima or minima of $\psi_i(t)$is located at $t = \tau_i$. Then, the triplet (A_i, β_i, and τ_i) can be retrieved as

$$\hat{\tau}_i = \max\{\psi_i(t)\} \text{ or } \hat{\tau}_i = \min\{\psi_i(t)\} \quad (4)$$

$$\hat{A}_i = e f_i(\hat{\tau}_i) \quad (5)$$

$$\hat{\beta}_i = -\frac{e}{\ln(10)} \frac{\psi_i(\hat{\tau}_i)}{\hat{A}_i}. \quad (6)$$

The question arises whether the estimation of A_i,β_i, and τ_i parameters is correct or not by following this approach. By assuming that $\tau_1 \ll \tau_2 \ll \cdots \ll \tau_N$, the proposed method searches for the maxima and/or minima of the logarithmic derivative of $f(t)$ given by $\psi(t) = \sum_{i=1}^{N} \psi_i(t)$ obtaining preliminary estimations ($\hat{\tau}_1, \hat{\tau}_2, \ldots, \hat{\tau}_N$). Since $\tau_1 \ll \tau_2 \ll \cdots \ll \tau_N$, it is possible to approximate $I_N(\tau_i)$ as

$$I_N(\hat{\tau}_i) \approx 1 + \frac{A_i}{e} + \sum_{k=i+1}^{N} A_k \quad (7)$$

for all $i = 1, \ldots, N$. Solving the linear system described in (7), estimates of $A_1, A_2, \ldots, A_N$ can be obtained. Lastly, β coefficients can be estimated by using (6).

By observing Fig. 1(b), the number of transients is $N = 2$, and the solution is a set $p = [A_1, \tau_1, \beta_1, A_2, \tau_2, \beta_2]$ of fitting

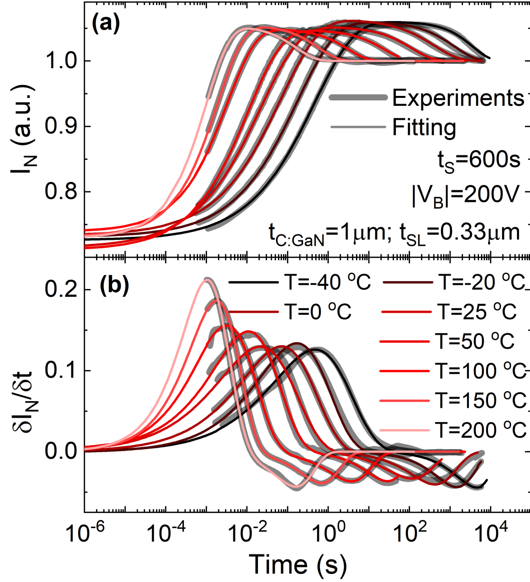

Fig. 2. (a) Recovery current transient and (b) its derivative with different temperatures ranging between −40 °C and 200 °C. The stressing phase has been performed for 600 s with $|V_B| = 200$ V.

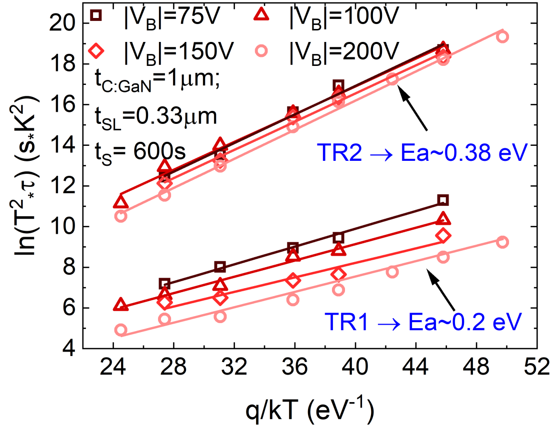

Fig. 3. Arrhenius plot in the case of stress voltage $V_B = -75$, −100, −150, and −200 V, with a stress time of 600 s.

parameters with constraints $A_1 < 0$, $A_2 > 0$, $\tau_1 < \tau_2$, and $\beta_i \in [0, 1]$.

The criticality lies in the accuracy of (7), which is ensured only if τ_1 and τ_2 are significantly different from each other. In addition, even if the current transients are nicely reproduced, $\psi_i(t)$ may not match the actual derivative. To get rid of such issues, the preliminary estimation is used as an initial solution of an optimizing algorithm, which minimizes an error function defined as the sum of the root-mean-square error (rms) of $I_N(t)$ and its logarithmic derivative [29]

$$E = \sum_{j=1}^{N_{\text{samples}}} \left| I_{N_{\text{fit}}}(t_j; \hat{P}) - I_N(t_j) \right|^2 + \left| \psi_{\text{fit}}(t_j; \hat{P}) - \psi(t_j) \right|^2. \tag{8}$$

The goal of such an algorithm is to find the optimal set of parameters p providing the best fit of the transients and their derivatives. This is possible by using a differential evolution algorithm [29], [30], i.e., a metaheuristic method that iteratively reduces E by evolving a population of approximate solutions accordingly to genetic algorithm methodology [31].

An initial population of vectors is generated by adopting the methodology described in this section. Then, a competitor (different possible solution) for each parameter vector under test is constructed by mutation and crossover over the current population. Each population element is compared with its own competitor and only one is selected (i.e., the one with the lower error), resulting in an evolved population. Finally, the mutation, crossover, and selection steps are iterated until the genetic algorithm is unable to generate a solution with a smaller error. This tool finds several applications in telecommunication systems, such as the optimization of low-density parity-check (LDPC) codes degree profile [32] and the design of coded random access protocols [33].

V. Role of the Test Conditions

A. Temperature Dependence

Fig. 2(a) and (b) shows I_N and its derivative, respectively, in the case of $|V_B| = 200$ V, stress time $t_S = 600$ s, and temperature ranging from −40 °C to 200 °C. Such t_S, widely adopted for this study, has been chosen to: 1) allow a saturation of TR2 for any V_B and 2) avoid causing permanent degradation. As observed, the methodology described in Section IV guarantees a good fitting, also in the case of high temperatures where the two transients are superimposed. Similar analyses have been performed also with different $|V_B|$, i.e., 75, 100, and 150 V. Both transients TR1 (ascending) and TR2 (descending) show a clear temperature dependence, suggesting the presence of thermally activated charging/discharging processes with an activation energy (E_A) of 0.2 and 0.38 eV, respectively (Fig. 3). Such values are similar to the ones extrapolated in [13], [19], [34], and [35] by means of back-gating measurements on AlGaN/GaN buffers.

In the case of TR1, its ascending trend may be ascribed to electron emission from acceptor traps in C:GaN layer, as reported in [6], [11], and [12]. In [36], [37], and [38], $E_A = 0.2$ eV has been ascribed to carbon atoms occupying substitutional position on nitrogen sites (C_N), leading to the creation of acceptor shallow traps with E_A between 0.08 and 0.29 eV from VB. However, more recent studies [39], [40] report that the C_N acceptors in GaN bulk are energetically located at 0.9 eV from VB. In such a case, the adoption of a relatively high carbon concentration ($\sim 10^{19}$ in this case) determines a Fermi level position slightly lower than the one of C_N, forcing the occupation of any possible preexisting acceptor states (assuming lower concentration with respect to C_N) with energy level below the Fermi one. This has been confirmed by TCAD simulation (not shown). Consequently, it is more plausible that the extrapolated $E_A = 0.2$ eV is not ascribed to the trap itself, but it represents the activation energy of trap-assisted charge transport in a defect band, probably centered at 0.9 eV from VB, i.e., carbon-related. In [13], a 3-D hopping via a defect band mechanism has been proposed. Additional discussion, supported by TCAD simulations, will follow in Section VI.

Regarding TR2, $E_A = 0.38$ eV might be associated with donor-like defects such as C_{GA} [41], oxygen [42], or silicon

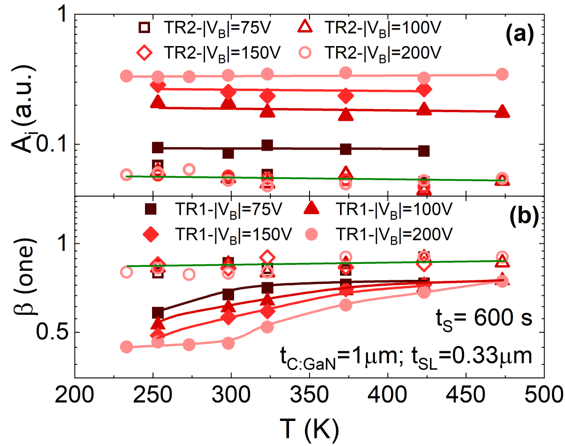

Fig. 4. Temperature dependence of the: (a) amplitude A_i and (b) stretching parameter β_i and for the two transient TR1 and TR2. Parameters have been extrapolated from measures reported in Fig. 2.

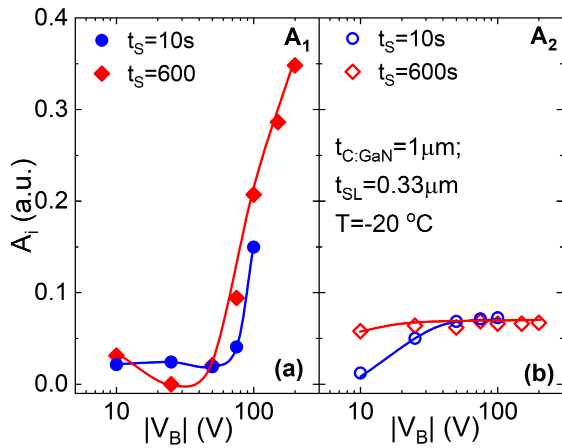

Fig. 5. Stressing voltage dependence of A_i for: (a) TR1 and (b) TR2.

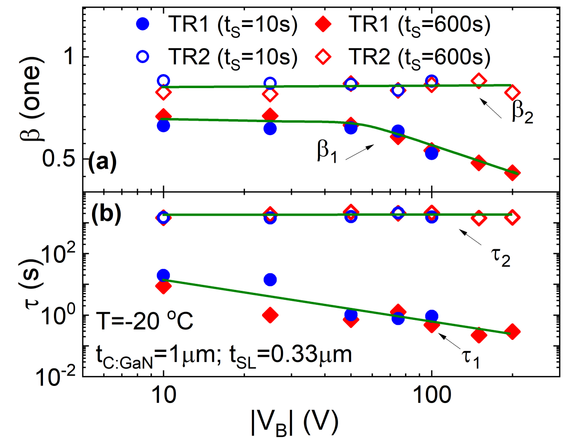

Fig. 6. Stressing voltage dependence of: (a) stretching term β and (b) trap emission time for both transients.

[19] impurities. However, most likely, such value is not related to a defect itself but it could represent the energy of a charge-transport mechanism leading to electron–hole recombination among excess 2DEG electrons and holes accumulated at the C:GaN/SL heterojunction during the stress phase [13].

Fig. 4(a) and (b) shows the temperature dependence of the stretched exponential fitting parameters A and β, respectively. A is temperature-independent in both transients TR1 and TR2 [Fig. 4(a)], suggesting that the amount of charge trapped (TR1) and accumulated (TR2) during the stress is temperature-independent; it can be faster or slower but the quantity is only bias-dependent (detailed in the next section). Regarding β, a T-dependence is shown in the case of TR1, i.e., the higher T the higher β_1, while β_2 (TR2) is almost independent, suggesting two distinct mechanisms and strengthening the theory reported in [13], i.e., electron detrapping from acceptor states (TR1) and recombination of the accumulated hole density at the C:GaN/SL interface (TR2).

B. Substrate Stress-Bias Dependence

To investigate the V_B dependence of the two transients, tests have been performed at $T = -20$ °C in order to have TR1 and TR2 quite distant from each other and to measure a bigger excursion of TR1. Fig. 5(a) shows the amplitude A_1 of TR1 as a function of $|V_B|$. Two regimes can be observed. For $|V_B| \leq 50$ V, A_1 is roughly constant and quite small, smaller than A_2 [Fig. 5(b)]. In this region, the electron trapping during the stress can be compensated and/or perturbed by the mechanism inducing hole accumulation at the C:GaN/SL interface, i.e., band-to-band electron tunneling from C:GaN VB to 2DEG. Electrons tunneling releases free holes in the VB, which can accumulate at the C:GaN/SL interface as free charge or neutralize the acceptor states [6], opposing the increase of A_1. For $|V_B| > 50$ V, A_2 saturates (also for short t_S) while A_1 increases with $|V_B|$ becoming bigger than A_2. In this regime, on the one hand, leakage can start to flow through the entire epi-stack, electrons are injected from the substrate, and hole accumulation at the C:GaN/SL interface saturates, as well as A_2. On the other hand, more electrons can be trapped in the C:GaN layer because of the higher electric field, increasing A_1. The latter mechanism is further supported by TCAD simulations reported and discussed in the next section.

Fig. 6(a) reports the V_B-dependence of β. β_1 decreases by increasing $|V_B|$, except for low $|V_B|$, whereas β_2 is bias-independent. As reported in [20], when the stretched exponential model is adopted to fit the effects of trapping/detrapping mechanisms, β can represent the energy window of the trap involved in the mechanisms. A value close to 1 implies that the trap behaves like a point defect with a discrete energy level, whereas a smaller β is associated with trapping centers forming a continuous distribution of energy levels. Based on this assumption, the smaller β_1 by increasing $|V_B|$, reported in Fig. 4, may be the result of charge trapping during the stress in a wider energy window centered at ~0.9 eV. On the contrary, the lack of V_B-dependence of β_2 further supports that TR2 is not linked to charge detrapping mechanisms but to the recombination of holes accumulated at the C:GaN/SL interface. The two mechanisms are further supported by the V_B-dependence of τ_1 and τ_2 reported in Fig. 6(b). Also in this case, τ_1 is stress bias-dependent while τ_2 is not, confirming and excluding trapping/detrapping mechanisms for TR1 and TR2, respectively.

C. Stress Time Dependence

Fig. 7 reports the stress time dependence of the A_i parameters for three different V_B. As anticipated in Section V-B, as long as A_1 is smaller than A_2 ($|V_B| < 50$ V), the trend of A_1 with both stress bias [Fig. 5(a)] and stress time [Fig. 6(a)]

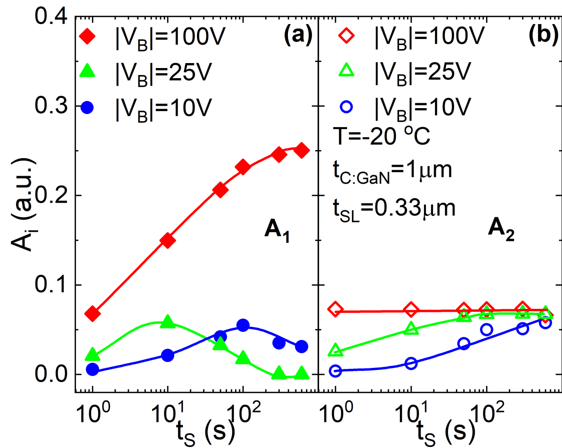

Fig. 7. Stress time dependence of Ai in the case of: (a) TR1 and (b) TR2. The temperature is −20 °C.

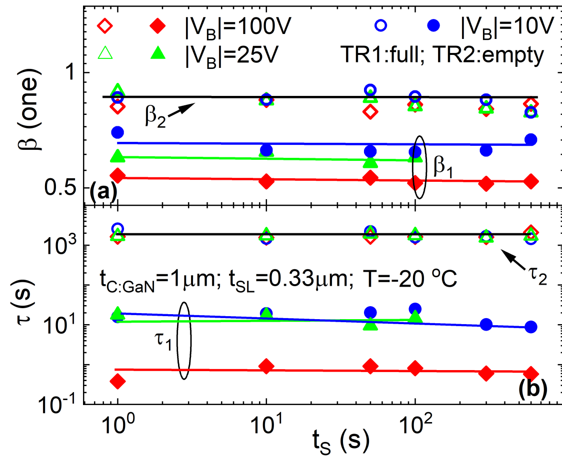

Fig. 8. Stress time dependence of: (a) stretching parameter and (b) trap emission time for both transients. The temperature is −20 °C.

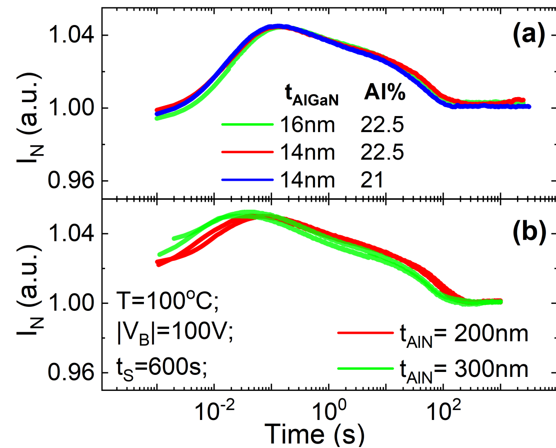

Fig. 9. Dependence of I_N in the case of: (a) different AlGaN barrier configurations and (b) AlN thicknesses. Test condition is $T = 100$ °C, $t_S = 600$ s, and $V_B = -100$ V.

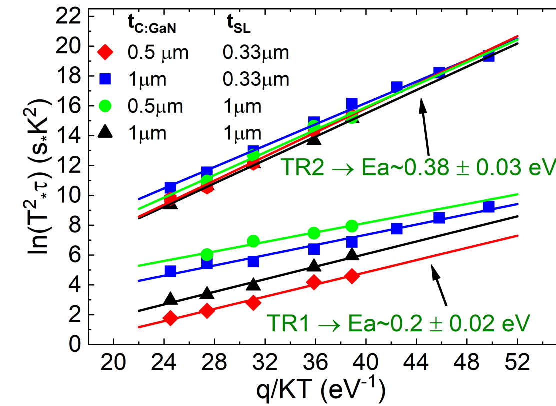

Fig. 10. Arrhenius plot in the case of stress voltage $V_B = -200$ V, with a stress time of 600 s in the case of different process splits.

is not monotonous because of the two competing mechanisms occurring during the stress phase, i.e., ionization and neutralization of acceptor states in the C:GaN layer, caused by the electric field and by free hole releasing (electron band-to-band) in the VB, respectively. Nonmonotonic R_{ON} drift has also been reported in [43].

For $|V_B| > 50$ V, A_2 is already saturated while A_1 increases hinting at a saturation for relatively long stress times (~600 s with $|V_B| = 100$ V), which is a typical behavior observed for trapping mechanisms in preexisting defects.

Finally, as expected, the stress time has no impact on β and τ, as reported in Fig. 8(a) and (b), respectively.

VI. Role of the Buffer Stack Composition

Once the role played by the stress conditions is investigated, structures featuring different epi-stacks have been analyzed and compared. Fig. 9(a) shows I_N in the case of structures featuring different AlGaN barrier configurations in terms of thickness and aluminum content (Al%). As observed, both do not significantly impact on, confirming that the underneath mechanisms do not originate from the AlGaN barrier and its interfaces. Fig. 9(b) reports the same analysis carried out on structures with different AlN nucleation layer thicknesses. A negligible impact is shown also in this case, excluding such layer as location of trapping/accumulation mechanisms.

Since the charge storage/release mechanisms are linked to the C:GaN layer, a detailed analysis has been performed by changing its thickness and the one of the SL layer.

First, a T-dependent analysis has been carried out with $|V_B| = 200$ V and $t_s = 600$ s. The Arrhenius plot in Fig. 10 shows that the activation energies of TR1 and TR2 are unimpacted neither by SL nor by C:GaN thickness, suggesting that the kind of storage/release mechanisms are always the same.

To investigate the role of the two layers on TR1 and TR2, the amplitudes A_1 and A_2 have been analyzed for each split as a function of $|V_B|$ and reported in Fig. 11(a) and (b), respectively. By focusing on TR1 [Fig. 11(a)], thus on the electron detrapping from carbon-related acceptor states in the C:GaN layer, two trends can be observed: 1) the thinner the C:GaN layer, the smaller the A_1 and 2) the thicker the SL layer, the smaller the A_1.

To better understand such experimental evidences, TCAD simulations have been performed by introducing an acceptor states concentration of $5\cdot \times 10^{18}$ cm^{-3} at 0.9 eV from the VB in the C:GaN layer, which is similar to carbon concentration. Fig. 12(a) reports the electron trapped charge (eTC) density along the C:GaN and SL layers in the case of processes featuring the same and different thicknesses for SL ($t_{SL} = 330$ nm) and C:GaN ($t_{C:GaN} = 0.5$ and 1 μm) layer,

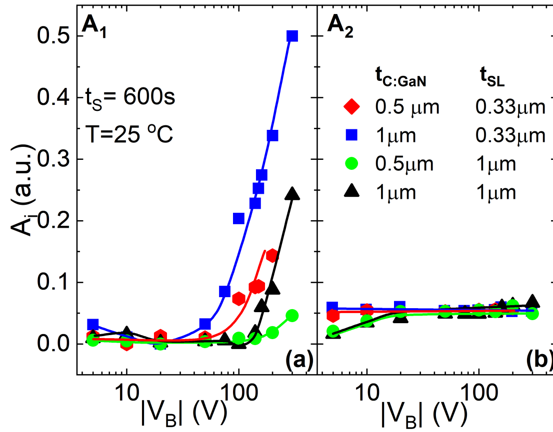

Fig. 11. Stress voltage dependence of Ai in the case of: (a) TR1 and (b) TR2 for different process splits. The test condition is $T = 25$ °C and $t_S = 600$ s.

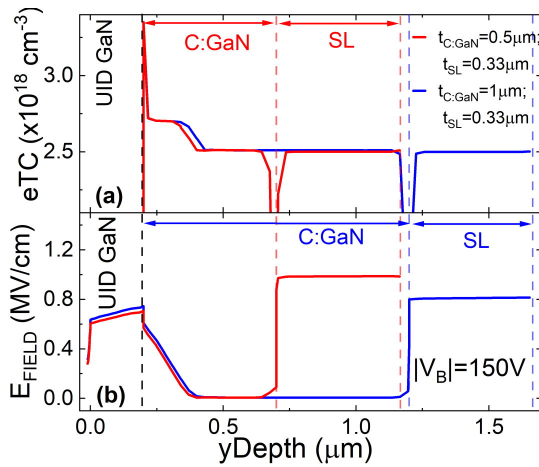

Fig. 12. (a) TCAD simulated eTC density along the vertical direction (y cutline) with $|V_B| = 150$ V for two structures featuring the same $t_{SL} = 330$ nm and a C:GaN layer thickness of 0.5 (red line) and 1 μm (blue line). (b) Corresponding simulated electric field.

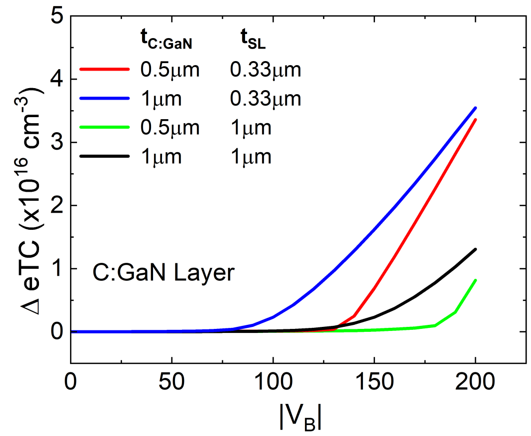

Fig. 13. Quasi-stationary simulation of the eTCs density variation (ΔeTC $=$ eTC$_{|VB|}$ $-$ eTC$_{|VB|=0V}$) as a function of $|V_B|$ for different process splits.

respectively. A thicker C:GaN layer leads to a higher electron trapping, which in turn causes a higher ΔR_{ON} (A_1). The reason can be ascribed to a different electric field distribution ruled by a capacitance voltage divider [Fig. 12(b)]. A thicker C:GaN (1 μm) gives rise to a smaller capacitance $C_{C:GaN}$, whereas the one related to the SL layer (C_{SL}) remains unchanged. The voltage drop across the C:GaN layer ($V_{C:GaN}$) is $\sim |V_B| * C_{SL}/(C_{SL} + C_{C:GaN})$, whereas the one on the SL layer (V_{SL}) is $\sim |V_B| * C_{C:GaN}/(C_{SL} + C_{C:GaN})$. As a result, the smaller the $C_{C:GaN}$ (thicker C:GaN), the higher the $V_{C:GaN}$, and the lower the V_{SL}. The result of such a divider is a higher electric field in the C:GaN layer [Fig. 12(b)], inducing a higher amount of trapped electrons (higher A_1). The opposite effect is obtained by increasing the SL layer thickness, i.e., the thicker the SL, the lower the $V_{C:GaN}$ and related electric field, the lower the eTC. Fig. 13 shows the simulated ΔeTC in the C:GaN layer, calculated with respect to $V_B = 0$ V, for all the process splits. The $|V_B|$-dependence is qualitatively in agreement with the experiments [A_1, Fig. 11(a)].

Concerning TR2, Fig. 11(b) shows an almost V_B-independent A_2, except for the low-bias regime where hole accumulation is not saturated yet (see Section V-B), even for relatively long t_S. In such a case, a thicker SL helps to significantly reduce the electric field along the uid-GaN and C:GaN layers, weakening the electron band-to-band tunneling and giving rise to a smaller A_2 [Fig. 11(b)].

VII. Conclusion

An in-depth analysis of the role of both test conditions and epi-stack buffer of GaN-on-Si devices on the mechanisms inducing ΔR_{ON} has been investigated by means of back-gating I-DLTS tests. For the first time, a genetic algorithm has been employed to accurately fit the experiments, which are often the result of two superimposed mechanisms, allowing us to investigate the temperature, stress-bias, and stress-time dependence of the representative parameters (A, β, and τ). According to the state-of-the-art, the first one is ascribed to electron trapping/detrapping in carbon-related acceptor states located in the C:GaN layer, whereas the second one can be associated with hole accumulation at the C:GaN/SL heterointerface.

A further novelty of this work relies on the study of the role of the buffer epi-stack, reporting that both mechanisms do not show dependence on the kind of adopted AlGaN barrier (neither thickness nor Al%) and on the thickness of the AlN nucleation layer. In addition, the second mechanism is almost insensitive also to C:GaN and SL thickness, except for low $|V_B|$, whereas the electron trapping in acceptor states is clearly depending on these layer thicknesses, providing useful information for the epi-stack optimization, i.e., vertical scaling down. In particular, a thinner C:GaN layer and a thicker SL layer turn out to be the best choice to attenuate the ΔR_{ON} induced by charge storage/release mechanisms, triggered by OFF-state voltage, in the buffer epi-stack.

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Open Access funding provided by 'Alma Mater Studiorum - Università di Bologna' within the CRUI CARE Agreement