Transconductance Overshoot, a New Trap-Related Effect in AlGaN/GaN HEMTs

Gao Zhan, *Member, IEEE*, Fabiana Rampazzo, Carlo De Santi, *Member, IEEE*, Mirko Fornasier, *Member, IEEE*, Gaudenzio Meneghesso, *Fellow, IEEE*, Matteo Meneghini, *Senior Member, IEEE*, Hervé Blanck, Jan Grünenpütt, Daniel Sommer, Ding Yuan Chen, Kai-Hsin Wen, Jr-Tai Chen, and Enrico Zanoni, *Life Fellow, IEEE*

***Abstract*— DC characteristics of AlGaN/GaN HEMTs with different thickness values of the undoped GaN channel layer were compared. An abnormal transconductance (g_m) overshoot accompanied by a negative threshold voltage (V_{TH}) shift was observed during I_{DS}–V_{GS} sweep in devices with thinner GaN layer. At the same time, a non-monotonic increase in gate current was observed. In OFF-state, electron trapping occurs in the undoped GaN layer or at the GaN/AlN interface, leading to a positive V_{TH} shift. When the device is turning on at a sufficiently high V_{DS}, electron de-trapping occurs due to trap impact-ionization; consequently, V_{TH} and therefore I_D suddenly recovers, leading to the g_m overshoot effect. These effects are attributed to electron trap impact-ionization and consequent modulation of the device's electric field.**

***Index Terms*— AlGaN/GaN, high electron mobility transistors (HEMTs), hot electron, impact-ionization, short channel effects, trapping.**

I. Introduction

AlGaN/GaN-BASED high electron mobility transistors (HEMTs) currently represent the best choice for high-power, high-frequency, and high-temperature applications and have found application in radar amplifiers, automotive electronics, modern telecommunication systems as 5G [1], [2], [3]. Recent requests for higher frequency operation of these devices have pushed the gate length (L_g) scaling down to a technological limit. As L_g becomes smaller and the device aspect ratio decreases, short-channel effects (SCE) may become more relevant [4], [5], [6]. Control of SCE requires scaling of vertical dimensions; reduction of substrate conductivity can be achieved by compensating the GaN buffer with Fe and/or C. However, this may give rise to parasitic effects, such as increased gate leakage current [7], [8], [9], [10], [11], decrease of electron mobility [12], trapping phenomena [13], [14], [15], and V_{TH} instability [16], [17]. An alternative way to control leakage current and SCE is to use a not-intentionally-doped GaN channel/buffer with largely reduced thickness, so that the AlN nucleation layer acts as a backbarrier.

In this work, devices under test were fabricated using undoped GaN channel layers of different thicknesses (thin, medium, and thick); interaction between hot electron effects and electron traps lead to a g_m overshoot effect which was enhanced in devices having a thin GaN channel. This transconductance overshoot, previously unexplained [18] is therefore another sign of the presence of deep levels in GaN HEMTs, as current collapse [19], [20] or kink effects [21], [22]. A physics-based explanation of this effect is proposed and discussed, which is relevant for the characterization of deep levels effects in scaled GaN HEMTs.

The device under test and experimental details are described in Section II, while results of dc electrical characterization are reported in Section III: a transconductance (g_m) overshoot was observed during transfer I_D–V_{GS} measurements at high V_{DS}. Section IV describes the results of threshold voltage (V_{TH}) transient spectroscopy. Discussion and conclusions are presented in Section V.

II. Device and Experimental Details

The RF GaN HEMT tested in this work are based on a buffer-free AlGaN/GaN on SiC epitaxy [23], [24], [25] and were processed using a production-level 0.15 μm gate length (L_g) technology. In this study, the thickness of the undoped GaN channel layer was the only variable among the samples analyzed. The samples adopted three different thickness values

Manuscript received 27 March 2023; accepted 18 April 2023. Date of publication 9 May 2023; date of current version 25 May 2023. This work was supported in part by the Italian Ministry of Research project "Empowering GaN-on-SiC and GaN-on-Si technologies for the next challenging millimeter-wave applications, 'GANAPP'; in part by the U.S. Office of Naval Research under Award N000142012177, supervisor Paul Maki; and in part by the European Commission Horizon 2020 ECSEL initiative project 5G_GaN2. The review of this article was arranged by Editor M. Hua. *(Corresponding author: Gao Zhan.)*

Gao Zhan, Fabiana Rampazzo, Carlo De Santi, Mirko Fornasier, Gaudenzio Meneghesso, and Enrico Zanoni are with the Department of Information Engineering, University of Padua, 35131 Padua, Italy (e-mail: zhan.gao@unipd.it).

Matteo Meneghini is with the Department of Information Engineering, University of Padua, 35131 Padua, Italy, and also with the Department of Information Engineering and the Department of Physics and Astronomy, University of Padua, 35131 Padua, Italy.

Hervé Blanck, Jan Grünenpütt, and Daniel Sommer are with United Monolithic Semiconductors, GmbH, 89081 Ulm, Germany.

Ding Yuan Chen, Kai-Hsin Wen, and Jr-Tai Chen are with SweGaN AB, 583 30 Linköping, Sweden.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3270134.

Digital Object Identifier 10.1109/TED.2023.3270134

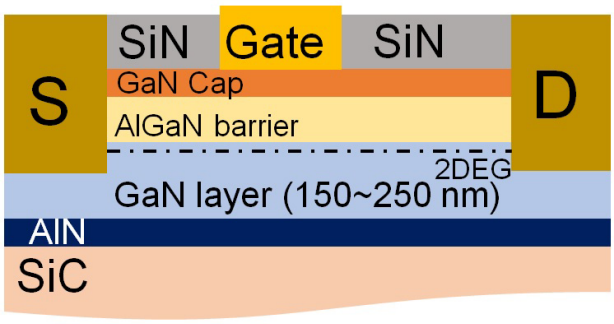

Fig. 1. Schematic cross section of the devices under test.

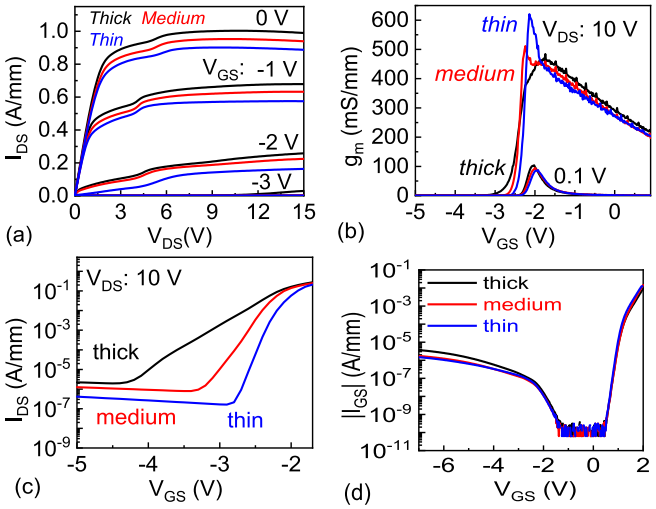

Fig. 2. (a) Output I_D–V_D characteristics at $V_{GS} = -3$ to 0 V. (b) Transfer g_m–V_{GS} characteristics at $V_{DS} = 0.1$ V and 10 V. (c) Transfer I_{DS}–V_{GS} characteristics at $V_{DS} = 10$ V. (d) I–V characteristics of the gate–source diode.

TABLE I
DC PARAMETER SUMMARY

	thin	*medium*	*thick*
I_{DSS} (A/mm)	0.90 ± 0.06	0.95 ± 0.05	0.99 ± 0.08
R_{ON} (Ω·mm)	2.2 ± 0.03	2.0 ± 0.04	1.9 ± 0.03
DIBL (mV/V)	20 ± 0.6	32 ± 1.4	83 ±3
SS (mV/dec)	109.5 ± 7.8	191 ± 29	374 ±65
$I_{DS,leak}$ (μA/mm)	4.5 ± 0.5	4.8 ± 0.9	13 ± 1.2

of the GaN layer in the range of 150–250 nm [25], [26] (Fig. 1), which are identified as *thin*, *medium*, and *thick* for ease of reference. The devices under test are two-finger devices with a width (W_G) of 2 × 40 μm.

III. DC CHARACTERIZATION

The output I_D–V_{DS}, transfer I_D–V_G, g_m–V_{GS} characteristics, and I–V curves of the gate–source diode of devices having different GaN channel thicknesses are shown in Fig. 2(a)–(d).

Results show that the *thin* devices have the best subthreshold swing (SS) and the smallest drain-induced barrier lowering (DIBL), but slightly reduced drain current (I_{DSS}).

The *thick* devices show the largest drain–source leakage current ($I_{DS,leak}$), and the highest I_{DSS}, as summarized in Table I. In the buffer-free, ultrathin GaN layer design, the AlN

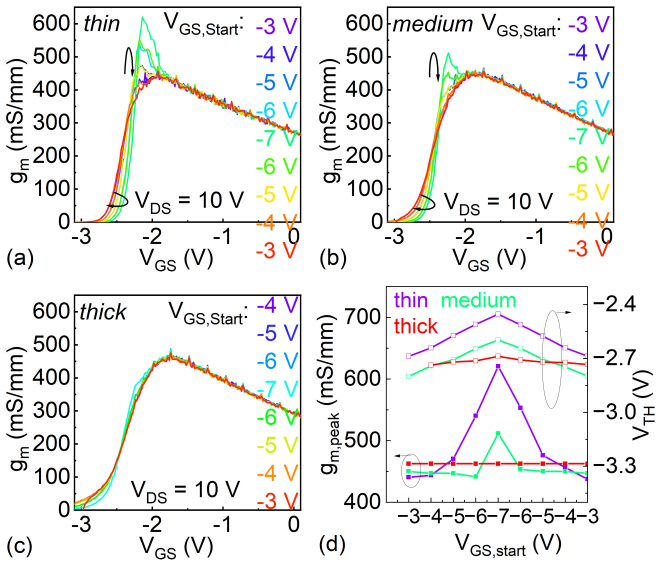

Fig. 3. (a)–(c) g_m versus V_{GS} curves of the devices at $V_{DS} = 10$ V with different V_{GS_Start}. (d) Peak g_m and V_{TH} shift as a function of $V_{GS,Start}$ in the three wafers, here V_{TH} is the gate voltage axis intercept of the linear extrapolation of the $g_m V_{GS}$ characteristics at its maximum first derivative (slope) point.

nucleation layer, with a high bandgap, acts as a backbarrier and effectively controls drain-to-source leakage, thus improving short-channel effects. Better electron confinement results in very good values of SS, DIBL, and $I_{DS,Leak}$ of the *thin* devices. However, the thinner GaN layer implies a higher vertical electric field for the same bias conditions, thus enhancing electron trapping and R_{ON} increase.

All devices are affected by a small kink effect in the output I_D–V_{DS} characteristics, Fig. 2(a). Abnormal g_m overshoot effects are observed in the *medium* and *thin* devices; the g_m overshoot amplitude is maximum in the *thin* devices [see Fig. 2(b)].

To check the influence of reverse bias in OFF-state on the overshoot, the g_m–V_{GS} characteristics were measured in the saturation region ($V_{DS} = 10$ V), increasing the absolute value of the starting gate voltage value ($V_{GS,Start}$) in pinch-off conditions, (Fig. 3). Measurements have been taken using a 20 ms integration time. When $V_{GS,Start}$ was decreased in steps from −3 to −7 V, the g_m overshoot became more and more apparent and was accompanied by a gradual positive V_{TH} shift in the *thin* and *medium* devices [see Fig. 3(a) and (b)]. These effects were recoverable when measurements were repeated by gradually increasing $V_{GS,Start}$. *Thick* devices are not affected by dynamic V_{TH} shift effects [Fig. 3(c)]. Fig. 3(d) shows the amplitude of g_m overshoot and V_{TH} values for the three types of devices, as a function of $V_{GS,Start}$.

The presence of hysteresis effects in the g_m–V_{GS} characteristics was studied by taking the measurements twice, i.e., first by increasing (V_{GS}), i.e., from −7 to 1 V ("Go" measurement) and then with decreasing V_{GS} from 1 to −7 V ("Back"), at $V_{DS} = 10$ V, as shown in Fig. 4(a) for a representative *thin* channel device; I_G–V_{GS} characteristics were simultaneously measured.

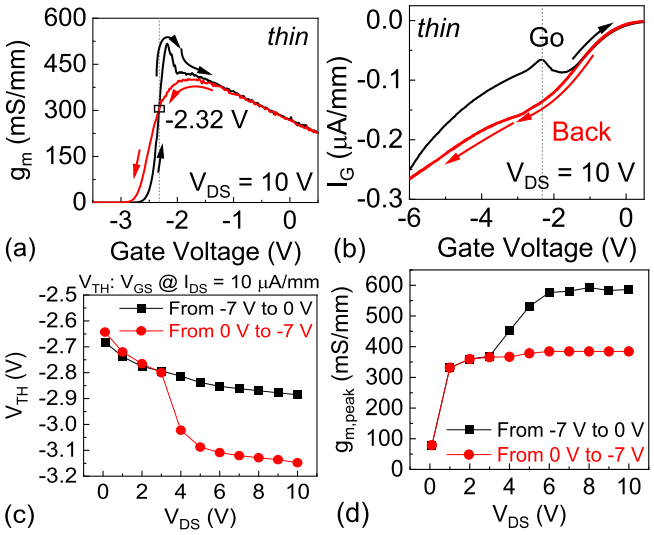

Fig. 4. (a) Transconductance characteristics and (b) gate current characteristics of a representative *thin* device, at $V_{DS} = 10$ V, (c) V_{TH}, and (d) $g_{m,peak}$ as a function of V_{DS}.

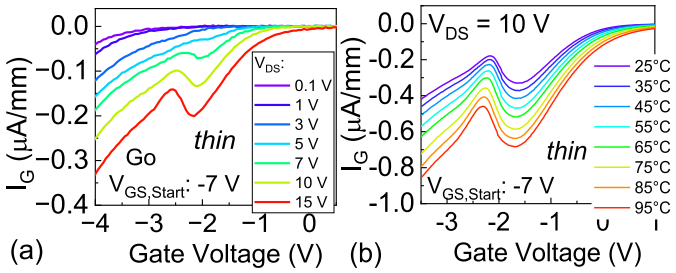

Fig. 5. I_G versus V_{GS} at $V_{DS} = 10$ V of a representative *thin* device (a) at different drain voltage at RT and (b) at various backplate temperatures.

During the "Go" measurement, once V_{GS} becomes larger than V_{TH} ($\cong -2.5$ V), electrons populate the channel, drain current starts to flow, and g_m increases steeply to the overshoot value. At the same bias conditions, a bell-shaped bump appears in the I_G–V_{GS} characteristics, corresponding to a sudden increase of gate current, Fig. 4(b).

In pinch-off conditions, a negative gate current (I_{GS}) is measured, consisting of electrons injected from the gate into the AlGaN barrier. As V_{GS} increases, $|I_G|$ becomes lower, since the reverse bias between the gate and source/drain decreases, leading to lower electric field values. However, at $V_{GS} \approx -2.32$ V, $|I_G|$ starts to increase again and creates a bell-shaped bump in the I_G–V_{GS} characteristics, which is typical of impact-ionization effects [27], [28]. Finally, around $V_{GS} = -0.5$ V, $|I_G|$ resumes the initial decreasing trend.

During the "Back" sweep, no g_m overshoot is observed, and V_{TH} recovers (i.e., it shifts toward more negative values), Fig. 4(a). In the "Back" sweep, I_G shows no bump, and its absolute value is larger than the values measured during the "Go" phase [see Fig. 4(b)], thus creating hysteresis in the I_G versus V_{GS} characteristics. These measurements were repeated for different values of V_{DS}: g_m overshoot, V_{TH} shift, and I_G bell shape occurred only for $V_{DS} \geq 4$ V [see Figs. 4(c), (d), and 5(a)].

Conventionally, the non-monotonic increase of $|I_G|$ is attributed to the hot-electrons-induced generation of holes via band-to-band impact-ionization (i.i.), and subsequent collection at the gate. As V_{GS} is increased beyond V_{TH}, 2DEG density increases, more hot electrons are generated and can impact-ionize, thus increasing $|I_G|$. For higher V_{GS} values, due to electric field decrease and enhanced phonon- and electron-electron scattering, electron energy and impact-ionization are reduced, leading to the observed non-monotonic, bell-shape behavior of $|I_G|$.

In the devices under test, however, direct band-to-band i.i. seems unlikely: 1) the bell-shaped $|I_G|$ increase is observed even at $V_{DS} = 4$ V, which is too low for band-to-band i.i. to occur in a wide bandgap material like GaN [29] and 2) I_G versus V_{GS} characteristics show hysteresis effects which suggest that traps may be involved; in fact, experimental data can be explained by trap assisted impact ionization, consisting in the detrapping of electrons due to the interaction (impact-ionization) between high energetic hot electrons and filled deep levels, without hole generation. The energy required for this process is just the difference between the conduction band edge and the deep level energy, much lower than the energy gap. As in the case of band-to-band impact-ionization, trap-related impact-ionization requires hot electrons, but it can occur at much lower values of energy (or electric field). When, at increasing V_{GS}, the channel is opened, channel hot electrons impact-ionize traps, and the negative charge stored in the access region between the gate and drain is removed, leading to a sudden increase of the electric field [29], and a consequent jump of the gate leakage current. At the same time, a negative threshold voltage shift occurs, leading to the g_m overshoot due to the corresponding sudden increase in drain current. As V_{GS} is further increased, the decrease of V_{GD} and of the electric field induces a decrease in the gate leakage current. The bell-shaped, non-monotonic behavior of I_G is therefore due to a modulation of the electric field consequent to trap impact-ionization. In its turn, the increase of the electric field induces an increase in gate leakage current. Since the latter dominates I_G its thermal coefficient is positive, Fig. 5(b), with an activation energy of around 0.87 eV. Gate current (I_G) as a function of temperature [see Fig. 5(b)] shows that the bell-shaped behavior is present at all temperatures, from 25 °C to 95 °C.

IV. Threshold Voltage Transients

V_{TH} transients were measured using a two-phase trap filling/recovery experiment. During the filling phase (duration 100 s), the device was biased in pinch-off at $V_{GS} = -6$ V, $V_{DS} = 0$ V. During the recovery phase, the device was biased either in OFF-state ($V_{GS,B} = -4$ V) or in the semi-ON state ($V_{GS,B} = -2$ V). Recovery experiments were repeated at increasing V_{DS} from 1 to 15 V, in 1 V steps. At various intervals during both phases, filling or recovery bias was turned off for 4 μs and the $I_D V_{GS}$ characteristics were measured. The "dynamic" V_{TH} value was extrapolated; its values are reported in Fig. 6 for a representative *thin* device.

During the filling stress, a positive V_{TH} shift is observed, with a logarithm dependence on the stress time. This behavior was previously detected in transistors based on silicon [30]

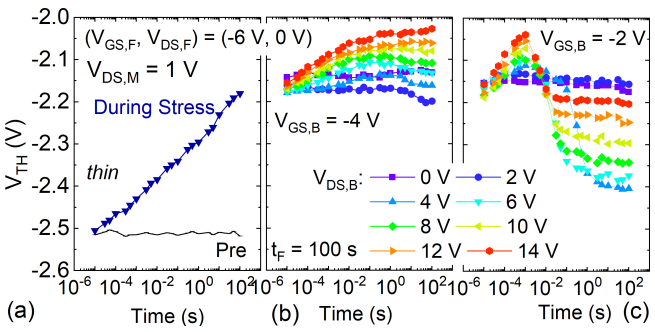

Fig. 6. (a) For reference, V_{TH} transient during a trap filling pulse at (−6 V, 0 V), V_{TH} is extracted from I_D–V_{GS} measurements at $V_{DS} = 1$ V, (b) V_{TH} recovery transient with device in OFF-state, and (c) semi-ON state.

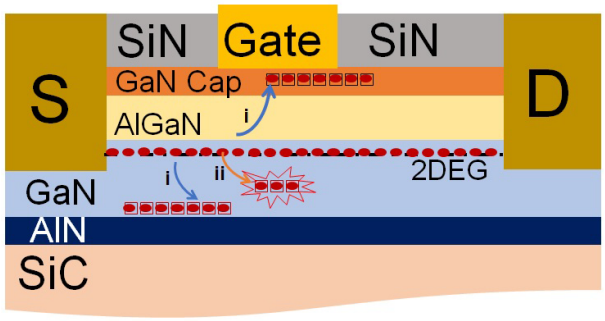

Fig. 7. Schematic representation of the trapping/detrapping process. (i) Hot electrons get trapped by surface or buffer traps and (ii) hot electrons impact ionize trapped electrons, leading to negative V_{TH} shift. (Solid circles: electrons, open squares: holes, explosion pattern: impact ionization.)

Ga_2O_3 [31], GaN [32], [33] and SiC [34], and is usually described by an "inhibition model" [30], [32] which assumes that when an electron is trapped, a Coulombic potential is generated, and this inhibits charge trapping in neighboring defects, thus decreasing the trapping rate. The long filling time explains why V_{TH} positive shift and g_m overshoot are not observed for short integration times (20 μs).

When the recovery phase is evaluated in OFF-state with V_{DS} lower than 4 V, negligible recovery of V_{TH} (<10 mV) occurs [see Fig. 6(b)]; for higher V_{DS}, further trapping occurs and an additional positive V_{TH} shift is observed [35]. On the contrary, when the device is biased in a semi-ON state ($V_{GS} = -2$ V) with $V_{DS} \geq 3$ V, significant recovery occurs, i.e., device current is required to promote detrapping. On the other hand, for $V_{DS} \geq 7$ V fast (100 μs) hot-electron trapping effects compete with de-trapping, and recovery is incomplete [see Fig. 6(c)].

The shape of the V_{TH} transients can be explained as follows: When, after an OFF-state stress phase, the device recovery is studied in the semi-ON state, hot electrons are generated, inducing two competing mechanisms: 1) hot electrons may be trapped on the device surface or in the buffer, thus inducing a positive threshold voltage shift and 2) hot electrons impact-ionize negatively charged traps, leading to negative threshold voltage shift (Fig. 7). The former mechanism is very fast (10–100 μs), the second is slower (1–10 ms), leading to a non-monotonic behavior of V_{TH} transients as a function of

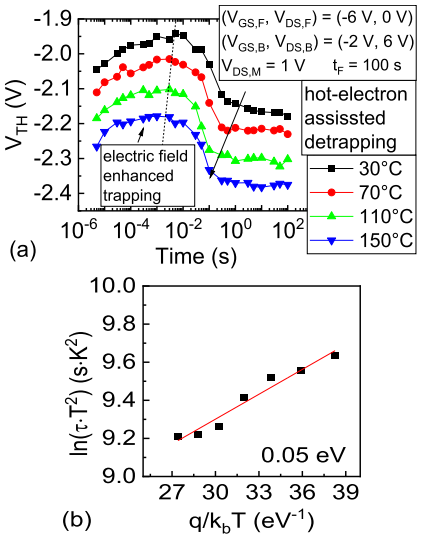

Fig. 8. (a) V_{TH} recovery transients at various temperatures, after 100 s filling at (−6 V, 0 V). During recovery, the *thin* device was biased at $V_{GS,B} = -2$ V, $V_{DS,B} = 6$ V. (b) Arrhenius plot.

time, Fig. 6(c). At V_{DS} higher than 8 V, the first mechanism prevails, and V_{TH} does not recover anymore.

Fig. 8 shows V_{TH} semi-on recovery transients as a function of temperature in a representative *thin* device, after 100 s filling at (−6 V, 0 V). During recovery, the device was biased at $V_{GS,B} = -2$ V, $V_{DS,B} = 6$ V, in semi-on. The Arrhenius plot [see Fig. 8(b)] indicates that recovery is very weakly thermally activated, with a very low activation energy of 0.05 eV, possibly resulting from trapping and detrapping mechanisms having opposite dependence on temperature. The identification of the relevant deep levels is difficult, as the detrapping mechanism is due to trap impact-ionization and not to temperature-enhanced electron release. This also contributes to making the activation energy of the recovery process extremely low.

V. Discussion and Conclusion

In this work, buffer-free AlGaN/GaN HEMTs with ultrathin GaN layers of different thicknesses were studied. It is shown that by reducing GaN layer thickness, one can effectively improve charge confinement, reducing SS and DIBL. However, trapping effects in devices having a thin GaN layer thickness led to g_m overshoot effects, and bell-shaped $|I_G|$ increase. These effects can be explained by the interaction of hot electrons, deep levels, and trapped charge.

In OFF-state, electron trapping occurs in the undoped GaN layer or at the GaN/AlN interface, leading to positive V_{TH} shift, as shown in Fig. 9. When increasing $|V_{GS}|$ in OFF-state conditions, trapping is enhanced and further V_{TH} shift occurs, Fig. 3. When the GaN channel layer is thicker, the distance between the 2DEG channel and the defective region at the GaN/AlN interface is increased [23], [29], [36], thus reducing trapping effects within the GaN layer and at its interface with AlN.

When the device is turning on at a sufficiently high V_{DS}, electron de-trapping occurs, due to the impact-ionization of filled traps by hot electrons. V_{TH} (and therefore I_D) suddenly

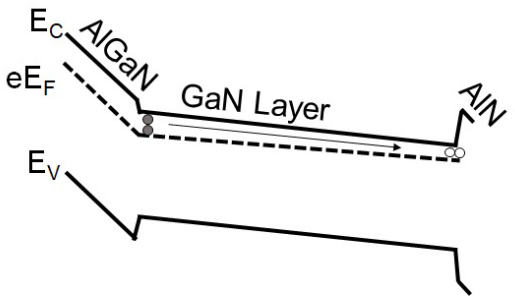

Fig. 9. Schematic energy band diagrams of the device during OFF-state stress. (Solid circles: electrons, open circles: traps.)

recovers, leading to the g_m overshoot effect during g_m–V_{GS} measurements, as shown in Fig. 3.

The de-trapping mechanism is identified by analyzing its correlation with I_G: an indirect mechanism involving the impact-ionization of traps can indeed explain all the experimental results.

In GaN HEMTs, negative trapped charge under the gate and in the gate–drain access regions controls the electric field profile. Once electrons are removed by trap i.i., the electric field increases, leading to gate leakage current increase. Trap impact-ionization follows the same non-monotonic trend of band-to-band impact ionization, causing a bell-shape in the I_G–V_{GS} curve (Fig. 5). However, once traps are depleted of electrons, they remain empty during the subsequent part of the measurement, as filling time is longer than measurement time (Fig. 6). This explains the hysteresis during "Go" and "Back" I_G–V_{GS} measurements (Fig. 3): during the "Go" measurement with V_{GS} from −7 to 0 V, the negative charge is removed as the channel is opened, through traps i.i. As a consequence, during the "Back" measurement (V_{GS} from 0 to −7 V), traps are empty, without trapped negative charge in the gate–drain region, and the electric field becomes higher, thus leading to a higher gate reverse leakage current I_G, as shown in Fig. 5.

Trap i.i. is confirmed by several experimental observations: de-trapping is not due to the electric field, as it does not take place in OFF-state, Fig. 6(b); the electron energy required to impact-ionize traps is much lower than that needed for the band-to-band generation of electron-hole pairs, so that trap i.i. and the consequent transconductance overshoot can occur at V_{DS} values as low as 4 V. Finally, semi-ON-state de-trapping is not thermally activated (Fig. 8), possibly due to the compensation of two counteracting mechanisms, i.e., the decrease of electron energy at increasing T, and thermally-activated de-trapping.

In conclusion, in buffer-free AlGaN/GaN HEMTs adopting a *thin* undoped GaN channel layer, trapping in OFF-state followed by impact-ionization of traps in semi-ON state explains the anomalous g_m overshoot, as well as the observed V_{TH} shift and the non-monotonic, bell-shaped, increase of $|I_G|$.

Devices adopting a *thick* GaN layer are free from those parasitic effects, showing that optimization of GaN thickness and epitaxial layers leads to excellent performances of these HEMTs in terms of gate length scalability and electrical reliability.

Acknowledgment

The authors are indebted to Manuel Fregolent (University of Padua), for useful discussions on the nature of deep levels. The authors would like to thank Niklas Rorsman and Mattias Thorsell (Chalmers University) for the data, samples, and useful technical discussions.

References

[1] P. M. Asbeck, N. Rostomyan, M. Özen, B. Rabet, and J. A. Jayamon, "Power amplifiers for mm-wave 5G applications: Technology comparisons and CMOS-SOI demonstration circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3099–3109, Jul. 2019, doi: 10.1109/TMTT.2019.2896047.

[2] P. Waltereit et al., "GaN HEMTs and MMICs for space applications," *Semicond. Sci. Technol.*, vol. 28, no. 7, Jul. 2013, Art. no. 074010, doi: 10.1088/0268-1242/28/7/074010.

[3] K. Yuk, G. R. Branner, and C. Cui, "Future directions for GaN in 5G and satellite communications," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2017, pp. 803–806, doi: 10.1109/MWSCAS.2017.8053045.

[4] O. Breitschädel et al., "Short-channel effects in AlGAN/GaN HEMTs," *Mater. Sci. Eng., B*, vol. 82, nos. 1–3, pp. 238–240, May 2001, doi: 10.1016/S0921-5107(00)00747-9.

[5] G. H. Jessen et al., "Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2589–2597, Oct. 2007, doi: 10.1109/TED.2007.904476.

[6] C. W. Pearce and D. S. Yaney, "Short-channel effects in MOSFET's," *IEEE Electron Device Lett.*, vol. ED-6, no. 7, pp. 326–328, Jul. 1985, doi: 10.1109/EDL.1985.26143.

[7] J. Lei et al., "Reverse-blocking normally-OFF GaN double-channel MOS-HEMT with low reverse leakage current and low ON-state resistance," *IEEE Electron Device Lett.*, vol. 39, no. 7, pp. 1003–1006, Jul. 2018, doi: 10.1109/LED.2018.2832180.

[8] L. He et al., "The influence of Al composition in AlGaN back barrier layer on leakage current and dynamic R_{ON} characteristics of AlGaN/GaN HEMTs," *Phys. Status Solidi, A*, vol. 214, no. 8, Aug. 2017, Art. no. 1600824, doi: 10.1002/pssa.201600824.

[9] Y. Shi et al., "Investigation on the device geometry-dependent reverse recovery characteristic of AlGaN/GaN lateral field-effect rectifier (L-FER)," *Superlattices Microstruct.*, vol. 120, pp. 605–610, Aug. 2018, doi: 10.1016/j.spmi.2018.06.020.

[10] M. Hua et al., "Characterization of leakage and reliability of SiN_x gate dielectric by low-pressure chemical vapor deposition for GaN-based MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3215–3222, Oct. 2015, doi: 10.1109/TED.2015.2469716.

[11] W. S. Tan, M. J. Uren, P. A. Houston, R. T. Green, R. S. Balmer, and T. Martin, "Surface leakage currents in SiN_x passivated AlGaN/GaN HFETs," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 1–3, Jan. 2006, doi: 10.1109/LED.2005.860383.

[12] A. Cappy, B. Carnez, R. Fauquembergues, G. Salmer, and E. Constant, "Comparative potential performance of Si, GaAs, GaInAs, InAs submicrometer-gate FET's," *IEEE Trans. Electron Devices*, vol. ED-27, no. 11, pp. 2158–2160, Nov. 1980, doi: 10.1109/T-ED.1980.20166.

[13] A. M. Angelotti, G. P. Gibiino, C. Florian, and A. Santarelli, "Trapping dynamics in GaN HEMTs for millimeter-wave applications: Measurement-based characterization and technology comparison," *Electronics*, vol. 10, no. 2, p. 137, Jan. 2021, doi: 10.3390/electronics10020137.

[14] Y. Shi, W. Chen, Z. Fu, S. Chen, and B. Zhang, "Influence of the acceptor-type trap on the threshold voltage of the short-channel GaN MOS-HEMT," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 606–611, 2021, doi: 10.1109/JEDS.2021.3085886.

[15] M. J. Uren et al., "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 395–398, Feb. 2006, doi: 10.1109/TED.2005.862702.

[16] F. Crupi, P. Magnone, S. Strangio, F. Iucolano, and G. Meneghesso, "Low frequency noise and gate bias instability in normally OFF AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2219–2222, May 2016, doi: 10.1109/TED.2016.2544798.

[17] K. Fu et al., "Threshold switching and memory behaviors of epitaxially regrown GaN-on-GaN vertical *p-n* diodes with high temperature stability," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 375–378, Mar. 2019, doi: 10.1109/LED.2019.2891391.

[18] F. Albany et al., "Stability of the threshold voltage in fluorine-implanted normally-off AlN/GaN HEMTs co-integrated with commercial normally-on GaN HEMT technology," *Microelectron. Rel.*, vol. 126, Nov. 2021, Art. no. 114291, doi: 10.1016/j.microrel.2021.114291.

[19] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proc. IEEE*, vol. 90, no. 6, pp. 1048–1058, Jun. 2002, doi: 10.1109/JPROC.2002.1021569.

[20] J. Joh, J. A. del Alamo, and J. Jimenez, "A simple current collapse measurement technique for GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 665–667, Jul. 2008, doi: 10.1109/LED.2008.2000919.

[21] R. Cuerdo et al., "The kink effect at cryogenic temperatures in deep submicron AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 209–212, Mar. 2009, doi: 10.1109/LED.2008.2011289.

[22] G. Meneghesso, B. Cogliati, G. Donzelli, D. Sala, and E. Zanoni, "Development of 'kink' in the output I–V characteristics of pseudomorphic HEMT's after hot-electron accelerated testing," *Microelectron. Reliab.*, vol. 37, nos. 10–11, pp. 1679–1682, Oct. 1997, doi: 10.1016/S0026-2714(97)00138-8.

[23] J.-T. Chen et al., "A GaN–SiC hybrid material for high-frequency and power electronics," *Appl. Phys. Lett.*, vol. 113, no. 4, Jul. 2018, Art. no. 041605, doi: 10.1063/1.5042049.

[24] J. Grünenpütt et al., "Evaluation of novel iron-free QuanFINE® structure by 100 nm and 150 nm AlGaN/GaN HEMT technology," in *Int. Conf. Compound Semiconductor Manuf. Technol., Dig. Papers*, 2021, pp. 149–152.

[25] D. Y. Chen and K.-H. Rorsman, "Improve 2DEG confinement in 70 nm AlGaN/GaN HEMTs by reducing the GaN channel thickness in buffer-free heterostructures," in *Proc. Int. Workshop Nitride Semiconductors*, 2022, pp. 149–151.

[26] D.-Y. Chen et al., "Microwave performance of 'buffer-free' GaN-on-SiC high electron mobility transistors," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 828–831, Jun. 2020, doi: 10.1109/LED.2020.2988074.

[27] K. Hui, C. Hu, P. George, and P. K. Ko, "Impact ionization in GaAs MESFETs," *IEEE Electron Device Lett.*, vol. 11, no. 3, pp. 113–115, Mar. 1990, doi: 10.1109/55.46951.

[28] D. Bisi et al., "Observation of ID–VD kink in N-polar GaN MIS-HEMTs at cryogenic temperatures," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 345–348, Mar. 2020, doi: 10.1109/LED.2020.2968875.

[29] A. Soni and M. Shrivastava, "Interplay of various charge sources in AlGaN/GaN epi-stack governing HEMT breakdown," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2378–2386, May 2021, doi: 10.1109/TED.2021.3068079.

[30] D. R. Wolters and J. J. van der Schoot, "Kinetics of charge trapping in dielectrics," *J. Appl. Phys.*, vol. 58, no. 2, pp. 831–837, Jul. 1985, doi: 10.1063/1.336152.

[31] M. Fregolent et al., "Logarithmic trapping and detrapping in β-Ga_2O_3 MOSFETs: Experimental analysis and modeling," *Appl. Phys. Lett.*, vol. 120, no. 16, Apr. 2022, Art. no. 163502, doi: 10.1063/5.0085068.

[32] M. Ruzzarin et al., "Highly stable threshold voltage in GaN nanowire FETs: The advantages of p-GaN channel/Al_2O_3 gate insulator," *Appl. Phys. Lett.*, vol. 117, no. 20, Nov. 2020, Art. no. 203501, doi: 10.1063/5.0027922.

[33] D. Bisi et al., "On trapping mechanisms at oxide-traps in Al_2O_3/GaN metal-oxide-semiconductor capacitors," *Appl. Phys. Lett.*, vol. 108, no. 11, Mar. 2016, Art. no. 112104, doi: 10.1063/1.4944466.

[34] F. Masin et al., "Non-monotonic threshold voltage variation in 4H-SiC metal–oxide–semiconductor field-effect transistor: Investigation and modeling," *J. Appl. Phys.*, vol. 130, no. 14, Oct. 2021, Art. no. 145702, doi: 10.1063/5.0057285.

[35] Z. Gao et al., "Degradation mechanism of 0.15 μm AlGaN/GaN HEMTs: Effects of hot electrons," *Microelectron. Rel.*, vol. 114, Nov. 2020, Art. no. 113905, doi: 10.1016/j.microrel.2020.113905.

[36] J. Lu et al., "Transmorphic epitaxial growth of AlN nucleation layers on SiC substrates for high-breakdown thin GaN transistors," *Appl. Phys. Lett.*, vol. 115, no. 22, Nov. 2019, Art. no. 221601, doi: 10.1063/1.5123374.

Open Access funding provided by 'Università degli Studi di Padova' within the CRUI CARE Agreement