Fine-Tunable Emission Pulse Generation Circuit Based on p-Type Low-Temperature Poly-Si Thin-Film Transistors for Active Matrix Organic Light-Emitting Diode Displays

Min Kyu Chang, Ji Hoon Kim, and Hyoungsik Nam, *Member, IEEE*

***Abstract*— Active matrix organic light-emitting diode (AMOLED) displays have deployed the compensation techniques to cope with the luminance non-uniformity issues caused by variations on electrical characteristics of thin-film transistors (TFTs). While some compensation circuits require control signals of longer pulse widths than a line time, the luminance control as well as the higher bit depth representation have been also accomplished by adjusting the pulse widths. A proposed EM pulse generation circuit consists of 11 p-type low-temperature poly-Si (LTPS) TFTs and a one coupling capacitor. While previous tunable circuits could address pulse widths of either even or odd multiples of a line time, the proposed circuit can generate any multiples by changing phases of additional clock signals. In particular, the internal inverter is implemented with a load connected to the output of a previous stage's inverter to reduce the power consumption over pulse widths. The coupling capacitor is also connected between two adjacent stages through one TFT, eliminating coupling noises on the output pulses. The proposed EM circuit is simulated at a line time of 3.8 μs for a 120 Hz 3840 $\times$ 2160 display. The results ensure that pulse widths from three to 2160 lines are generated successfully without coupling noises and the small variation on power consumption from 1.23 to 0.33 mW is achieved at 30 stages for the whole range of pulse widths, compared to the large range from 1.26 to 76.91 mW with the inverter of a diode-connected load.**

***Index Terms*— EM circuit, fine-tunable, low-temperature poly-Si thin-film transistor (LTPS TFT), organic light-emitting diode (OLED), tunable pulsewidth.**

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The authors are with the Department of Information Display, Kyung Hee University, Seoul 02447, South Korea (e-mail: hyoungsiknam@khu.ac.kr).

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I. Introduction

RECENTLY, active matrix organic light-emitting diode (AMOLED) displays have attracted humongous interest due to high-contrast ratio, wide-viewing angle, large-color gamut, high resolution, slim form factor, and flexible design [1], [2], [3], [4], [5], [6]. AMOLED displays have led the smartphone markets mainly and are expanding their portion even in the large size display area such as televisions [7].

Although AMOLED displays adopt a similar scanning way to active matrix liquid crystal displays (AMLCDs) by means of source and gate driver circuits, they require additional schemes to compensate for variations on thin-film transistor (TFT), supply voltage, and organic light-emitting diode (OLED) that cause observable artifacts, such as Mura, non-uniformity, and image-sticking. Consequently, many compensation techniques including current programming, voltage programming, digital programming, and external compensation are reported [8], [9], [10], [11], [12]. While voltage programming circuits are widely employed in small and medium-sized applications, the external compensation schemes are adopted in large-sized displays that suffer from supply voltage variation and need a long operational lifetime. To realize these compensation methods, additional control signals should be supported except for scanning pulses. A representative one is an emission control signal (EM) that manages the light emission time of an OLED. In general, this signal is used to block the undesired light emission during the compensation operation. Also, the EM signal can be in use to change the luminance by the pulsewidth modulation (PWM) scheme. In smartphones, the luminance needs to be adjusted according to the ambient illuminance to save the power consumption and to alleviate the image-sticking problem [13]. It has been also reported that the higher bit depth for the gray representation can be achieved by managing data voltage level as well as emission time [14], [15] and the high-moving image picture quality can be achieved by black frame insertion [16], [17]. The tunable EM circuits can support the scanning as well as the pulsewidth adjustment for a variety of applications, such as compensation,

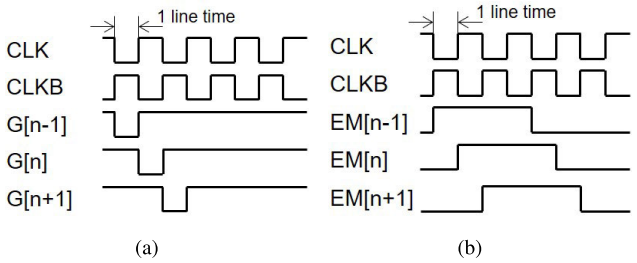


Fig. 1. Control signal pulses for AMOLED pixel circuits. (a) Gate pulses. (b) EM pulses.

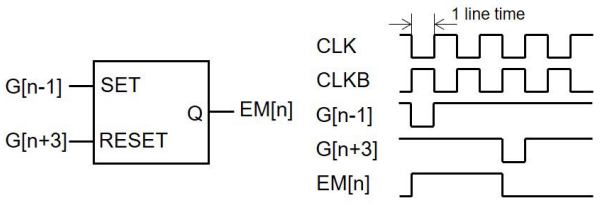


Fig. 2. EM pulse generation based on scanning pulses.

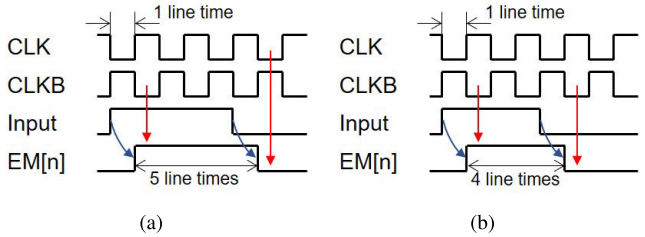


Fig. 3. Conventional tunable EM pulse generation scheme. (a) Odd multiple pulsewidth of a line time (five line times). (b) Even multiple pulsewidth of a line time (four line times).

luminance control, high-bit depth representation, and black frame insertion.

The previous EM circuits have programed the duty ratio by changing the start pulsewidth applied to the first stage and shifted the pulse in a fashion of stage-by-stage by means of the same clock signals used in scanning shift registers [13], [18], [19], [20]. However, their pulsewidth tunability is limited by odd or even number multiples of the line time. This limitation has been coped with by the low-temperature poly-Si oxide (LTPO) circuit in addition to the reduction on the power consumption [21]. Since the duty ratio is only changed by the hard-wired input signals that are the output signals from other scanning shift registers, there do not exist any ways to adjust the pulsewidth after the fabrication. The equivalent approach has been also reported to support the foveation-based driving circuit for the high-resolution head-mounted AMOLED display [22]. Another LTPO circuit has been proposed to control EM pulse widths by the number of the input pulses that have the pulsewidth of one line time [23]. However, it can also support only pulse widths of even multiples. In addition, while the pulse widths are extended, the scanning pulses should not be generated. EM circuits cannot operate independently of the pixel programming conducted by scanning pulses.

This article introduces a fine-tunable EM pulse generation circuit that controls the pulsewidth precisely by any multiples of a line time. Because its pulsewidth is programed only by the start pulse like previous approaches, the duty ratios of EM pulses are adjustable even after the fabrication.

II. Proposed EM Pulse Generation Circuit

As presented in Fig. 1, the key requirements of the EM circuit are to get longer pulses (EM[$n-1$], EM[n], EM[$n+1$]) than a line time as well as to shift them by one line time like shift registers that generate scanning gate pulses (G[$n-1$], G[n], G[$n+1$]). To support the shifting operation by a line time, the EM circuit should share clock signals (CLK, CLKB) or output pulses of scanning shift registers.

The simplest implementation of the EM circuit is to use gate pulses to specify the timing of output transitions. As shown in Fig. 2, ($n-1$)th and ($n+3$)th gate pulses (G[$n-1$], G[$n+3$]) of the low voltage level at a backplane of p-type low-temperature poly-Si (LTPS) TFTs may be used as set and reset signals of the conventional shift register circuit to trigger falling and rising transitions of the nth EM pulse (EM[n]) with the pulsewidth of four line times. However, this scheme provides only the fixed pulsewidth.

Most tunable EM circuits have maintained long pulse widths by the input signal of the target pulsewidth that is usually the EM pulse of the previous stage and shifted them by means of clock signals used in scanning shift registers. In an example of Fig. 3(a), CLKB and CLK delay rising and falling transitions of the input pulse by a line time, respectively. Because the time interval between CLK and CLKB pulses is an odd multiple of a line time, the pulsewidth of the output is restricted to an odd multiple of a line time. If one clock signal like CLKB controls both rising and falling transitions as depicted in Fig. 3(b), only the pulsewidth of an even multiple of a line time is achieved. Since the phases of CLK and CLKB are fixed for the scanning pulse generation, this implementation has a limit to supporting pulse widths of either odd or even multiples of a line time.

In this article, we employ two additional clock signals which phases are adjusted by the external clock generation circuit. Because these variable phase clock signals are used to set the rising transition of the output, the proposed EM circuit achieves the programmable pulse widths of any multiples of a line time.

The proposed EM pulse generation circuit consists of 11 p-type LTPS TFTs (P1–P11) and one capacitor ($C1$) as illustrated in Fig. 4. VGH and VGL are high and low supply voltages. CLK and CLKB are two-phase clock signals for both shift registers of scanning and EM pulses. CLKE is also one of two-phase clock signals, but is adjustable in a phase depending on whether the pulsewidth is an odd or even multiple of a line time. P1 and P2 generate A[n] pulses synchronized at CLKB only during the low level of EM[$n-1$], P3 and P4 pull Q[n] up and down, P5 and P6 pull EM[n] up and down, and P7–P10 are integrated into an inverter for the generation of QB[n] to control pull-up TFTs of P3 and P5. In particular, P11 is deployed between the current and next stages at Q[n] and EM[$n+1$] to attenuate the coupling noises from EM[$n+1$].

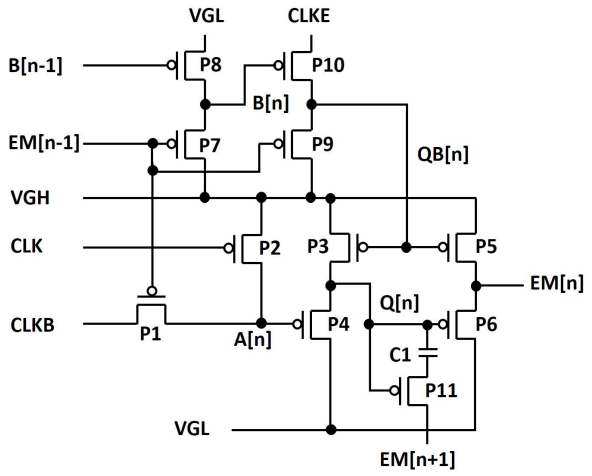


Fig. 4. Proposed EM circuit schematic.

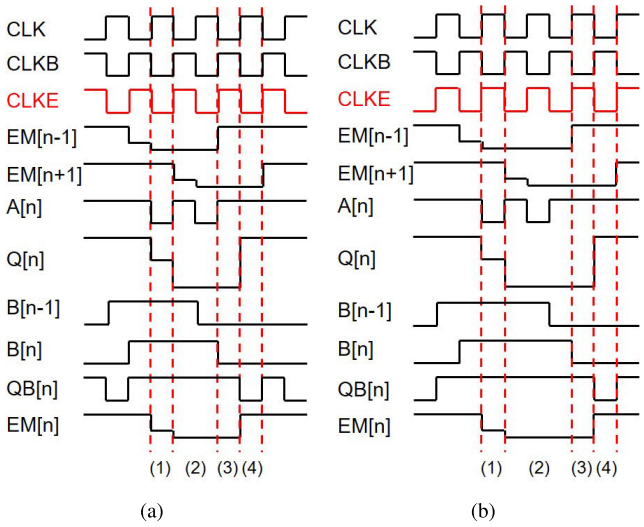


Fig. 5. Timing diagram for the proposed EM pulse generation circuit. (a) Even multiple pulsewidth of a line time. (b) Odd multiple pulsewidth of a line time. While even multiples are generated by CLKE equal to CLKB, odd multiples are given rise to by CLKE equal to CLK. It is assumed that EM[$n-1$] has the rising transition at the low pulse of CLK. There are four steps: 1) pulling-down; 2) capacitive-coupling; 3) holding; and 4) pulling-up.

$C1$ is used to enable pulling EM[n] down to VGL by coupling the falling transition of EM[$n+1$] to Q[n]. The details of the whole operation are expressed in four steps: 1) pulling-down; 2) capacitive-coupling; 3) holding; and 4) pulling-up, as shown in Fig. 5(a) and (b) for even and odd multiples of a line time, respectively. CLKE is set to be equal to CLKB for even multiples and CLK for odd multiples. Unlike Fig. 3, the proposed circuit controls the high pulsewidth by adjusting the low pulsewidth due to a fixed frame period of time.

1) *Pulling-Down*: Because the inverter of P7–P10 sets QB[n] to be high by the low voltage of EM[$n-1$], P3 and P5 are turned off as illustrated in Fig. 6(a). High CLK and low CLKB discharge A[n] to turn P4 on, leading to pull down Q[n] as well as EM[n]. However, A[n], Q[n], and EM[n] cannot be fully pulled down to VGL due to the threshold voltages of P1, P4, and P6. They are settled at VGL $+ |V_{th}|$, VGL $+ 2|V_{th}|$, and VGL $+ 3|V_{th}|$, where V_{th} is a threshold voltage. The falling transition of EM[n] always gets delayed by one line time over EM[$n-1$] since the falling transition of EM[$n-1$] is synchronized to the high pulse of CLKB and Q[n] is triggered at the low pulse of CLKB.
2) *Capacitive-Coupling*: As presented in Fig. 6(b), P4 is maintained to be turned off because its source–gate voltage is lower than V_{th}, making Q[n] floating. Therefore, the low transition of EM[$n+1$] pulls Q[n] down to the lower voltage than VGL by the capacitive coupling via $C1$. At the same time, this lower voltage of Q[n] further turns on P6 and allows EM[n] to be fully discharged to VGL. During the period of low EM[$n-1$], since QB[n] and Q[n] are maintained at high and low voltage levels, respectively, EM[n] is kept at VGL regardless of CLK, CLKB, and CLKE.
3) *Holding*: To make the delay of a line time at the rising transition over EM[$n-1$], the low level of EM[n] must be maintained even at the high voltage of EM[$n-1$] during one line time. As shown in Fig. 6(c), CLKE is asserted at high through P10, which keeps turning off P3 and P5. Because EM[$n-1$] is high, A[n] stays at VGH, turning P4 off. At the same time, Q[n] and EM[n] are maintained at low. In this period, it is very important to set the level of CLKE to high in order to turn P3 and P5 off. Therefore, the phase of CLKE should be adjusted depending on whether the pulsewidth is odd or even multiple of a line time.
4) *Pulling-Up*: As depicted in Fig. 6(d), Q[n] and EM[n] are pulled up to VGH through P3 and P5 turned on by the low pulse of CLKE. Even though QB[n] follows the pulse levels of CLKE, the high voltage levels of Q[n] and EM[n] are maintained at the floating state for the high pulse of CLKE due to P4 and P6 turned off. This step turns off P11 and reduces the coupling effect between Q[n] and EM[$n+1$] owing to the small parasitic capacitor between the source and gate nodes of P11.

In particular, the proposed circuit copes with two issues of increased power consumption over EM pulse widths and undesired coupling effects through $C1$ from EM[$n+1$] in the previous one [24]. First, conventional one-type TFT inverters have employed a diode-connected load of P8, giving rise to the shoot-through current paths that contribute to the increased power consumption as shown in Fig. 7(a). In addition, the longer pulsewidth increases shoot-through intervals further, leading to larger power consumption. However, as presented in Fig. 7(b), an internal inverter of P7 and P8 in the proposed circuit does not use P8 as a diode-connected load but controls it by B[$n-1$] that is the inverter output of a previous stage. Because the shoot-through current path takes place only during one line time, the proposed circuit dramatically reduces the variation of the power consumption over EM pulse widths.

Second, $C1$ is adopted to pull EM[n] down fully to VGL by the capacitive coupling effect from the falling transition of EM[$n+1$] to Q[n]. This coupling effect can be achieved simply by directly connecting Q[n] and EM[$n+1$] through

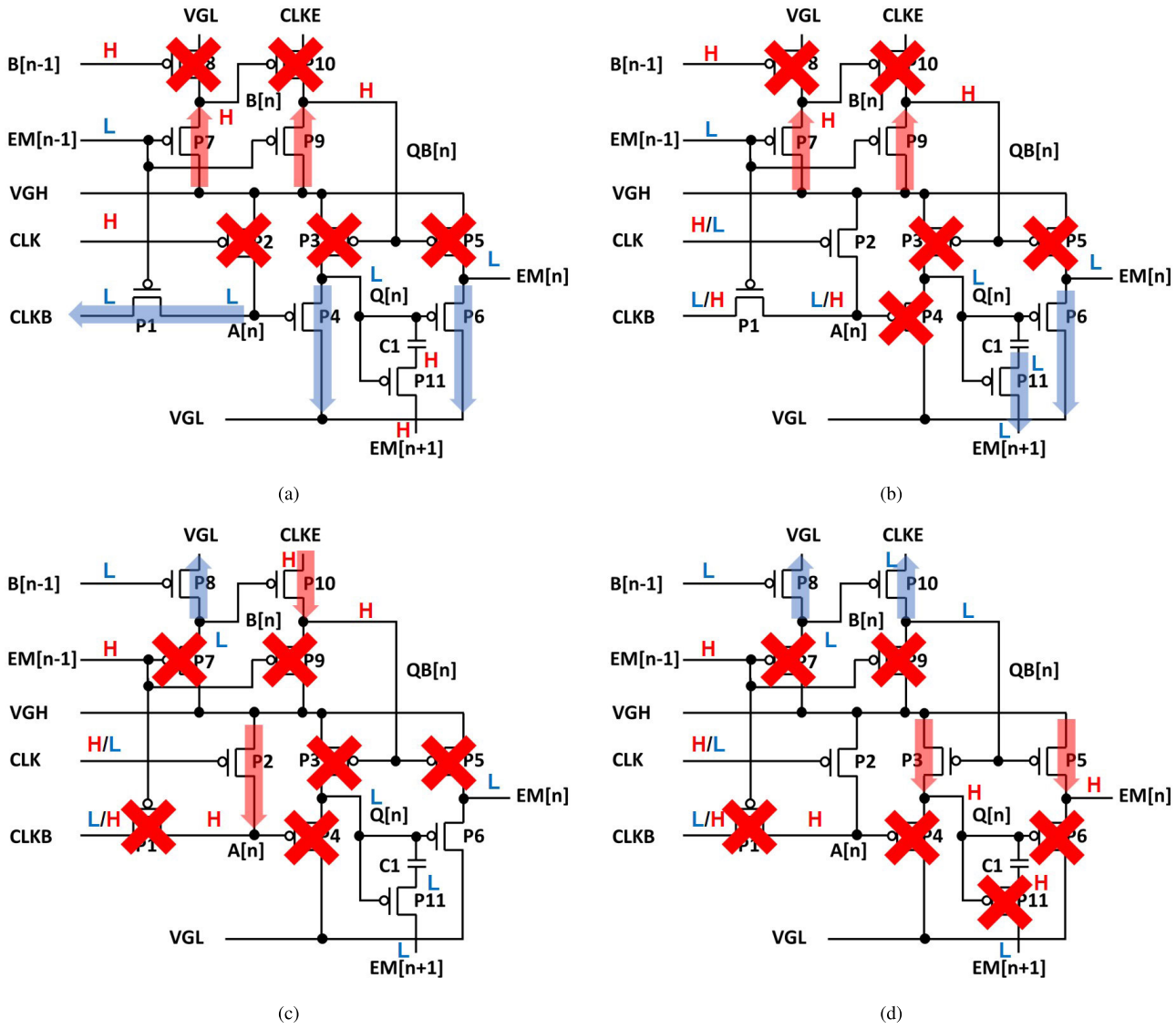


Fig. 6. Four step operations of the proposed EM circuit. (a) Pulling-down. (b) Capacitive-coupling. (c) Holding. (d) Pulling-Up.

$C1$ without P11. However, Q[n] and EM[n] can also get the undesired capacitive coupling effect from the rising transition of EM[n+1]. As illustrated in Fig. 8(a), when the pulse widths are even multiples of a line time, the capacitively coupled voltage at the rising transition of EM[n+1] is lowered to VGH via P4 due to the high voltage of A[n] asserted by VGH. A[n] is connected to VGH through P2 turned on by low CLK. On the other hand, as presented in Fig. 8, A[n] gets floated by high CLK for the pulse widths of odd multiples and the falling transition of Q[n] through P4 causes the falling transition of A[n]. Because the larger capacitive load at Q[n] than at A[n] causes the voltage difference between source and gate nodes that turns P4 on, the voltages of A[n] and Q[n] keep falling for one line time, resulting in the falling ripples at EM[n]. Unfortunately, since EM[$n-1$] also experiences similar coupling noises from EM[n] and contributes to the EM[n] generation as an input, these coupling noises may bring out additional ripples at the EM[n] waveform. However, when Q[n] and EM[n+1] are connected with P11, P11 is turned off at the rising transition of EM[n+1]. As a result, the coupling capacitance between Q[n] and E[n+1] becomes very low due to the very small parasitic capacitor between the source and gate nodes of P11, reducing coupling effects at Q[n] for both even and odd multiples as shown in Fig. 9(a) and (b). Thus, the coupling noises at EM[n] are alleviated.

III. Simulation Results

The proposed EM circuit is verified by a simulation program with integrated circuit emphasis (SPICE) at a backplane of p-type LTPS TFTs with threshold voltage and mobility of -1.72 V and 62.6 cm^2/Vs, respectively. Its transfer curve is shown in Fig. 10 at channel length and width of 10 and 180 μm, respectively. High and low supply voltages of VGH and VGL are 20 and 0 V, respectively, where CLK, CLKB, CLKE, and CLKEB have voltage swings between VGH and VGL. It is assumed that capacitive and resistive loads are 150 pF and 10 kΩ, respectively, and target resolution and frame rate are 120 Hz and 3840 $\times$ 2160, respectively, where the line time is about 3.8 μs and the vertical blank length is ten lines. The channel widths of TFTs, with the minimum channel

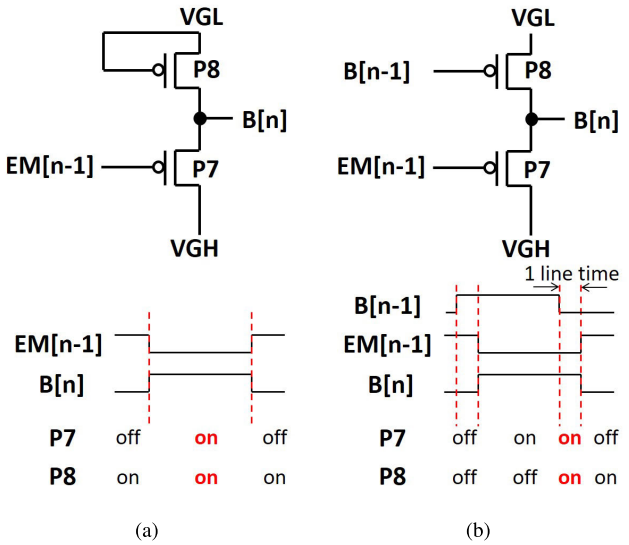


Fig. 7. Comparison on one-type TFT inverter structures. (a) Conventional diode-connected load structure. (b) Proposed structure controlled by B[$n-1$]. While EM[$n-1$] and B[$n-1$] are the EM pulse and inverter outputs of a previous stage, B[n] is the inverter output of a current stage.

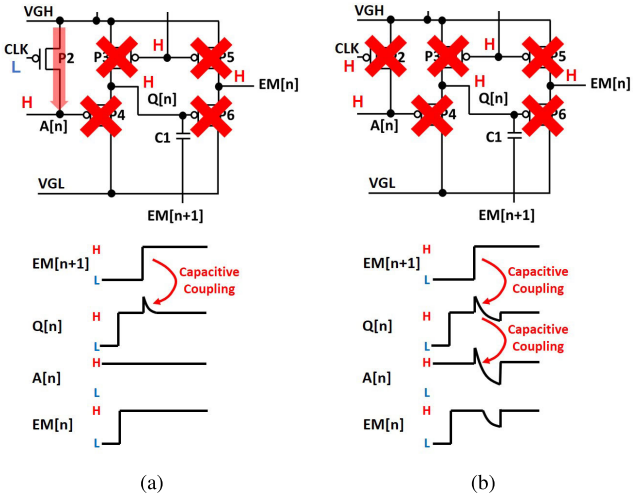


Fig. 8. Coupling effects on EM[n] by the rising transition of EM[$n+1$] when Q[n] and EM[$n+1$] is connected via $C1$ without P11. (a) Even pulsewidth. (b) Odd pulsewidth.

TABLE I
CHANNEL WIDTHS AND LENGTHS OF TFTS IN A PROPOSED EM CIRCUIT

TFT	Width	Length	TFT	Width	Length
P1	7 μm	10 μm	P2	7 μm	10 μm
P3	7 μm	10 μm	P4	7 μm	10 μm
P5	250 μm	10 μm	P6	150 μm	10 μm
P7	7 μm	10 μm	P8	7 μm	10 μm
P9	7 μm	10 μm	P10	15 μm	10 μm
P11	7 μm	10 μm			

length of 10 μm, are 7 μm for P1–P9, and P11, 15 μm for P10, 250 μm for P5, and 150 μm for P6 as summarized in Table I. $C1$ is given as 1 pF. The overall configuration of EM circuits is described in Fig. 11 and the layout of an EM circuit is presented in Fig. 12.

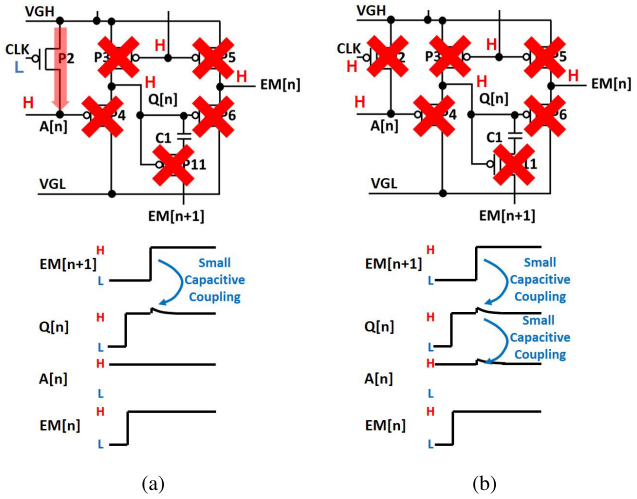


Fig. 9. Reduced coupling effects on EM[n] by the rising transition of EM[$n+1$] when Q[n] and EM[$n+1$] is connected via $C1$ with P11. (a) Even pulsewidth. (b) Odd pulsewidth.

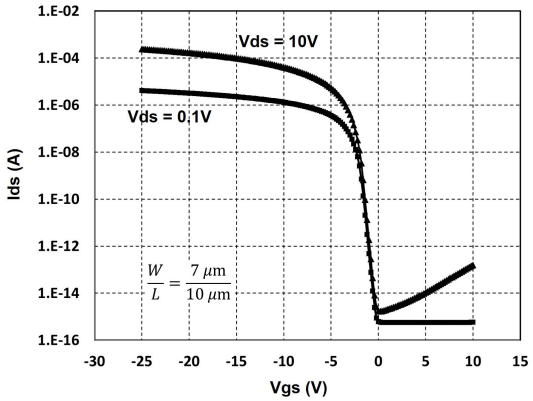


Fig. 10. Transfer curve of p-type LTPS TFT.

Among 30 stages, the 29th EM circuit is investigated to estimate the waveforms of input–output, and internal node voltages for pulse widths of even and odd multiples of a line time, as shown in Fig. 13(a) and (b), respectively. In those plots, lower negative fluctuations than VGL at B[n]-nodes are caused by the capacitive coupling from CLKE.

In addition, we verify the operation range of pulse widths from four to 2160 lines for even multiples and from three to 2159 lines for odd multiples as presented in Fig. 14. Especially, long pulse widths are described with positive pulse widths for visualization.

The coupling noises on EM[n] are also compared by means of the simulation results about the connections through $C1$ without and with P11. As described in Section II and depicted in Fig. 15, outputs of odd pulse widths without P11 include the coupling noises from the rising transitions of EM pulses of following stages while outputs of even pulse widths show no coupling noises. However, P11 ameliorates these coupling noises at even pulse widths as well as at odd pulse widths as illustrated in Fig. 16. Rising time, falling time, and coupling noise magnitude at EM pulses without and with P11 are summarized in Table II. In particular, because the capacitive

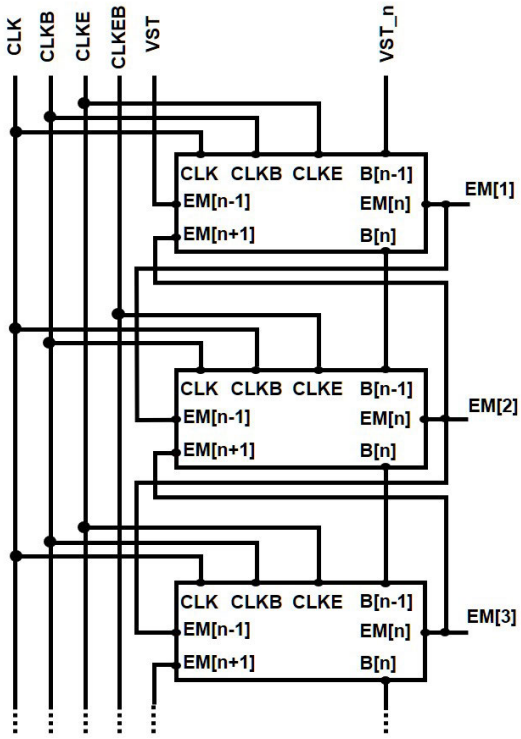


Fig. 11. Configuration of EM pulse circuits.

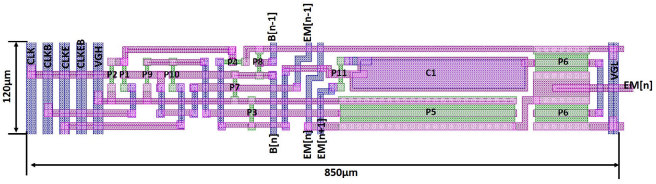
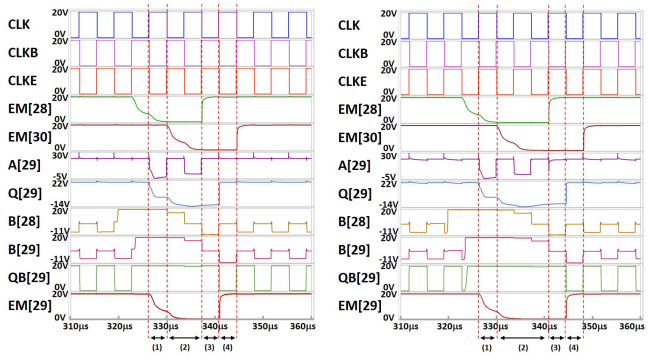


Fig. 12. Layout of the proposed EM pulse circuit.

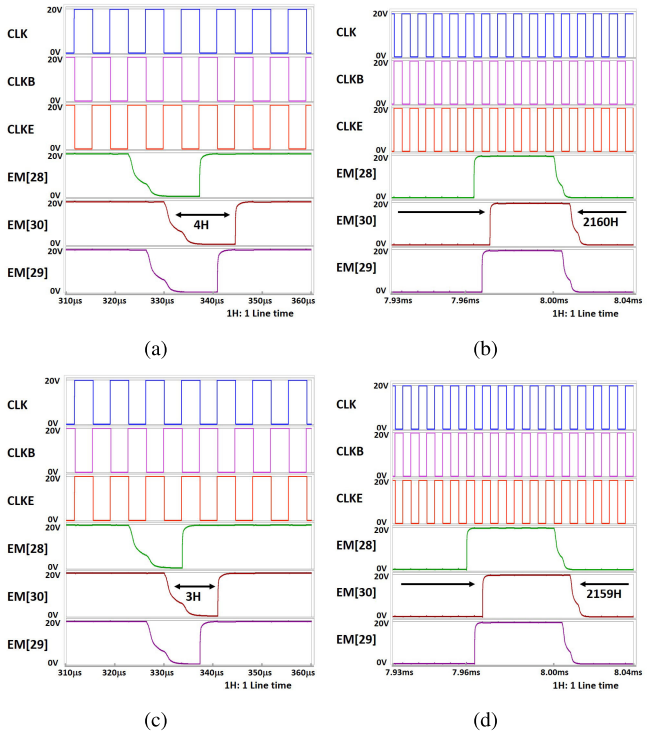


(a) (b)

Fig. 13. Simulated waveforms of inputs, outputs, and internal nodes. (a) At the even pulsewidth of four line times. (b) At the odd pulsewidth of five line times.

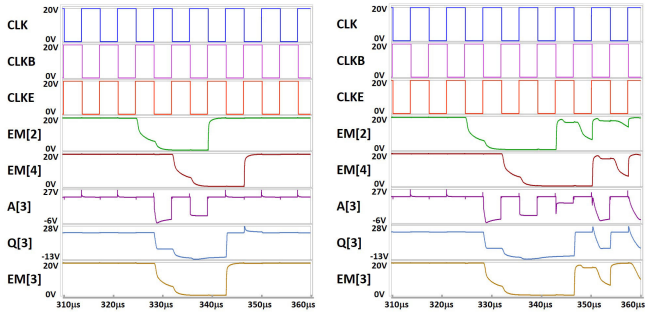
coupling occurs after EM outputs are predischarged in the pulling-down period, the falling time is estimated to be longer than one line time of 3.8 μs.

The B[$n-1$]-connected load structure of an internal inverter is evaluated by power consumption over pulse widths that are compared to the diode-connected load scheme as plotted in Fig. 17. The power consumption is estimated for EM circuits of 30 stages. Although the diode-connected load experiences large power variation from 1.26 to 76.91 mW at the pulsewidth range of 3–2159 lines, the B[$n-1$]-connected load structure



(a) (b) (c) (d)

Fig. 14. Operation range of pulse widths. (a) Short even pulsewidth of four lines. (b) Long even pulsewidth of 2160 lines. (c) Short odd pulsewidth of three lines. (d) Long odd pulsewidth of 2159 lines. For long pulse widths, high pulse widths are presented for the visualization. The low pulsewidth of 2160 lines is equal to the high pulsewidth of ten lines and the low pulsewidth of 2159 lines is equal to the high pulsewidth of 11 lines due to the vertical blank period of ten lines.

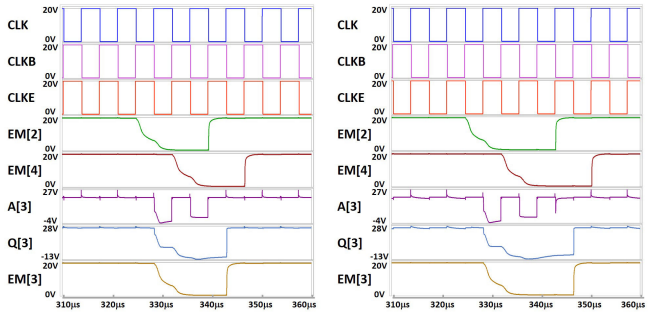


(a) (b)

Fig. 15. EM output waveforms without P11. (a) Even pulsewidth. (b) Odd pulsewidth. EM outputs of odd pulse widths suffer from the coupling noises by the rising transitions of the following output stages.

TABLE II
RISING TIME, FALLING TIME, AND COUPLING NOISE MAGNITUDE AT EM PULSES WITHOUT AND WITH P11

Conditions	Even Pulse Width		Odd Pulse Width	
	w/o P11	w/ P11	w/o P11	w/ P11
Rising Time (μs)	0.51	0.49	0.61	0.49
Falling Time (μs)	4.32	4.53	4.37	4.54
Coupling Noise (V)	0.28	0.28	14.57	0.28



(a) (b)

Fig. 16. EM output waveforms with P11. (a) Even pulsewidth. (b) Odd pulsewidth. EM outputs of both even and odd pulsewidths are robust to coupling noises from the rising transitions of the following output stages.

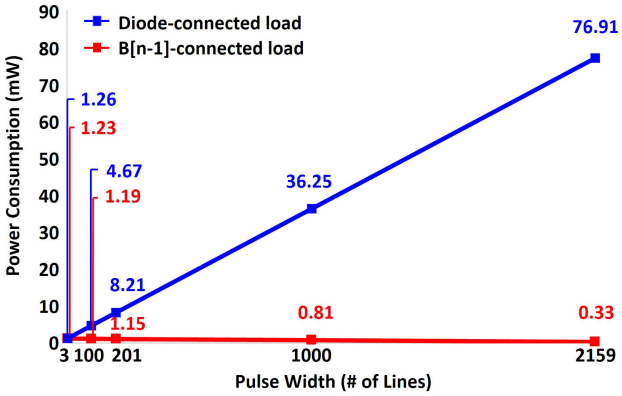


Fig. 17. Power consumption over pulse widths for EM circuits of 30 stages. Blue and red dots represent power consumption for internal inverters of diode-connected load and B[$n-1$]-connected load, respectively.

TABLE III
POWER CONSUMPTION DETAILS AT VGH AND CLOCK SIGNALS IN THE PROPOSED EM CIRCUIT

Pulse Width (Lines)	3	100	201	1000	2159
VGH (mW)	0.259	0.256	0.257	0.255	0.255
CLK/CLKB (mW)	0.007	0.007	0.008	0.008	0.011
CLKE/CLKEB (mW)	0.962	0.922	0.880	0.548	0.066

shows a very small change from 1.23 to 0.33 mW. In addition, the power consumption of the proposed circuit is divided into three parts of VGH, CLK/CLKB, and CLKE/CLKEB as summarized in Table III. As explained in Fig. 7, the power consumption from VGH is kept at the constant value of around 0.26 mW regardless of pulse widths. The power consumptions at CLK and CLKB are also maintained. On the other hand, because CLKE and CLKEB drive the large capacitive load of QB[n] only during the high voltage period of EM[$n-1$], their power consumption is reduced from 0.962 to 0.066 mW while increasing the low pulse widths of EM outputs. For the comparison, the details of the power consumption in the EM circuit with a diode-connected load inverter are also presented in Table IV. Due to the shoot-through current path between VGH and VGL, the power consumption at VGH increases from 0.300 to 70.711 mW over the EM pulsewidth. Furthermore, because the diode-connected load inverter provides a lower voltage level than VGH at the low pulse period of

TABLE IV
POWER CONSUMPTION DETAILS AT VGH AND CLOCK SIGNALS IN THE EM CIRCUIT WITH A DIODE-CONNECTED LOAD INVERTER

Pulse Width (Lines)	3	100	201	1000	2159
VGH (mW)	0.300	3.469	6.772	32.881	70.711
CLK/CLKB (mW)	0.007	0.007	0.008	0.008	0.011
CLKE/CLKEB (mW)	0.953	1.190	1.431	3.363	6.192

TABLE V
EM PULSE GENERATION CIRCUIT COMPARISON

	[20]	[21]	[22]	This Work
Backplane	n-type LTPS	LTPO	LTPO	p-type LTPS
# TFT	9	12	24	11
# Capacitor	1	0	3	1
# Clock	2	2	6	4
Pulse width Tunability	Even Multiples	No	Even Multiples	Any Multiples
Power Variance	Small	Very Small	Very Small	Small
Year	2015	2021	2022	2023

EM[$n-1$], CLKE and CLKEB cannot avoid the increasing power consumption via P10 from 0.953 to 6.192 mW over the EM pulsewidth. Finally, the EM pulse generation circuits are compared in Table V.

IV. CONCLUSION

This article demonstrates the fine-tunable EM pulse generation circuit that covers pulse widths of any multiples of a line time without the large power variation as well as the coupling noises. Unlike previous tunable EM circuits that support either odd or even multiple pulse widths, the proposed one provides pulse widths of any multiple lines by adjusting the phase of additional clock signals. Thanks to the internal inverter of the B[$n-1$]-connected load, the small variation in the power consumption from 1.23 to 0.33 mW is achieved for pulse widths from three to 2159 lines, while the diode-connected load structure shows a large variation from 1.26 to 76.91 mW. In addition, the robustness of EM pulses to coupling noises is also established by connecting Q[n] and EM[$n+1$] through the capacitor and TFT.

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