SOI LDMOS With High-k Multi-Fingers to Modulate the Electric Field Distributions

Jiafei Yao[ID], *Member, IEEE*, Mingshun Sun, Tianci Xu, Xin Liu, Man Li[ID], Jing Chen[ID], Maolin Zhang[ID], *Member, IEEE*, Jun Zhang[ID], and Yufeng Guo[ID], *Member, IEEE*

Abstract— The silicon-on-insulator (SOI) lateral double-diffused metal–oxide–semiconductor (LDMOS) with high-k multi-fingers (HKMFs) is proposed and investigated. The fingertips are distributed at specific locations to modulate the electric field distributions and improve the device performances. First, the electric field peaks formed at the fingertips could optimize the electric field distributions, which improves the breakdown voltage (BV) of the LDMOS effectively. Meanwhile, the multi-fingers are embedded into the drift region to increase the optimal drift doping concentration, which facilitates the positive conduction of the device and reduces the specific ON-resistance ($R_{on,sp}$). The simulation results show that the proposed HKMF-LDMOS with five multi-fingers increases the BV by 59.2%, reduces $R_{on,sp}$ by 37.8%, and improves the figure of merit (FOM) by 4.07 times when compared to the conventional LDMOS.

Index Terms— Breakdown voltage (BV), electric field, high-k, lateral double-diffused metal–oxide–semiconductor (LDMOS), multi-fingers, specific ON-resistance.

I. INTRODUCTION

THE lateral double-diffused metal–oxide–semiconductor (LDMOS) based on the silicon-on-insulator (SOI) structure is one of the key devices that determine the performances of the whole power integrated circuit [1]. With the rapid development of the power IC industry, LDMOS has been widely adopted due to its great compatibility with CMOS processes [2]. The tradeoff between the specific ON-resistance ($R_{on,sp}$) and breakdown voltage (BV) is a major issue to be considered in the design of SOI LDMOS [3], [4], [5], [6], [7]. In order to obtain the high breakdown characteristics and reduce the specific ON-resistance, high-k

dielectric is employed in the SOI LDMOS. One method is depositing the high-k film on the surface of the top silicon layer, which modulates the lateral electric field distribution, but has little effect on the vertical electric field and weak assisted depletion effect on the drift region [8], [9], [10]. Another method is depositing the high-k dielectric into the deep trench with the integration of variable-k technology, trench gate technology, and so on; the figure of merit (FOM) of the SOI LDMOS is significantly improved, but the fabrication process is more complex [11], [12], [13]. The application of the sidewall high-k dielectric is also an effective method to modulate the lateral and vertical electric field distributions [14], [15], [16], [17]. Moreover, the assisted depletion of the sidewall high-k dielectric to the drift region reduces $R_{on,sp}$ obviously. Therefore, the high-k dielectric applied into the SOI LDMOS can effectively balance the tradeoff between $R_{on,sp}$ and BV, ultimately improving the electrical characteristics of the SOI LDMOS.

In this article, a novel SOI LDMOS with high-k multi-fingers (HKMFs-LDMOS) is proposed. The HKMFs have different lengths so that new electric field peaks would be formed at the fingertips and modulate the around electric field distributions. Meanwhile, the drift doping concentration of the drift region is improved because of the assisted depletion of the HKMFs. Therefore, $R_{on,sp}$ and BV are both improved. The device structure and the mechanism are given in Section II. Then, the influence of the device parameters, such as the length, width, and permittivity of the HKMFs, is discussed in Section III. Finally, Section IV makes the conclusion.

II. DEVICE STRUCTURE AND MECHANISM

Fig. 1 shows the three-dimensional structure of the proposed HKMF-LDMOS. The basic concept of the design is to introduce electric field peaks in the drift region by the HKMFs with different lengths. As seen in the figure, the multiple fingers extend from the P-well into the drift region and away from the N$^+$ region of the drain side. The fingertips are distributed at specific locations so that they could lead to the electric field peaks to modulate the device performance. For the design of the HKMF-LDMOS, the lengths of the fingers are increased alternately to regulate the electric field distribution and maximize the use of the drift area for drain
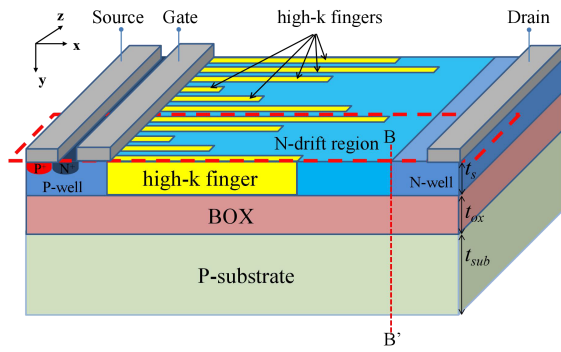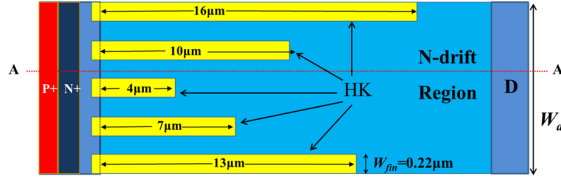
Fig. 1. 3-D structure of HKMF-LDMOS.

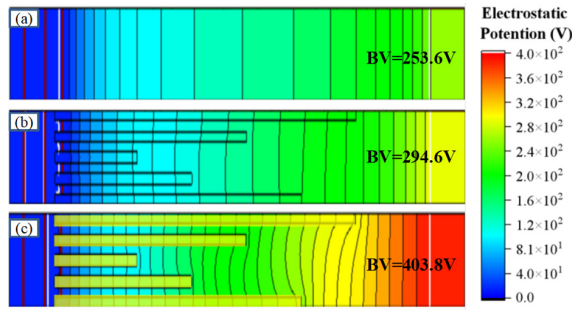Fig. 2. Top view of the basic unit for simulation.

Fig. 3. Equipotential contour plots at own optimal BV for (a) CONV-LDMOS, (b) OXMF-LDMOS, and (c) HKMF-LDMOS.

depletion. The widths of the HKMFs are optimized to maintain the silicon path. The thickness of the HKMFs is the same as the thickness of the top silicon layer.

Fig. 2 shows the basic cell's top view of the HKMF-LDMOS with five fingers, and the length values and width of each HKMF are also given in the figure. Compared to conventional LDMOS (CONV-LDMOS), the HKMF-LDMOS requires only one additional mask to form the HKMFs in the drift region. To investigate the effect of the dielectric fingers on device performance, the common parameters, e.g., the thickness of the top silicon layer (t_s) is 1 μm, the thickness of the buried oxide layer (t_{ox}) is 3 μm, the thickness of the substrate thickness (t_{sub}) is 5 μm, the length (L_d) and width (W_d) of the drift region, are 20 and 2 μm.

In order to investigate the mechanisms of HKMF-LDMOS, the 3-D device simulation software SENTAURUS is employed to perform the 3-D simulations of the CONV-LDMOS, the LDMOS filled with oxide multi-finger (OXMF-LDMOS), and HKMF-LDMOS. The physical models used in the simulation include the effective intrinsic density, doping dependence, high field saturation, enormal, SRH, auger, and avalanche (eparallel). Both the OXMF-LDMOS and HKMF-LDMOS have the same multi-fingers, and the corresponding permittivity of the dielectric fingers is 3.9 and 110. Fig. 3 shows the surface equipotential contour for the three LDMOSs at their
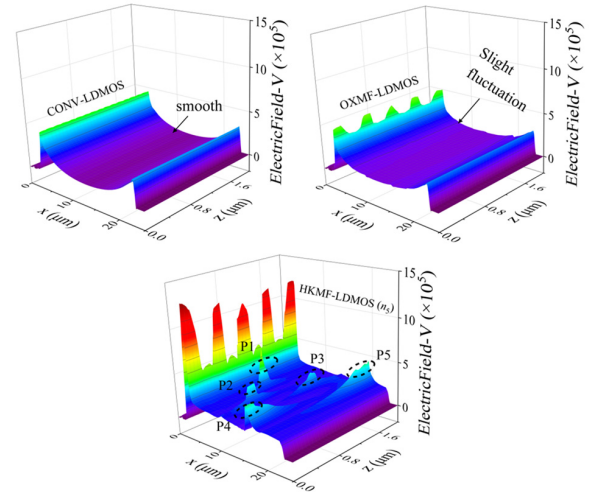

Fig. 4. 3-D distributions of the surface electric field for the three LDMOSs.

maximum BV. The maximum BV of the CONV-LDMOS is 253.6 V at the optimal drift doping concentration of 9×10^{15} cm^{-3}, the OXMF-LDMOS has the maximum BV of 294.6 V at the optimal drift doping concentration of 1.3×10^{16} cm^{-3}, and the HKMF-LDMOS reaches the maximum BV of 403.8 V at the corresponding doping concentrations of 2.6×10^{16} cm^{-3}. As shown in Fig. 3(a), the equipotential lines of the CONV-LDMOS are mainly concentrated at both ends of the drift region, but spreading toward the middle of the device. The application of the OXMFs in the OXMF-LDMOS results in a less sparse potential distribution in the middle of the drift region, which increases the BV when compared to the conventional one. For the HKMF-LDMOS, the potential distribution at both ends of the drift region becomes significantly more uniform and the equipotential lines move closer to the middle part of the drift region. As a result, the maximum BV of 403.8 V for the HKMF-LDMOS increases 59.2% when compared to the BV of the CONV-LDMOS.

Fig. 4 plots the three-dimensional surface electric field distributions for the CONV, OXMF, and HKMF-LDMOS at the top of the drift region. The surface electric field of the CONV-LDMOS is smoothly distributed like a U-shaped. For the OXMF-LDMOS, the oxide fingers lead to a slight fluctuation in the surface electric field of the drift region. When the HKMFs have been applied in the drift region, new electric field peaks P1, P2, P3, P4, and P5 are formed at the fingertips and affect the related area on both sides of the fingertips. Meanwhile, the electric field of the N-drift/N$^+$ junction has been reduced, which avoids the premature breakdown at this junction. Note that, there are five electric field peaks on the left side of the figure, and these electric field peaks occur in the high-doped P-well region caused by HKMFs extents into the P-well, which has no effect on the breakdown characteristic of the drift region. Therefore, the BV can be improved by modifying the surface electric field using the HKMFs.

To make a clear contrast, Fig. 5(a) shows the two-dimensional surface electric field distribution along the AA' line for the three LDMOSs. It can be seen that the oxide fingers
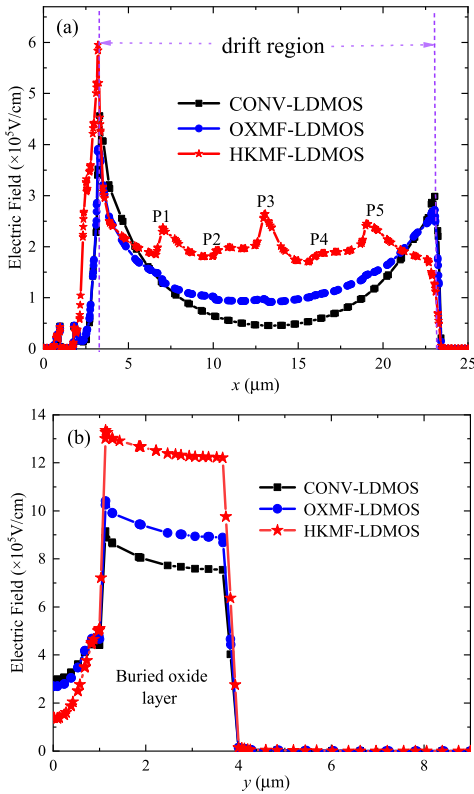
Fig. 5. (a) Surface electric field distributions. (b) Vertical electric field at the drain end for the three LDMOSs.
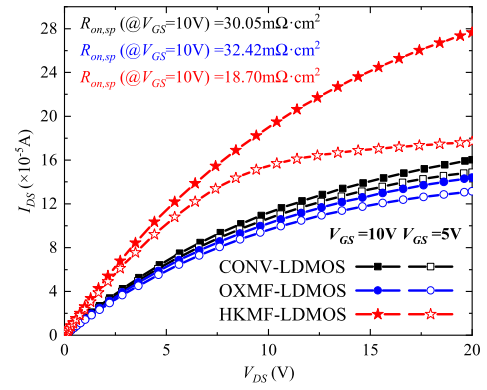

Fig. 6. Output characteristics of the three LDMOSs.

Fig. 7. Transfer characteristics of the three LDMOSs.

have improved the middle electric field distribution, but no distinct electric field peaks formed. For the HKMF-LDMOS, new electric field peaks are obviously formed in the drift region and further increasing the electric field distribution. The reduction of the electric field at the right edge also enhances the device breakdown performance. Fig. 5(b) shows the vertical electric field at the drain (along the BB' line in Fig. 1) for the three LDMOSs. The vertical electric field of the HKMF-LDMOS is lower at the surface ($y = 0$ μm), but higher at the interface of the top silicon layer and buried oxide layer. It is obvious that the vertical electric field in the buried oxide is highest for the HKMF-LDMOS, which achieves 1.3×10^{6} V/cm. Compared to the CONV-LDMOS, the HKMF-LDMOS is able to increase the peak vertical electric field by approximately 44%, thus increasing the vertical BV effectively. Therefore, the HKMFs not only modify the surface electric field but also improve the vertical electric field, leading to the significant increment in the breakdown characteristic.

The output characteristics of the three LDMOSs at $V_{\mathrm{GS}} = 10$ V and $V_{\mathrm{GS}} = 5$ V are shown in Fig. 6. Compared to the CONV-LDMOS and the OXMF-LDMOS, the HKMF-LDMOS has a greater slope of the $I_{\mathrm{DS}}-V_{\mathrm{DS}}$ curve in the linear region and higher saturation current in the saturated region. The doping concentration increased by the modulation of the HKMFs, which facilitates the positive conduction of the device and reduces the ON-resistance of the device. The calculated specific ON-resistance of the HKMF-LDMOS is 18.7 m$\Omega\cdot$cm^2 at $V_{\mathrm{GS}} = 10$ V, a 37.8% reduction when compared to $R_{\mathrm{on,sp}}$ of the CONV-LDMOS.
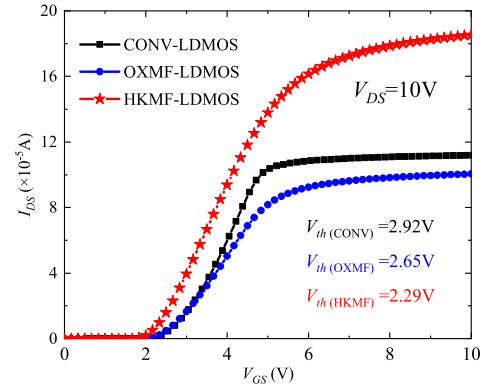
The transfer characteristics of the three LDMOSs are given in Fig. 7. As the HKMFs are partly extended into the P-well region, they have little modulation effect on the channel region. This is why the LDMOS could be turned on at a lower threshold voltage (V_{th}). The simulation results show that the threshold voltage of HKMF-LDMOS is 2.29 V, which is reduced by 22% when compared to 2.92 V of the CONV-LDMOS.

Fig. 8 shows the switching characteristics of the three LDMOSs. The test circuit for simulating the switch characteristics is shown in the subgraph of Fig. 8(a). The applied voltage V_{DD} is 100 V, the added load resistance is 3×10^{6} Ω, and the gate resistance is 100 Ω. The proposed HKMF-LDMOS has an ON-state time of about 0.35 ns and an OFF-state time of about 3.5 ns, while the CONV-LDMOS has an ON-state time of about 0.3 ns and an OFF-state time of about 2.5 ns. Studies have shown that the introduction of high-k dielectric would result in charge accumulation at the gate, thereby increasing the gate–drain capacitance and affecting the switching characteristics of the LDMOS. Overall, the switching characteristics of the proposed HKMF-LDMOS do not degrade much, while other excellent properties of HKMF-LDMOS have been obtained.

III. RESULTS AND DISCUSSION

The length and width of the HKMFs are the main parameters for the HKMF-LDMOS. First, the influences of the finger length on the BV, $R_{\mathrm{on,sp}}$, and FOM are discussed. The length of the base finger is half of the drift region length, which is defined as $L_b = L_d/2 = 10$ μm in this case. The other
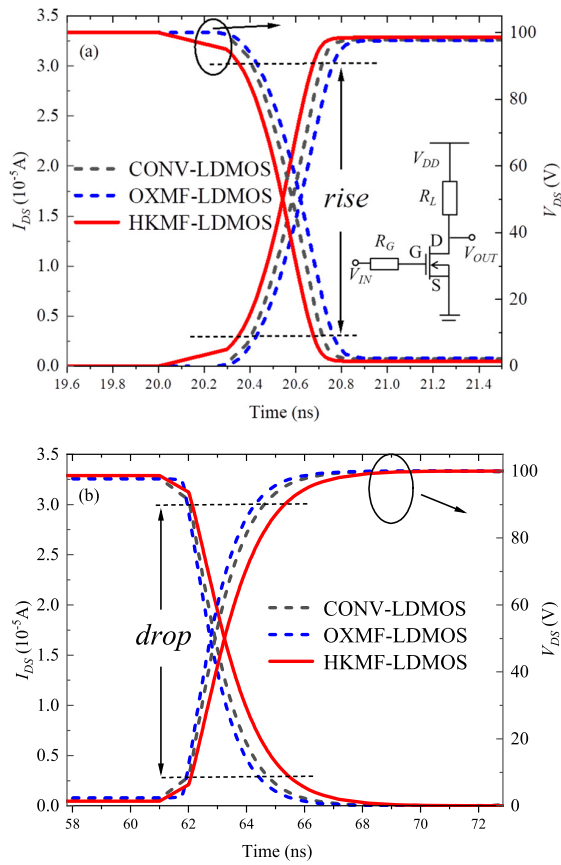
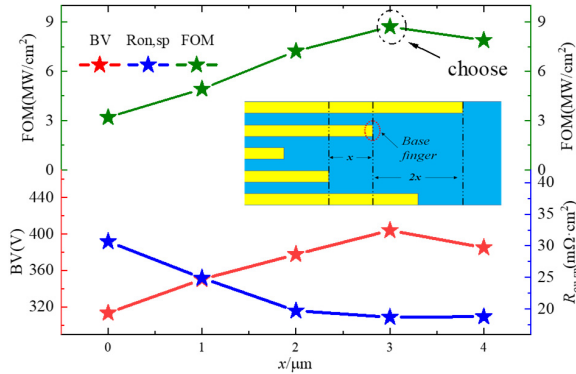Fig. 8. Switching characteristic for the different LDMOSs. (a) Turn-on. (b) Turn-off.

Fig. 9. BV, $R_{on,sp}$, and FOM at different x's (μm).

fingers are defined with the lengths of $L_b \pm x$ (μm) and $L_b \pm 2x$ (μm). Then, the shortest finger is arranged in the middle of the drift region and the longest finger is arranged at the side of the drift region along the z-direction. Fig. 9 shows the dependences of the BV, $R_{on,sp}$, and FOM on x. When $x = 0$ μm, the finger's lengths are the same, and each finger has the same effect on the modulation of electric field, thus not able to maximize the FOM. The results indicate that the FOM of the LDMOS with the same length high-k fingers (HK-LDMOS) is only 3.2 MW/cm^2. When $x > 0$ μm, the fingers with different lengths form the electric field peaks to modulate the electric field distributions so that the BV has been increased. Meanwhile, the silicon area becomes V-shape from drain to source and enhances the conduction to reduce the ON-resistance. The highest BV reaches over 400 V and $R_{on,sp}$
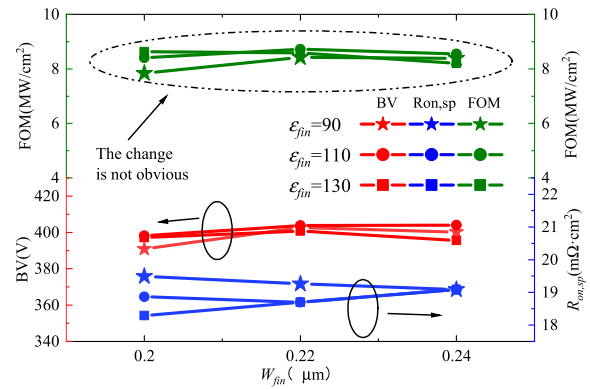

Fig. 10. BV, $R_{on,sp}$, and FOM at $\varepsilon_{fin} = 90$, 110, and 130 with different finger widths.
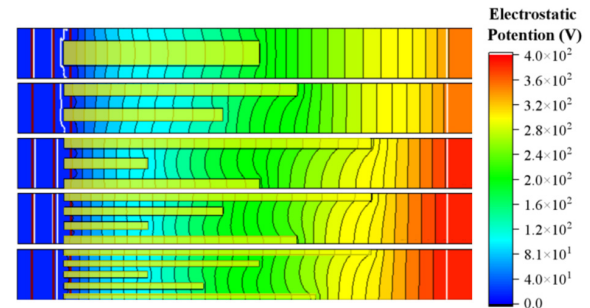

Fig. 11. Equipotential contour at own optimal BV for the HKMF-LDMOS with different n_i's ($i = 1$–5).

reduces under 20 m$\Omega\cdot$cm^2. When $x = 3$ μm, the FOM reaches the maximum value of 8.72 MW/cm^2. However, the shortest and longest HK fingers approach both ends of the drift region as x continues to increase, which weakens the modulation effect on the electric field and decreases the BV.

Next, the influence of the finger width (W_{fin}) on the performance of HKMF-LDMOS is discussed. The width of the basic simulation unit is fixed at 2 μm. To place the HKMFs but maintain the silicon path, the HKMFs and silicon path use the approximate width. The BV, $R_{on,sp}$, and FOM with different permittivities (ε_{fin}) under different W_{fin}'s are shown in Fig. 10. It can be seen that the width of the HKMFs has little impact on the FOM of the device and then leaves a certain error range in the preparation of the actual device. In this article, a finger width of 0.22 μm is selected for the HKMF-LDMOS with five fingers, and the optimal FOM was obtained at $\varepsilon_{fin} = 110$.

The number of fingers is another important parameter for the HKMF-LDMOS. The influences of the finger number on the LDMOS characteristics are discussed as follows. The finger number n_i is set as 1–5 and the lengths and widths of the fingers are optimized for different n_i's. The design principle is to control the width of the HKMFs approach to the silicon path between the fingers, and the fingertips are symmetrical to the base finger. Then, the drift doping concentration is optimized to obtain the maximum BV. Fig. 11 shows the equipotential contours for the HKMF-LDMOS with different n_i's when they reach their own maximum BV at their own optimized drift doping concentration. According to this figure, the equipotential lines become more uniform when the HKMF-LDMOS has more fingers. The three-dimensional
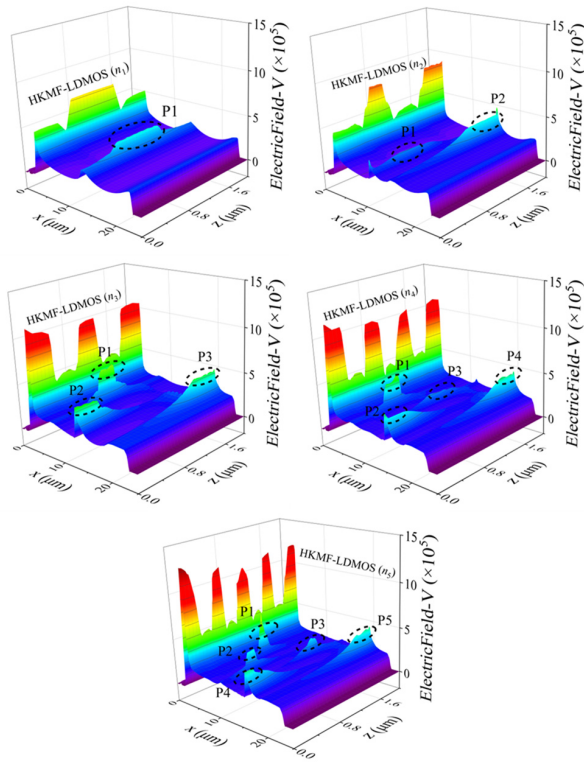
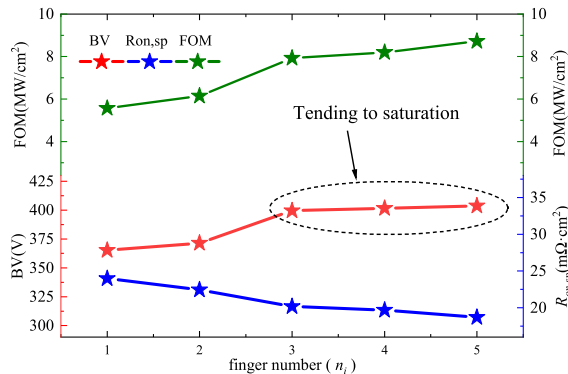Fig. 12. 3-D surface electric field distribution of the HKMF-LDMOS with different n_i's ($i = 1–5$).

Fig. 13. Comparison of BV, $R_{on,sp}$, and FOM with an increasing number of fingers.

Fig. 14. Comparative of BV, $R_{on,sp}$, and FOM for HKMF-LDMOS with one finger (n_1), three fingers (n_3), and five fingers (n_5).

Fig. 15. Comparison of the output characteristics of the CONV and the HKMF at different n_i's ($i = 1–5$).

surface electric field distributions for the HKMF-LDMOS with different n_i's are given in Fig. 12. Obviously, the new electric field peaks are formed at the fingertips and the peak width is depending on the finger width. The more HK fingers, the more electric field peaks are formed, leading to the better electric field distributions. However, more fingers mean that the widths of the HK fingers and silicon paths become narrower, which reduces the electric field modulation effect and increases the process accuracy.

After optimizing the design of the HKMF-LDMOSs with different n_i's, the BV, $R_{on,sp}$, and FOM versus the finger number n_i are given in Fig. 13. It can be seen that the BV increases with increasing of the high-k finger number due to the enhancement of the electric field modulation effect. However, the BV trends to saturation because of the RESURF effect. Also, as the finger number increases, the drift doping
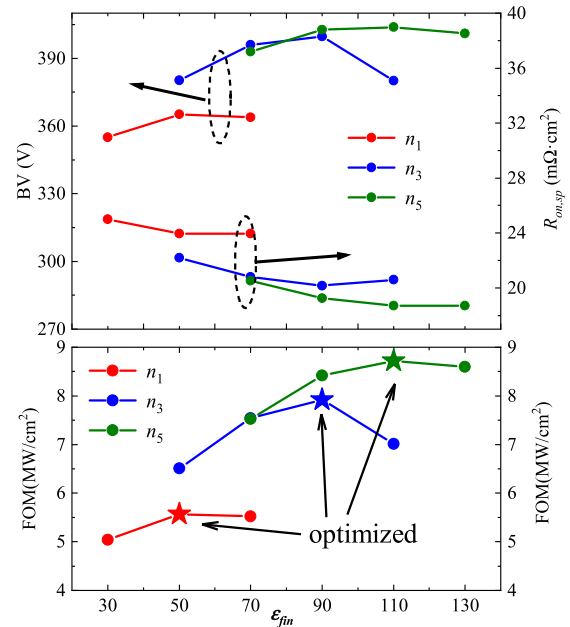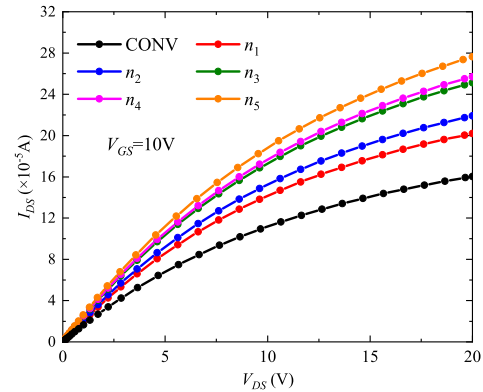
concentration has continued to increase, thus reducing the specific ON-resistance. Therefore, the FOM is increased when the finger number is increased, which indicated that the HKMF number has a relatively significant enhancement on the HKMF-LDMOS. Fig. 14 shows the BV, $R_{on,sp}$, and FOM versus the permittivity ε_{fin} for the HKMF-LDMOS with one finger (n_1), three fingers (n_3), and five fingers (n_5). The higher permittivity could optimize the potential and electric field distribution to improve the BV and increase the drift doping concentration to reduce $R_{on,sp}$. However, the BV is decreased when continuing to increase ε_{fin} because of the rapid breakdown near the drain [10]. Therefore, there is an optimized FOM for the HKMF-LDMOS with different n_i's. The max FOM is 8.72 MW/cm^2 for the HKMF-LDMOS with five fingers at $\varepsilon_{fin} = 110$, which is about 4.07 times of the FOM of 2.14 MW/cm^2 for the CONV-LDMOS with the same geometry size.

The output characteristics and transfer characteristics for the HKMF-LDMOS with different n_i's are plotted and analyzed. As shown in Fig. 15, I_{DS} of the HKMF-LDMOS is higher than that of the CONV-LDMOS at the same V_{DS}, and I_{DS}
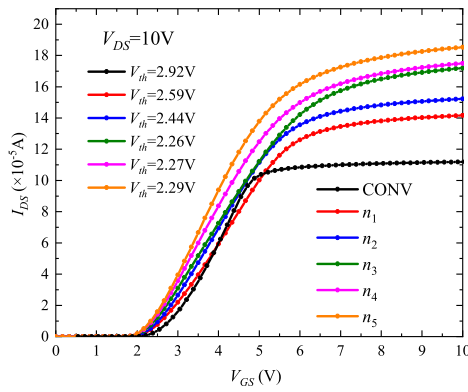
Fig. 16. Comparison of the transfer characteristics of the CONV and the HKMF at different n_i's ($i = 1$–5).
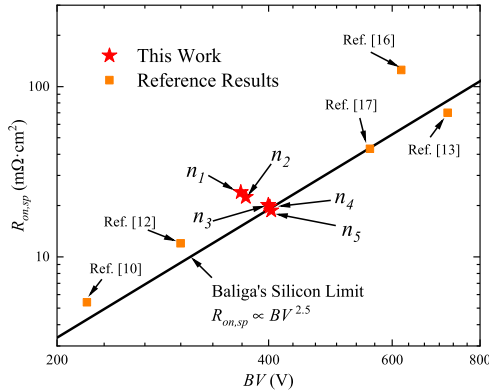

Fig. 17. $R_{on,sp}$ against BV between this work and other reported work.

increases with increasing n_i because HKMFs improve the drift doping concentration to reduce $R_{on,sp}$. Therefore, the HKMF-LDMOS with five fingers has the best output characteristics and the lowest ON-resistance. The specific ON-state resistance of 18.7 m$\Omega\cdot$cm^2 for the HKMF-LDMOS (n_5) is reduced by 37.8% when compared to $R_{on,sp}$ of 30.05 m$\Omega\cdot$cm^2 for the CONV-LDMOS. The transfer characteristics of the different LDMOSs are shown in Fig. 16. The threshold voltages of the HKMF-LDMOS are lower than those of the CONV-LDMOS because the HKMFs modulate the channel region. When the HKMF-LDMOS has more high-k fingers, the saturation current is improved and the threshold voltage is reduced because the drift doping concentration is increased with more high-k fingers. These two figures indicate that the HKMF-LDMOS has a better static characteristic than the CONV-LDMOS.

Fig. 17 compares the relationship between the $R_{on,sp}$ and BV of the HKMF-LDMOS with different finger numbers n_i, together with other reported works. As seen in this figure, the device performance of the HKMF-LDMOS is close to Baliga's silicon limit with the increase of finger number n_i. The HKMF-LDMOS with n_5 breaks the silicon limit, which indicates the superior performance of the proposed LDMOS. This figure also shows that the HKMF-LDMOS has the same or even better performance than some reported technologies.

IV. CONCLUSION

The novel HKMF-LDMOS is proposed to modulate the electric field distributions for improving the device performance. First, the mechanism of the modulation effect of the HKMFs is investigated. The HKMFs not only form additional electric field peaks at the fingertips to optimize the electric field distributions but also improve the conductor ability by increasing the drift doping concentration. Then, the parameters, such as the length, width, and permittivity of the multi-fingers, are optimized to obtain the best electrical characteristics. The breakdown characteristic, transfer characteristic, output characteristic, and switching characteristic have been discussed. The simulation results show that the proposed HKMF-LDMOS with five fingers has the FOM of 8.72 MW/cm^2, which is 2.73 times and 4.07 times compared to 3.2 MW/cm^2 of the HK-LDMOS and 2.14 MW/cm^2 of the CONV-LDMOS. Therefore, the proposed HKMF-LDMOS can effectively balance the tradeoff between $R_{on,sp}$ and BV.

REFERENCES

[1] K. S. Nikhil, N. DasGupta, A. DasGupta, and A. Chakravorty, "SOI-LDMOS transistors with optimized partial n$^+$ buried layer for improved performance in power amplifier applications," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4931–4937, Nov. 2018.

[2] C. Zhang et al., "Super field plate technique that can provide charge balance effect for lateral power devices without occupying drift region," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 2218–2222, May 2020.

[3] K. N. Kaushal and N. R. Mohapatra, "A zero-cost technique to improve ON-state performance and reliability of power LDMOS transistors," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 334–341, 2021.

[4] B. Duan, Y. Wang, Y. Wang, Z. Dong, and Y. Yang, "Novel vertical power MOSFET with step Hk insulator close to super junction limit relationship between breakdown voltage and specific ON-resistance by improving electric field modulation," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5048–5054, Oct. 2021.

[5] M. Li, D. Chen, D.-S. Jung, and X. Shi, "A novel 500–700 V ultra high-voltage LDMOS with low on-state resistance by multiple local RESURF enhancement technology," in *Proc. China Semiconductor Technol. Int. Conf. (CSTIC)*, Mar. 2019, pp. 1–3.

[6] J. Wei et al., "Analyses and experiments of ultralow specific on-resistance LDMOS with integrated diodes," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 1161–1165, 2021.

[7] Z. Cao, B. Duan, H. Song, F. Xie, and Y. Yang, "Novel superjunction LDMOS with a high-K dielectric trench by TCAD simulation study," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2327–2332, May 2019.

[8] J. Li, P. Li, W. Huo, G. Zhang, Y. Zhai, and X. Chen, "Analysis and fabrication of an LDMOS with high-permittivity dielectric," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1266–1268, Sep. 2011.

[9] J. Deng, J. Cheng, and X. B. Chen, "An improved SOI p-channel LDMOS with high-k gate dielectric and dual hole-conductive paths," *IEEE Electron Device Lett.*, vol. 38, no. 12, pp. 1712–1715, Dec. 2017.

[10] J. Yao et al., "Double dielectrics enhancement on the LDMOS using high-K field dielectric and low-K buried dielectric," *Results Phys.*, vol. 38, Jul. 2022, Art. no. 105599.

[11] H. Li, H. M. Huang, and X. B. Chen, "An improved SOI trench LDMOST with double vertical high-K insulator pillars," *J. Semiconductors*, vol. 39, no. 9, pp. 65–70, Sep. 2018.

[12] J. Cheng et al., "Potential of utilizing high-k film to improve the cost performance of trench LDMOS," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 3049–3054, Jul. 2019.

[13] Z. Cao, Q. Wang, and L. Jiao, "Analytical study on a 700 V triple RESURF LDMOS with a variable high-K dielectric trench," *IEEE Trans. Electron Devices*, vol. 68, no. 6, pp. 2872–2878, Jun. 2021.

[14] Y. F. Guo and J. F. Yao, "A lateral power device with high-K insulator," Chinese Patent CN1 032 193 86B, Jan. 20, 2016.

[15] W. Xiao-Wei et al., "Mechanism and optimal design of a high-K dielectric conduction enhancement SOI LDMOS," *Acta Phys. Sinica*, vol. 62, no. 23, 2013, Art. no. 237301.

[16] Y. Guo, J. Yao, B. Zhang, H. Lin, and C. Zhang, "Variation of lateral width technique in SoI high-voltage lateral double-diffused metal–oxide–semiconductor transistors using high-k dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 3, pp. 262–264, Mar. 2015.

[17] J.-F. Yao, Y.-F. Guo, Z.-Y. Zhang, K.-M. Yang, M.-L. Zhang, and T. Xia, "Numerical and analytical investigations for the SOI LDMOS with alternated high-K dielectric and step doped silicon pillars," *Chin. Phys. B*, vol. 29, no. 3, Feb. 2020, Art. no. 038503.