Editorial
Special Issue on Dielectrics for 2-D Electronics

IT IS our great pleasure to introduce this Special Issue on Dielectrics for 2-D Electronics to the IEEE TRANSACTIONS ON ELECTRON DEVICES readership. This Special Issue features the latest research aiming to clarify which would be the most suitable dielectric materials for state-of-the-art electronic devices containing 2-D materials.

Since their first fabrication in 2004 [1], 2-D materials have shown outstanding physical, chemical, mechanical, electronic, thermal, optical, and magnetic properties in multiple proof-of-concept laboratory experiments [2]. However, exploiting such properties to fabricate advanced solid-state electronic devices and circuits requires overcoming multiple manufacturing challenges. In 2017, 2-D materials were mentioned for the first time in the international roadmap of devices and systems (IRDS) as a potential solution for "channel material technology inflection," and since 2020, IRDS reports also consider 2-D materials as a potential solution for "beyond-CMOS as complementary to mainstream CMOS" [3]. Some products including 2-D materials are already being commercialized, although the 2-D materials are mainly used for low-integration-density sensors [4], [5].

The introduction of 2-D materials in high-integration-density circuits, such as transistor-based memories and microprocessors, still requires considerable research efforts. In 2019, TSMC and IMEC reported a breakthrough in the integration of 2-D materials in ultrascaled solid-state microelectronic devices and presented the first mass-production-compatible 2-D materials-based field-effect transistors (FETs) with channel lengths below 100 nm [6], [7]. However, the interaction of 2-D materials with adjacent traditional dielectrics (e.g., SiO_2, HfO_2, Al_2O_3, and TiO_2) is highly challenging; while the (theoretical) absence of dangling bonds in the 2-D materials provides enormous opportunities, the large number of defects at the interface to the insulators can have a dramatic impact on the performance and reliability of the FETs. The presence of native defects in 2-D materials synthesized with industry-compatible techniques (such as chemical vapor deposition) also involves numerous challenges. In this Special Issue, we delve deep into the problem of dielectrics for 2-D electronics from different points of view through eight articles.

The first group is composed of three reviews covering the existing literature and proposing solutions to different challenges that need to be overcome in the next few years. In the first review article [A1], Lin et al., from Taiwan Semiconductor Manufacturing Company, provide a general overview of the most suitable dielectric materials for 2-D FETs. Issues like band gap, dielectric constant, equivalent oxide thickness, dielectric field, subthreshold swing, and carrier mobility are extensively analyzed. In the second review article [A2], Prof. Tian, from Tsinghua University, and Dr. Peng, from the Chinese Academy of Sciences, expand 2-D dielectrics to other applications beyond transistors, such as radiofrequency switches, emerging resistive-switching memories, and neuromorphic devices. The article also discusses the most advanced examples of circuit-level integration based on 2-D materials, as well as challenges like variability and yield. These two articles provide a fairly complete review of the latest understanding of 2-D dielectrics while the third review article [A3] by Prof. Yu from the Nanjing University of Posts and Telecommunications and Prof. Wu from East China Normal University analyzes defect formation in dielectrics for 2-D electronics using transmission electron microscopy. The article focuses on understanding the density of native defects in the dielectrics and the nature of defect formation under electric field (from stress-induced leakage current to dielectric breakdown) in van der Waals materials.

The second part of the Special Issue is composed of five research articles presenting novel properties of dielectrics. The first technical article [A4] by Ang from the Singapore University of Technology and Design discusses the dielectric properties of lanthanum oxyhalide monolayers using atomistic calculations. The second article [A5] by Sharma et al. from the Indian Institute of Technology Mandi discusses the performance of transistors based on HfS_2 semiconducting channel and ZrO_2 as a gate dielectric. The authors have achieved a competitive subthreshold slope of 65 mV per decade and mobilities of 74 $cm^2 \cdot V^{-2} \cdot s^{-1}$ at gate voltages of 2 V, a quite low operating voltage within the reported 2-D FET prototypes. The third contributed article [A6] by Kee et al. from the Singapore University of Technology and Design presents the scaling of trap-limited current in ultra-thin dielectrics. Their analysis concludes that the estimated carrier mobility can be significantly different from the traditional calculations for 3-D structures, and they suggest that the strip contact geometry will always lead to a larger current flow than edge contacts.

The last two technical articles of this Special Issue cover other types of devices. In the fourth technical article [A7], Prof. Roldan from the University of Granada and Prof. Lanza from the King Abdullah University of Science and Technology discuss the variability of the currents across memristors made of metallic electrodes with multilayer hexagonal boron nitride in between. Finally, the fifth and last technical article [A8] by Prof. Lai from Chang Gung University presents the fabrication of photodetectors with Al_xO_y nanoparticles sandwiched by graphene and MoS_2 electrodes, which achieved

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a photoresponsivity of 6.24 A/W, a quantum efficiency of 2120% and a detectivity of $1.79 \cdot 10^{10}$ Jones when receiving an optical power of 10 $\text{mW} \cdot \text{cm}^2$.

Overall, the articles of this Special Issue cover multiple experiments and simulations and provide valuable conclusions that generate new state-of-the-art knowledge in this field. We believe that it will be a very valuable contribution to the readers of IEEE TRANSACTIONS ON ELECTRON DEVICES and to the entire micro/nano-electronics community, in general. Many of the contributions are from world-leading scientists in the field of 2-D materials. We would like to thank the former Editor-in-Chief of the journal, Prof. Giovanni Ghione, for giving us the opportunity to produce this Special Issue, and also to the newly appointed Editor-in-Chief, Prof. Patrick Fay, for guiding us during the editorial process and for approving the extended length of some of the review articles. We also would like to thank Marlene James for helping us to coordinate the call for papers and the review and editorial process for all the manuscripts. We sincerely hope that you enjoy reading these articles in this Special Issue which aims to provide a better understanding of these new electronic devices for the benefit of mankind.

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APPENDIX: RELATED ARTICLES

[A1] Y. C. Lin et al., "Dielectric material technologies for 2-D semiconductor transistor scaling," *IEEE Trans. Electron Devices*, early access, Nov. 28, 2022, doi: 10.1109/TED.2022.3224100.
[A2] A. Liu, X. Peng, S. Peng, and H. Tian, "Dielectrics for 2-D electronics: From device to circuit applications," *IEEE Trans. Electron Devices*, early access, Nov. 21, 2022, doi: 10.1109/TED.2022.3220483.
[A3] C. Luo et al., "Probing gate dielectrics for two-dimensional electronics at atomistic scale using transmission electron microscope," *IEEE Trans. Electron Devices*, early access, Nov. 21, 2022, doi: 10.1109/TED.2022.3220729.
[A4] Z. Jiang et al., "Lanthanum oxyhalide monolayers: An exceptional dielectric companion to 2-D semiconductors," *IEEE Trans. Electron Devices*, early access, Jan. 24, 2023, doi: 10.1109/TED.2023.3236903.
[A5] S. Sharma, S. Das, R. Khosla, H. Shrimali, and S. K. Sharma, "Two-dimensional van der Waals hafnium disulfide and zirconium oxide-based micro-interdigitated electrodes transistors," *IEEE Trans. Electron Devices*, early access, Oct. 18, 2022, doi: 10.1109/TED.2022.3202510.
[A6] C. Y. Kee, Y. S. Ang, E.-P. Li, and L. K. Ang, "Analytical scaling of trap-limited current in 2-D ultrathin dielectrics," *IEEE Trans. Electron Devices*, early access, Nov. 24, 2023, doi: 10.1109/TED.2022.3222279.
[A7] J. B. Roldan et al., "Modeling the variability of Au/Ti/h-BN/Au memristive devices," *IEEE Trans. Electron Devices*, early access, Aug. 30, 2022, doi: 10.1109/TED.2022.3197677.
[A8] H.-H. Tai, J.-C. Wang, W.-H. Chang, F.-Z. Chen, and C.-S. Lai, "Ultraviolet photoresponse enhancement of graphene/Al_xO_y-NPs/MoS_2 heterostructure photodetectors," *IEEE Trans. Electron Devices*, early access, Jan. 24, 2023, doi: 10.1109/TED.2023.3236905.

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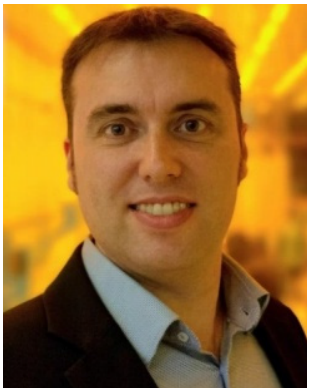
[2] C. Backes et al., "Production and processing of graphene and related materials," *2D Mater.*, vol. 7, no. 2, 2020, Art. no. 022001.
[3] *The International Roadmap for Devices and Systems*. Accessed: Mar. 3, 2022. [Online]. Available: https://irds.ieee.org/editions
[4] K. Zhu et al., "The development of integrated circuits based on two-dimensional materials," *Nature Electron.*, vol. 4, no. 11, pp. 775–785, Nov. 2021.
[5] *Website of Graphenea*. Accessed: Jun. 23, 2022. [Online]. Available: https://www.graphenea.com/
[6] C.-C. Cheng et al., "First demonstration of 40-nm channel length top-gate WS_2 pFET using channel area-selective CVD growth directly on SiO_X/Si substrate," in *Symposium on Very Large Scale Integration Technology*, 2019, pp. T244–T245.
[7] Q. Smets et al., "Ultra-scaled MOCVD MoS_2 MOSFETs with 42 nm contact pitch and 250 μA/μm drain current," in *IEDM Tech. Dig.*, 2019, pp. 23.2.1–23.2.4, doi: 10.1109/IEDM19573.2019.8993650.



Mario Lanza received the Ph.D. degree (Hons.) in electronic engineering from Universitat Autònoma de Barcelona, Barcelona, Spain, in 2010.

From 2010 to 2011, he was a National Science Foundation (NSFC) Postdoctoral Researcher with Peking University, Beijing, China, and from 2012 to 2013, he was a Marie Curie Postdoctoral Researcher with Stanford University, Stanford, CA, USA. In October 2013, he joined Soochow University, Suzhou, China, as an Associate Professor, and in March 2017, he was promoted to Full Professor. Since October 2020, he has been an Associate Professor of materials science and engineering with the King Abdullah University of Science and Technology (KAUST), Thuwal, Saudi Arabia. He has published more than 185 research papers, including Nature, Science and Nature Electronics (among others), and has registered four patents (one of them granted with U.S. $1 million).

Prof. Lanza is the Editor-in-Chief of the journal *Microelectronic Engineering* (Elsevier) and a Distinguished Lecturer of the Electron Devices Society (EDS), and has served in the board of many journals and conferences, including the International Electron Devices Meeting (IEDM) and the International Reliability Physics Symposium (IRPS). He leads a research group formed by 10–15 Ph.D. students and postdoctoral researchers, who investigate how to improve electronic devices and circuits using 2-D materials, with a special emphasis on resistive switching applications.

Kin-Leong Pey (Senior Member, IEEE) received the Bachelor of Engineering and Ph.D. degrees in electrical engineering from the National University of Singapore, Singapore, in 1989 and 1994, respectively.

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Dr. Kin-Leong is a fellow of the ASEAN Academy of Engineering and Technology and the Institute of Engineer, Singapore. He was the General Chair of IPFA2001, Singapore, and the Co-General Chair of IPFA2004, Taiwan. He was the Guest Editor of IEEE Transactions on Devices in and Materials Reliability from 2003 to 2005 and 2007, and the Chair of the Singapore IEEE REL/CPMT/ED Chapter from 2004 to 2005, 2009, and 2020. He has been an Editor of IEEE Transactions on Devices and Materials Reliability for more than ten years. He was recognized by the IEEE International Integrated Reliability Workshop (IIRW) as one of the top 20 experts of the Front-End device reliability (http://www.iirw.org/ref/reliabilityexperts.html) in 2018 and as a panelist of the Reliability Expert Forum (REF) of "Memory Technologies and Reliability" in 2019. With his pioneering effort, the SUTD undergraduate program was ranked in 2018 as the "Top Emerging Leader in Engineering Education" in the MIT benchmarking study on the global state of the art in engineering education (http://news.mit.edu/2018/reimagi-and-rethinkingengineering-education-0327).

Tibor Grasser (Fellow, IEEE) is the Head of the Institute for Microelectronics, TU Wien, Vienna, Austria. He has edited various books, e.g., on the bias temperature instability, hot carrier degradation, and noise in nanoscale devices (all Springer). He is a distinguished Lecturer of the IEEE EDS, and has been involved in outstanding conferences such as International Electron Devices Meeting (IEDM) (General Chair 2021), International Reliability Physics Symposium (IRPS), Simulation of Semiconductor Processes and Devices Conference (SISPAD), European Solid-State Device Research Conference (ESSDERC), and International Integrated Reliability Workshop (IIRW). He was a recipient of the Best and Outstanding Paper Awards from IRPS (2008, 2010, 2012, and 2014), International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2013 and 2014), European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF 2008), and the IEEE EDS Paul Rappaport Award (2011). He currently serves as an Associate Editor for IEEE Transactions on Electron Devices following his assignment for *Microelectronics Reliability* (Elsevier).