Highly Scaled GaN Complementary Technology on a Silicon Substrate

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***Abstract*— This article reports on the scaling of GaN complementary technology (CT) on a silicon substrate to push its performance limits for circuit-level applications. The highly scaled self-aligned (SA) p-channel FinFET (a fin width of 20 nm) achieved an $I_{D,\max}$ of −300 mA/mm and an R_{ON} of 27 Ω·mm, a record for metal organic chemical vapor deposition (MOCVD)-grown III-nitride p-FETs. A systematic study on impact of fin width scaling and recess depth in these transistors was conducted. A new SA scaled n-channel p-GaN-gate FET (n-FET) process, compatible with the p-FinFET, demonstrated enhancement-mode (E-mode) n-FETs (L_G = 200 nm, $I_{D,\max}$ = 525 mA/mm, and R_{ON} = 2.9 Ω·mm) on the same epitaxial platform. The p-FETs and n-FETs feature competitive performance in their respective categories and, when taken together, offer a leading solution for GaN CT on a silicon substrate.**

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I. Introduction

THE rising performance of GaN power ICs has offered compactness and record levels of efficiency and power for data centers, power adapters, electric vehicles (EVs), and 5G/6G telecommunication systems [1], [2], [3]. However, the lack of a GaN p-channel field effect transistor (p-FET) significantly increases static power dissipation (resulting from the use of n-type only enhancement-mode (E-mode)/depletion-mode logic) and prevents all-GaN integration (e.g., control loops and analog mixed-signal blocks) [4]. Furthermore, the availability of high-side switching GaN p-FETs would improve the switching speed (avoiding the issue of limited common-mode transient immunity (CMTI) in the level shifter), therefore enabling more efficient and higher density power converters [5]. Therefore, the availability of a high-performance GaN complementary technology (CT) would significantly improve the performance of GaN-based electronics.

Several recent works have studied the feasibility of a GaN CT, realized using the following: 1) epitaxy regrowth to optimize n- and p-channels separately, by Chu et al. [6], offering great flexibility in epitaxy and transistor design and 2) coexistence of n- and p-channels on p-GaN/GaN/AlGaN/GaN (or slight variations), by Hahn et al. [7], Nakajima et al. [8], [9], Chowdhury et al. [10], Zheng et al. [11], and Chen et al. [12], offering ease of integration. While each approach has its own merits, the next chapter of GaN CT research should adopt an application-driven perspective, where stringent requirements should be placed on: 1) easy integration of p-FETs and n-FETs on the same platform, ideally, without the need of regrowth steps that increase cost; 2) scalable platform to accelerate commercialization; 3) ability to withstand the large heat generation in EVs, data centers, and base stations; and 4) most importantly, concurrently high performance of both p-FET and n-FET. Thus far, discrete GaN p-FETs have received significant attention [13], [14], [15], [16], [17], [18], [19], [20], [21], but equal attention should be paid to their monolithic integration with n-FETs.

In view of the above application requirements and among the various options, the GaN CT platform in [10] based on p-GaN/AlGaN/GaN heterostructures stands out as a promising

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candidate. To this end, this work advances GaN CT based on the above-mentioned GaN-on-Si platform, by exploring the advanced scaling of GaN CT with self-aligned (SA) gate etch. It is noted that, aggressive scaling has been adopted in a wide range of novel transistors to improve their performance [22], [23] and will be a key strategy pursued in this work. The starting material is a III-N heterostructure grown by metal organic chemical vapor deposition (MOCVD) on 150-mm (6-in) Si wafers [Fig. 1(a)]. The epitaxial structure ["Epi-1," Fig. 1(a)] is modified from earlier work [10] by inserting a 1.5-nm AlN (in actual implementation, high Al composition AlGaN) layer. The use of an AlN layer allows for polarization enhancement of the p-channel charge density [20] and a better etch stop during the selective etch of p-GaN/UID-GaN over AlGaN (a key process step for the n-FET). Both p-FETs and n-FETs were fabricated on this structure [Fig. 1(b)–(d)]. In addition, a conventional p-GaN/AlGaN/GaN epitaxial structure ("Epi-2"), which has been used in the past for p-FETs [12], was investigated for SA p-GaN-gate n-FETs. The same epitaxial structure of Fig. 1(a) was processed to realize the p-FET and n-FET [Fig. 1(b)–(d)]. In this article, unless otherwise stated, the p-FET and the n-FET refer to GaN-based transistors.

The organization of this article is as follows. The concept of the p-FET, the device fabrication, and characterization are presented in Section II, followed by the same aspects of the n-FET in Section III. Section IV presents a benchmarking of the proposed GaN CT and an overview of the areas of future research, followed by Section V, which concludes this article.

II. GaN p-FET: Design and Characterization

Channel length scaling of p-FETs is critical to overcome the low hole mobility in these transistors (experimentally measured to be typically <30 cm^2/V·s) and to take advantage of field-induced acceptor ionization [24], [25]. To this end, an SA FinFET architecture [17] was adopted in this work, as it offers new opportunities for p-FET design. The impact of fin width scaling and recess depth on these transistors was studied. Further improvement in transistor performance was also contributed by optimizations to the key process steps of the proposed p-FET, which will be described in Section II-A.

A. SA GaN p-FinFET Process Flow

The process flow of the p-FET is an optimized version of the baseline flow as reported in [17], with the key improvements highlighted below. First, the ohmic contacts to p-GaN are formed using Ni/Au/Ni (30/50/30) and liftoff, and then annealing at 550 °C in $N_2 : O_2$ environment in 1 : 1 ratio for 45 min. Next, the fins are fabricated by electron-beam lithography using hydrogen silsesquioxane (HSQ) resist, followed by reactive ion etching (RIE) based on Cl_2/BCl_3 plasma. The length of the HSQ resist mask (and, consequently, the fins) extends through the entire source–drain spacing L_{SD}. The fins were aligned to the *m*-plane, in order to ensure smooth sidewalls as discussed later [26]. The HSQ thickness (70 nm) was optimized to achieve a balance between sufficient etch resistivity (as a mask) and the aspect ratio required for scaled fins. After the etch, HSQ is removed using hydrofluoric acid (HF). A similar Cl_2/BCl_3 plasma process is applied to perform the recess of the SA gate region, which is defined by the ohmic contacts. A medium-power Cl_2/BCl_3-RIE (etch rate of ≈1 nm/min) was used for these steps as a compromise among damage to ohmic contact, fin etch-induced damage, and good etch geometric profile. The optimized process was capable of achieving the fin widths of 20 nm at an L_{SD} of <200 nm. The SA architecture ensures that the access region (and therefore access resistance) is negligible, and that the entire length of the fin ($=L_{SD}$) is gated. The details of the p-FET process flow are reported in [27].

When compared with a planar channel, the fin channel has more surface area exposed to RIE plasma. Therefore, several steps were conducted to heal etch damage, namely, the following: 1) hot (75 °C) tetramethylammonium hydroxide (TMAH) treatment for 5 min, which was reduced from 15 min in [17] to prevent complete etching of the highly scaled fins and 2) N_2 treatment [28] in a furnace at 500 °C for 30 min. This treatment resulted in a 15% improvement in channel resistance (hence, current level). The gate-stack was formed by the atomic layer deposition (ALD) of SiO_2 (15 nm) using tris(dimethylamino)silane (TDMAS) and O_2 plasma at 250 °C, and RF magnetron sputtering of Ti/Au (30/50 nm). The gate dielectric quality and p-GaN/dielectric interface make a significant contribution to the device switching characteristics, therefore making this an area of active research [29], [30]. An optimized SA p-FinFET is presented in Fig. 1(c).

B. Results and Discussion

The performance of the p-FET with the best overall characteristics (L_{SD} = 175 nm, L_G SA, a fin width of 20 nm) is presented in Fig. 2. An $I_{D,\max}$ of −300 mA/mm, an R_{ON} of 27 Ω·mm, and current saturation at high gate overdrive were achieved, as shown in Fig. 2(a). The transfer characteristics [Fig. 2(b)] reveal a V_{th} of 3 V and a peak transconductance, g_m, of 13 mS/mm. The current ON–OFF ratio is 200, limited by the leakage current through the gate dielectric.

The impact of two key device design parameters (fin width and gate recess depth) on DC output characteristics ($I_{D,\max}$ and R_{ON}) was systematically studied for GaN p-FinFETs. As the fin width is reduced below 50 nm, the current density and R_{ON} improve [Fig. 2(c)]. However, this trend was not observed above 50 nm, possibly due to the significant reduction in the field-induced acceptor ionization effect [25]. In addition, a deeper gate recess was found to reduce current density [Fig. 2(d)], primarily due to reduction of carrier density in the p-channel, but is expected to significantly improve ON–OFF ratio and subthreshold swing, as is the case for p-FETs based on similar epitaxial structures. Unfortunately, the gate oxide quality in this batch of fabricated transistors was found to be the limiting factor for the current ON–OFF ratio (<10^4). It follows that, the OFF-state characteristics were limited by gate control and drain-induced barrier lowering (DIBL), before a destructive breakdown at ≈20 V.

An interesting observation is the presence of "two turn-ons" at large gate overdrive and highly negative V_{DS}, which is evident from the transfer characteristics [g_m *vs.* V_{GS}, Fig. 2(b)]. In order to study the "double turn-on" phenomenon from a

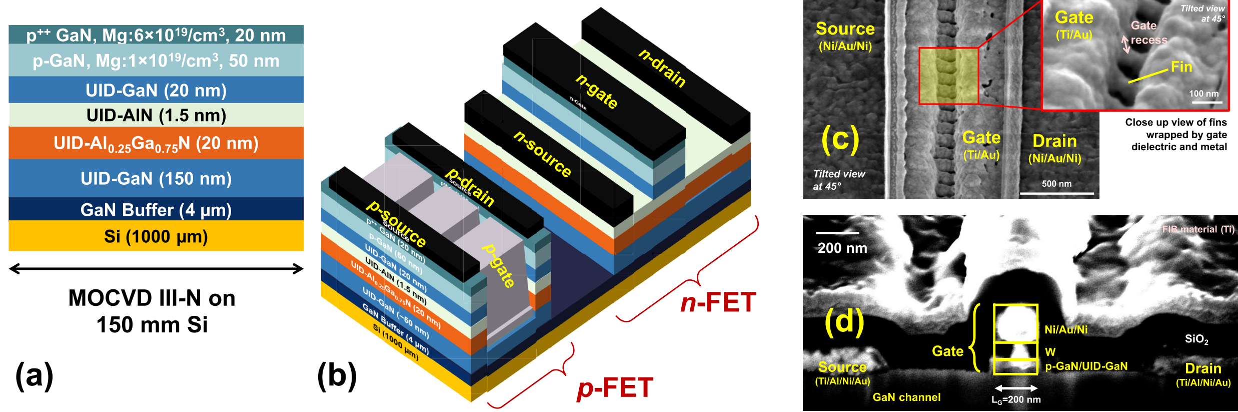

Fig. 1. Highly scaled GaN CT. (a) Epitaxial structure. (b) Device structures of p-FET (SA FinFET) and n-FET (SA-gate p-GaN-gate HEMT) based on the same GaN-on-Si platform, as illustrated in (a). (c) and (d) SEM images of representative p-FET and n-FET, respectively.

device mechanism aspect, technology computer-aided design (TCAD) simulation of a 2-D TCAD structure [considering a planar structure in the middle of the fin of the p-FET, Fig. 3(a)] was conducted using Silvaco ATLAS. Three gate recess (GR) depths were chosen (labeled as GR-{1,2,3}), with GR-1 being the deepest gate recess (least thickness of p-GaN remaining). For the three devices with different gate recess depths, a qualitative difference in g_m profiles was observed, as presented in Fig. 3(b). For a visualization of the electrical characteristics, the device cross sections showing the local hole concentrations are included in Fig. 3(c). In the case of GR-1, which is commonly featured in early demonstrations of GaN-on-Si p-FETs [31], a single g_m peak (bias point 1) was observed, which corresponds to the accumulation of the p-channel near the p-GaN/AlGaN interface. Next, the case of GR-3, which corresponds to shallow gate recess (more p-GaN remaining), is examined. A "g_m double peak" is observed. The first sub-channel (near the p-GaN/AlGaN interface) is activated at bias point 2, and its full accumulation is completed by bias point 3. Then, the activation of the second sub-channel (bulk p-channel underneath the gate metal) occurs at bias point 4. Finally, the case of GR-2 (gate recess depth in between GR-1 and GR-3) is examined. Similar to the case of GR-3, at bias point 5, the first sub-channel is activated. Then, at bias point 6, the theoretical peak contributed by the second sub-channel is less obvious. Therefore, this accumulation effect shows up as a kink in the g_m curve instead of a discrete peak. The phenomenon of GR-2 may be understood from two perspectives: 1) due to the limited amount of p-GaN remaining, the two sub-channels are not so distinct but are effectively fused into a single channel and 2) the theoretical g_m peaks contributed by the two sub-channels are two close to each other (in terms of V_{GS}). In all of the devices, at high gate overdrive, all of the channels have been turned on. This proof-of-concept simulation illustrates the impact of the sub-channels (whose existence is dependent on the recess depth) on the transfer characteristics of the p-FET.

The experiment and simulation confirm the significance of the gate recess depth (as a key design parameter) in transistor performance, in terms of $I_{D,\max}$, R_{ON}, and transfer characteristics. This phenomenon is unique to the p-FET (as

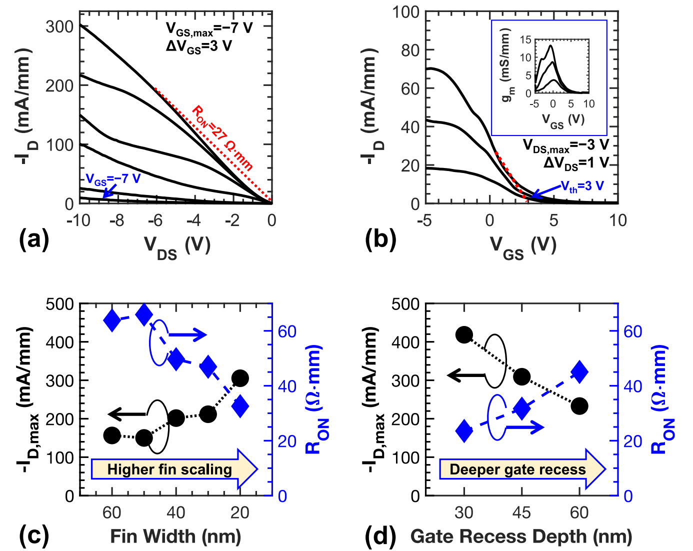

Fig. 2. Performance of p-FET and the scaling trends. (a) Output characteristics of p-FET with L_{SD} = 175 nm (L_G SA) and fin width = 20 nm. (b) Transfer characteristics of the abovementioned p-FET. The g_m profile is presented in the inset. Study of the impact of (c) fin width and (d) gate recess depth on the performance ($-I_{D,\max}$ and R_{ON}) of GaN p-FinFETs. $-I_{D,\max}$ and R_{ON} were measured at $V_{GS} = -7$ V.

opposed to HEMTs) due to the design of the epitaxial structure (p-GaN/AlGaN/GaN) and transistor structure (gate recessed MISFET). The formation of the p-channel at and surrounding the p-GaN/AlGaN interface is made possible by a highly p-doped material (p-GaN). The p-channel in the epitaxial structure is buried, and therefore, a simple top gate is not sufficient to exert electrostatic control over the entire channel. A recessed gate structure, while adding design flexibility to p-FETs, requires special consideration in the design (recess depth and geometric profile) and fabrication (e.g. reducing etch-induced damage [25], [28]).

III. GaN n-FET: Design and Characterization

This work also seeks to improve the performance of GaN n-FETs based on the GaN CT platform through the development of a gate technology where the gate metal is SA to the p-GaN region. The realization of E-mode n-FETs is highly desired for a wide variety of applications, including

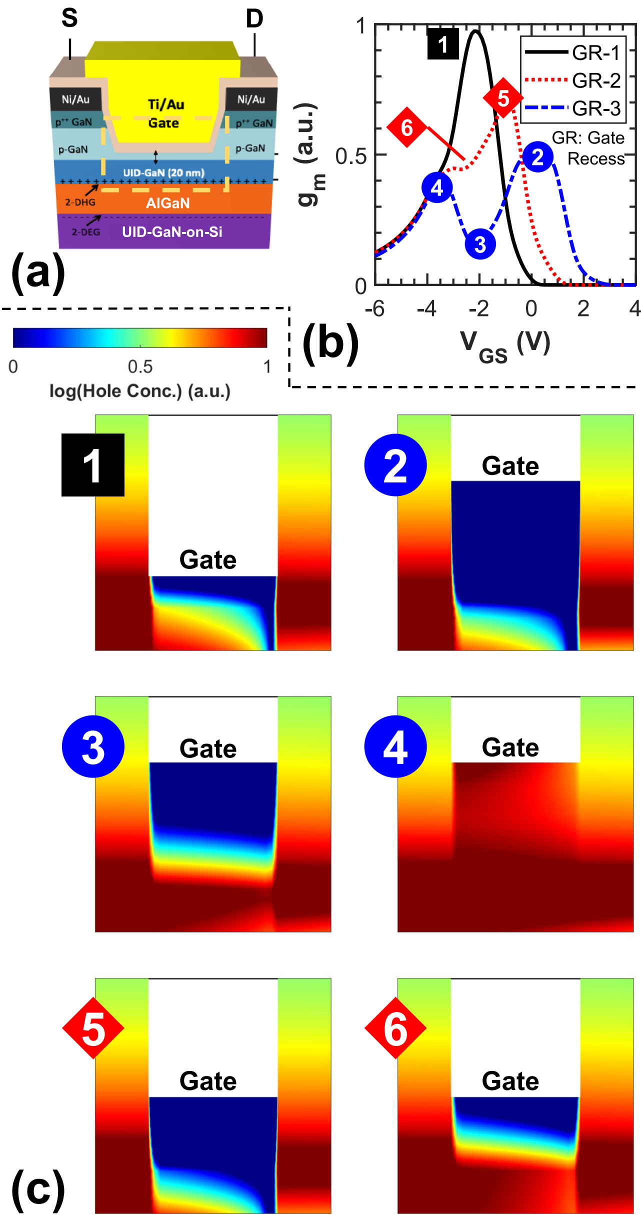

Fig. 3. Proof-of-concept simulation study of the "g_m double peak" phenomenon. (a) Representative 2-D device structure used in the simulation. This is a planar structure in the middle of the fin. (b) g_m profiles of various gate recess (GR) values, with GR-1 being the deepest gate recess (least thickness of p-GaN remaining). (c) Cross sections of the device of different gate recess depths and at various bias points. The number labels in the g_m profiles indicate different bias conditions and correspond to the device cross sections, which illustrate the local hole concentration.

power electronics, as well as digital and RF integrated circuits (ICs), where the bias circuitry could be simplified by eliminating the need of a third bias terminal (V_{SS}) [32], [33]. Approaches to the realization of GaN E-mode n-FETs include F-plasma treatment of the gate region [34], metal-insulator-semiconductor (MIS)-recessed gate [35], FinFET/tri-gate [36], and p-GaN-gate [10]. In this work, the p-GaN-gate n-FET is chosen because of the following considerations: 1) easy integration with p-FET [Fig. 1(b)] and other power IC components [4]; 2) minimum degradation of as-grown gate surface (i.e., no photoresist or etching), which reduces hysteresis and trapping issues; and 3) demonstrated performance and robustness in GaN circuits at high temperature (up to 500 °C) [37], [38].

While numerous p-GaN-gate HEMTs have been reported in the literature, the introduction of self-alignment between the metal electrode and the p-GaN would be beneficial to do the following: 1) achieving a shorter p-GaN gate length, because the alignment tolerances needed for the metallization would not be applicable and 2) reduction of gate capacitance, which is key for high-speed low/medium-voltage power ICs and analog mixed-signal applications. SA p-GaN-gate technologies were previously explored [39], [40]. This work proposes a simple gate-first process flow, which incorporates the following: 1) novel metallization scheme with lower sheet resistance; 2) GaN/AlGaN selective etch recipe; and 3) etch hard mask to ensure aggressive scaling of the gate length.

A. SA p-GaN-Gate HEMT Process Flow

The SA gate process begins with the blank sputtering deposition of W (100 nm). Then, Ni/Au/Ni (30/120/80 nm) was patterned by electron beam lithography and liftoff. W was etched using the top Ni as a hard mask. Selective etching of p-GaN over AlGaN was achieved using SF_6/BCl_3 plasma, which has been reported to give high etch selectivity [41]. W was chosen because of its high thermal stability (necessary for a gate-first process) and Schottky behavior with p-GaN gates [28]. Finally, ohmic contacts were formed by Ti/Al/Ni/Au alloyed at 800 °C in N_2 ambient. The typical contact resistance is ≈0.75 Ω·mm. A fabricated scaled SA p-GaN-gated n-FET is presented in Fig. 1(d). A proof-of-concept layout was adopted, where the fabricated n-FETs are symmetric (gate is located in the center of the ohmic contacts, or $L_{GS} = L_{GD}$), and that electric field management structures (e.g., edge termination) were not included.

Significant optimization was required to realize the proposed SA p-GaN-gate process, as illustrated in Fig. 4(a). The use of a Ni/Au/Ni metal stack allows for the following; 1) the top Ni to serve as the hard mask for gate definition and 2) the reduction of gate sheet resistance from 10 Ω/□ (W only) to <0.5 Ω/□ (this work). It was found to be difficult to deposit the entire W/Ni/Au/Ni stack using a single evaporation and liftoff step. Therefore, two metal deposition steps were required. Two aspects are critical for the gate module, namely: 1) a highly selective GaN/AlGaN etch with good surface morphology after etch and 2) highly robust etch mask using gate metal for the etch in (1). Fig. 4(b) presents short-loop tests of GaN/AlGaN selective etch, which indicate >10 : 1 selectivity and a root mean square (rms) roughness of 6 nm. Next, the top metal mask was integrated with this selective etch recipe. Careful optimization was required to the etch conditions and mask. A poor etch would result in significant redeposition of particles around the gate structure [Fig. 4(c)]. Furthermore, considering the degradation of the gate structure [Fig. 4(d)], such a transistor would require greater access region lengths (L_{GS} and L_{GD}) than what is required for lithography alignment tolerance of the ohmic contacts (as is the case of a standard HEMT). An optimized

TABLE I
BENCHMARKING OF GaN CT DEMONSTRATIONS BASED ON $|I_{D,\max}|$ AND R_{ON}

Affiliation	Year	Epitaxial Structure	Substrate	$\|I_{D,max}\|$ [mA/mm] (n/p-FET)	R_{ON} [Ω·mm] (p/n-FET)	V_{th} [V] (n/p-FET)
RWTH Aachen [7]	2014	p-GaN/GaN/AlInGaN/GaN	Sapphire	$10/0.2 = 500$	–	$0.5/-0.5$
				$800/15 = 53$	–	$-11/2$
AIST [8], [9]	2015	p-GaN/GaN/AlGaN/GaN	Sapphire	$16/1.8 = 8.8$	$30000/660 = 45$	$-2/4$
	2018	p-GaN/GaN/AlGaN/GaN	Sapphire	$0.14/0.01 = 14$	$20000/6000 = 3.3$	$4/-2.7$
HRL [6]	2016	(1) AlGaN/GaN (2) p-GaN/GaN/AlGaN (regrowth)	Sapphire	$230/1.65 = 140$	$1314/10 = 131$	$0/0$
MIT [10]	2020	p-GaN/GaN/AlGaN/GaN	Si	$310/1.2 = 258$	$2300/6 = 383$	$0.2/-1$
HKUST [11]	2021	p-GaN/AlGaN/GaN	Si	$170/1.65 = 103$	$4500/12.7 = 354$	$2.5/-2$
Xidian U. [12]	2022	p-GaN/AlGaN/GaN	Si	$275/0.45 = 611$	$8900/9.1 = 978$	$2.3/-2$
This Work	**2022**	**p-GaN/GaN/AlN/AlGaN/GaN**	**Si**	$\mathbf{525/300 = 1.75}$	$\mathbf{27/2.9 = 9.3}$	$\mathbf{1.6/3}$

Values, if not reported directly in the respective papers, are based on best estimates from the published data. Epitaxial layers are unintentionally doped (UID) unless otherwise stated.

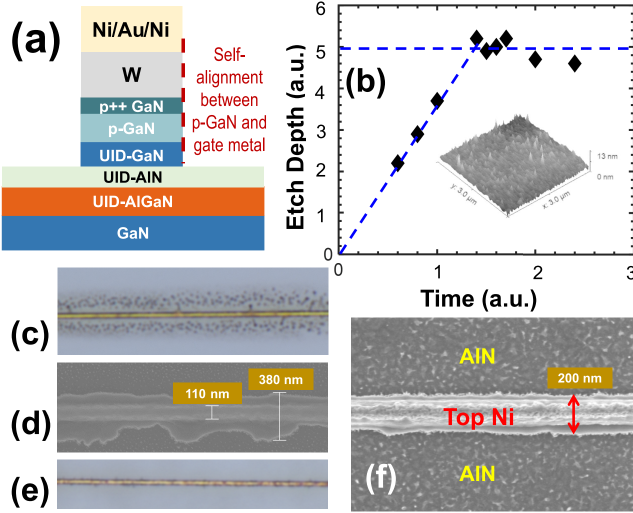

Fig. 4. Details of fabrication optimization of n-FET (p-GaN-gated AlGaN/GaN HEMT), with particular attention on the novel SA p-GaN-gate. (a) Device structure after the formation of the SA p-GaN-gate. (b) Selective etch of p-GaN over AlGaN using a BCl_3/SF_6 process. An "etch stop" is achieved with >10 : 1 selectivity. The inset illustrates the morphology of the etched surface showing an rms roughness of 6 nm. (c) Optical image of a gate region (but with thin top Ni mask), showing that significant amounts of metal were sputtered off the gates. (d) SEM image of a gate with a nonideal etch. (e) and (f) Optical and SEM images of a gate region with optimized etch, respectively. The region around the gate metal was clean. The complete process flow is presented in [27].

gate structure is presented in Fig. 4(e) and (f). An 80-nm-thick layer of Ni was required in order to ensure sufficient etch resistivity against both F-based and Cl-based plasmas. The details of the n-FET process flow are reported in [27].

B. Results and Discussion

Scaled n-FETs with $L_G = 200$ nm and $L_{SD} = 1.1$ μm show good current saturation with $I_{D,\max} = 525$ mA/mm and $R_{ON} = 2.9$ Ω·mm [Fig. 5(a)]. E-mode operation with $V_{th} \approx 1.6$ V was achieved [Fig. 5(b)]. A peak g_m of 265 mS/mm reflects good gate control using the proposed gate metallization stack. As expected, gate length scaling improves $I_{D,\max}$ for the ON-state characteristics, but slightly worsens the gate control in the OFF-state breakdown measurements. The destructive breakdown was ≈50 V. It should be noted that, none of the transistors in this work feature any electric field management structures (e.g., field plates and charge balancing [42]), which are expected to push the boundary of the $R_{ON}A \times$ BV trade-off.

The maximum achievable I_D in the W/p-GaN-gate HEMTs is typically limited by the following: 1) the allowable gate overdrive before the onset of significant gate leakage and 2) carrier velocity in scaled transistors. Through analysis of temperature-dependent current–voltage characteristics from room temperature to 500 °C, it was found that the gate current in the reverse bias and onset of forward bias is dominated by 2-D variable range hopping (2-D VRH), while the gate current in the strong forward bias regime is dominated by the leakage through the vertical junction current. The details of the study will be reported elsewhere.

While the scaled SA p-GaN-gate n-FET technology was originally developed for integration with p-FETs on the GaN CMOS platform, it could also be useful in its own in low-voltage GaN power ICs or GaN n-FET-only circuits. To evaluate the robustness of this technology for such a possibility, the process flow was applied on a conventional p-GaN-gate epitaxial structure made of p-GaN (70 nm)/AlGaN (15 nm)/GaN ("Epi-2") [31]. In the n-FETs based on Epi-2, better performance ($I_{D,\max} = 750$ mA/mm and $R_{ON} = 1.3$ Ω·mm), higher current ON–OFF ratio [Fig. 5(c)], sharper ON–OFF transition (SS values of n-FETs based on Epi-1 and Epi-2 are 123 and 100 mV/dec, respectively), and negligible hysteresis (<0.1 V) [Fig. 5(d)] were observed. The above improvements with respect to the n-FET in the CT platform are attributed to the location of the gate metal closer (by ≈25 nm) to the n-channel at the AlGaN/GaN interface and better gate electrostatic control by the metal gate to the n-channel (the absence of UID-GaN and AlN, and thinner AlGaN layer).

IV. BENCHMARKING

Fig. 6(a) summarizes the performance of GaN p-FETs in terms of two key device-level parameters, $-I_{D,\max}$ and I_{ON}/I_{OFF}. To the best of the authors' knowledge, the best p-FET in this work features the highest current density among MOCVD III-N p-FET (>2× the previous record, −140 mA/mm [17]), as well as competitive performance compared with GaN/AlN molecular beam epitaxy (MBE) counterparts [13].

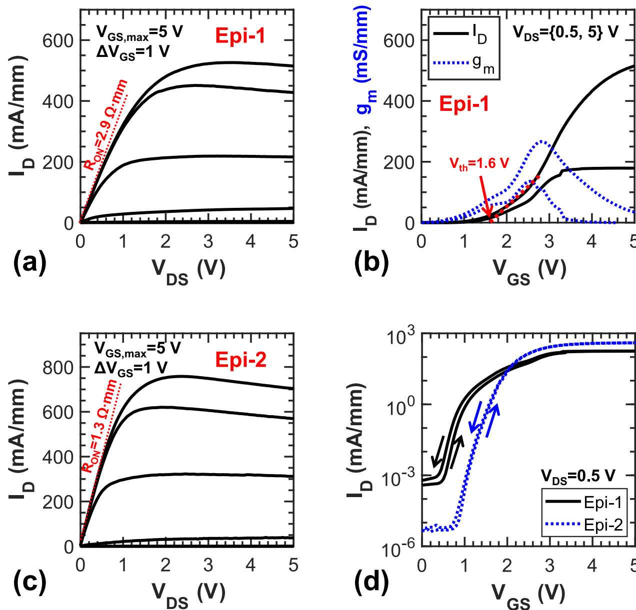

Fig. 5. Performance of n-FET with L_G = 200 nm and L_{SD} = 1.1 μm. (a) Output characteristics of n-FET based on Epi-1. (b) Transfer characteristics of n-FET based on Epi-1. (c) Output characteristics of n-FET based on Epi-2. (d) Comparison of transfer characteristics of the n-FETs fabricated using the same proposed process flow on Epi-1 and Epi-2. The definitions of these epitaxial structures are provided in Section I.

As presented in Fig. 6(b), the maximum current density of p-FETs was plotted against gate length to study the impact of (aggressive) channel length scaling, which is one of the main objectives of this work. The p-FET of this work achieved $-I_{D,\max} \times L_G = 52.5\ \mu$A, which is a record for MOCVD-based (single GaN/AlGaN epitaxial layer) p-FETs, and is close to the values for the record MBE-based p-FETs and MOCVD superlattice (multiple GaN/AlGaN epitaxial layers) p-FETs. Two observations may be made. First, the p-FETs with the highest current densities feature ultrascaled gate lengths <200 nm. This observation is in agreement with the previous p-FET reports on gate length scaling of a single type of p-FET [28]. Second, to achieve substantial improvement from the state-of-the-art $-I_{D,\max} \times L_G$ values, new epitaxial structures and better quality growth of the p-channel would be highly desired. In addition to the benchmarking of Fig. 6(a) and (b), it is worthy to note that, the proposed p-FET technology is compatible with n-FETs fabricated on the same GaN-on-Si platform, as indicated by the solid symbols in these figures.

A benchmarking of GaN CT based on the same platform is presented in Fig. 6(c) and (d). All of the reports of n-FETs and p-FETs based on the same platform (i.e., reported in a single publication) are based on MOCVD-grown epitaxial structures [6], [7], [8], [9], [10], [11], [12]. The results of the benchmarking are graphically presented in Fig. 6(c) and (d), while more detailed information is presented in Table I. Two parameters, namely, $|I_{D,\max}|$ [ratio of n-FET/p-FET, Fig. 6(c)] and R_{ON} [ratio of p-FET/n-FET, Fig 6(d)], are highlighted because of their significance in power and digital IC design. A ratio approaching unity (=1) is desired to achieve reasonable transistor sizing. The current density of the reported GaN CT is comparable with that of 5-V-rated Si CMOS in an industry

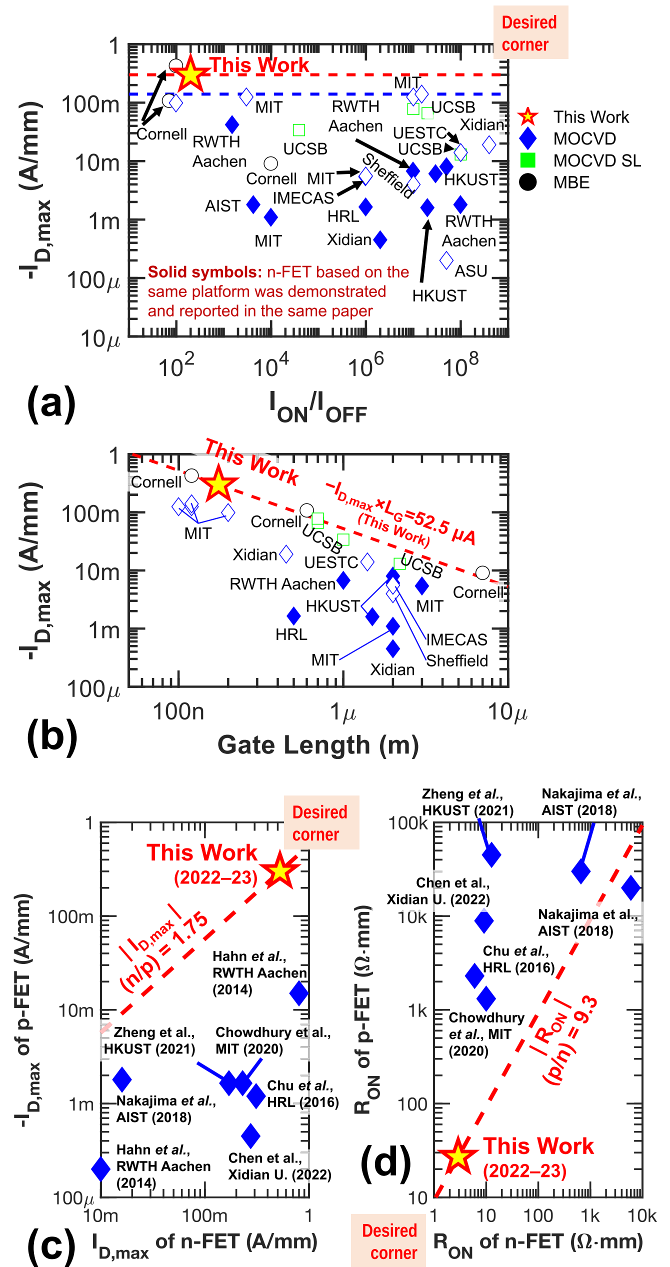

Fig. 6. Benchmarking of this work with other published works. (a) GaN p-FETs in terms of ON-current and ON–OFF ratio. (b) GaN p-FETs taking into account the trade-off between current density and gate length. (c) and (d) GaN CTs (complementary transistors reported in the same article) in terms of current densities and R_{ON}, respectively. Solid symbols indicate that complementary transistors (p-FET and n-FET) based on the same platform were demonstrated and reported in the same article.

0.13-μm bipolar-CMOS-DMOS (BCD) process published in 2016 ($I_{D,\max\{n,p\}}$ = {520, −323} mA/mm) [43].

Fig. 6(c) and (d) and Table I reveal that significant advancement in the performance of GaN CT has been achieved over the years. This work continues to push the performance of GaN CT, as compared with other reports and the authors' earlier demonstration [10], because of innovation in device architecture (self-alignment), aggressive scaling, and optimization of processing technology. These results were achieved despite relatively high channel resistances

($R_{sh\{p,n\}} \approx \{60\,000, 800\}\ \Omega/\square$), which could be improved with optimization of epitaxial design.

It is noted that, a disparity between the ratios of $|I_{D,\max}|$ and R_{ON} exists. This phenomenon is attributed to several reasons, mainly related to the characteristics of the p-FET: 1) Schottky turn-on behavior of the p-FET and 2) significant field-induced acceptor ionization at high gate overdrives and highly negative drain biases, in particular for the FinFET structure, as explained in Section II-B. Finally, it should be acknowledged that, significant research remains to be done in the co-optimization of this emerging GaN CT in the following: 1) further advancement of various process modules, e.g., ohmic contacts with low contact resistance [44], [45], [46] and low damage gate recess [25], [28]); 2) device and process engineering to achieve a good balance of performance specifications (DC and switching characteristics); and 3) epitaxial structure, to achieve lower channel resistances while ensuring carrier confinement.

V. Conclusion

Advanced scaling based on SA features, as proposed in this work, offers a viable technology path for future high-performance GaN CT based on a MOCVD GaN-on-Si platform. The scaled p-FETs and n-FETs achieve competitive performance in their respective categories and, when taken together, deliver a leading GaN CT solution. Further design innovation and engineering of the proposed technology would greatly benefit the eventual wafer-level heterogeneous integration of GaN CT (based on a Si substrate) with Si CMOS to achieve multifunctional chips [47].

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