Memristor-Based Cryogenic Programmable DC Sources for Scalable In Situ Quantum-Dot Control

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***Abstract*— Current quantum systems based on spin qubits are controlled by classical electronics located outside the cryostat. This approach creates a major wiring bottleneck, which is one of the main roadblocks toward scalable quantum computers. Thus, we propose a scalable memristor-based programmable dc source that can perform biasing of quantum dots (QDs) inside the cryostat. This novel cryogenic approach would enable to control the applied voltage on the electrostatic gates by programming the resistance of the memristors, thus storing in the latter the appropriate conditions to form the QDs. In this study, we first demonstrate multilevel resistance programming of TiO_2 memristors at 4.2 K, an essential feature to achieve voltage tunability of the memristor-based dc source. We then report hardware-based simulations of the electrical performance of the proposed dc source. A cryogenic TiO_2 memristor model fit on our experimental data at 4.2 K was used to show a 1 V voltage range and 100 μV resolution in situ memristor-based dc source. Finally, we simulate the biasing of double QDs (DQDs), enabling 120 s stability diagrams. This demonstration is a first step toward advanced cryogenic applications for resistive memories, such as cryogenic control electronics for quantum computers.**

***Index Terms*— Cryogenic electronics, memristors, quantum dots (QDs).**

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I. Introduction

SILICON quantum dots (QDs) are among the leading candidates for large scale integration of qubits given their compatibility with industrial semiconductor fabrication processes [1], which may enable mass production and easier co-integration with control electronics. Moreover, semiconductor qubits benefit from a small qubit pitch, a long coherence time, and high gate fidelity [2], [3]. However, quantum error correction and millions of physical qubits will be required to enable industrial applications, such as quantum machine learning, or drug synthesis. The current approach to realize a QD-based computer requires the qubit chip to be operated at 1 K or below [4], while its control electronics are placed outside of the dilution refrigerator [see Fig. 1(a)]. In particular, the number of QD gates that are required to properly confine the charge carriers can range from one to up to six for specific QD designs [5], and as many dedicated dc sources and cables per qubit. Although the control approach that is depicted in Fig. 1(a) has enabled important demonstrations over the past years, it will become cumbersome for few hundred qubits and unachievable for the million of physical qubits required for fault-tolerant quantum computing. To avoid this wiring bottleneck, integrated cryogenic control platforms are being

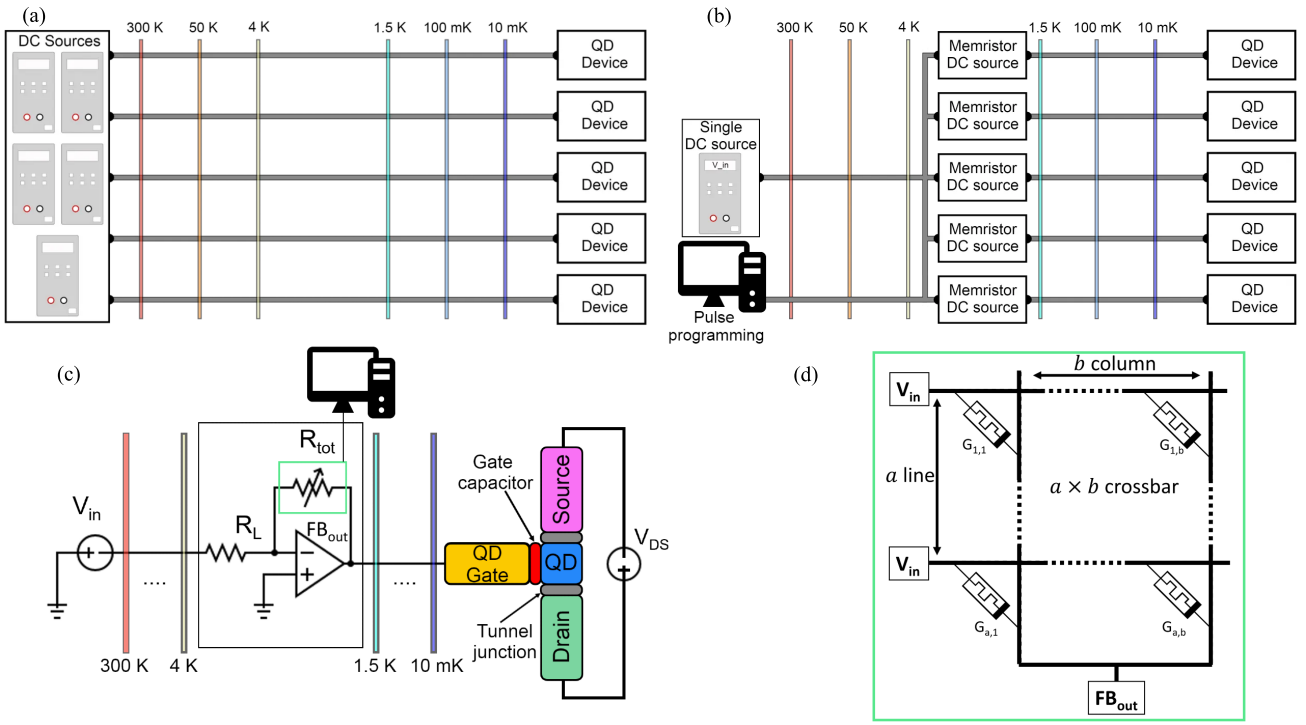

Fig. 1. **Memristor-based programmable dc source.** **(a)** Schematic view of a QD-based quantum computer that is limited to the QD biasing. The qubit chip is placed at the lower stage of a dilution refrigerator at 10 mK. The dc signals required to bias the qubits are generated by dc sources at room temperature and routed by coaxial cables leading to a wiring bottleneck. **(b)** Schematic view of a QD-based quantum computer using the proposed memristor-based dc source at 4 K and supplied by a single dc source delivering a fixed voltage V_{in}. An additional RF line is required to tune the memristors. **(c)** Zoom-in on a dc line supplying the voltage bias to a single QD gate. The green-framed variable resistor is the memristor circuit that is used as a tunable feedback resistor in a PGA circuit (framed in gray). **(d)** Circuit diagram of a memristor-based variable resistor. Memristors are fabricated in an arbitrary sized $a \times b$ crossbar array, i.e., a can be different from b yielding to non-square crossbars. By individually tuning the resistance of each memristor using dedicated logic electronics, we can vary the total resistance R_{tot} of the crossbar and thus the output voltage of the dc source. "FB out" is connected to the output of the feedback loop.

developed to control a larger number of spin qubits [5], [6], while limiting the control electronics required at room temperature [see Fig. 1(b)].

To identify and reach the correct electronic regime, it is necessary to individually tune all of the QD gate biases using dc signals, typically in the ± 1 V range with at least a 100 μV resolution, while maintaining a thermal budget in the order of a milliwatt or below per dc source [5], [7]. A first integrated solution based on switched-capacitors and charge-locking, conceptually close to dynamic random access memories (DRAMs), has been proposed to perform charge carrier confinement for several QDs [8]. This approach necessitates integrating several transistors on top of a qubit array of 100 nm pitch [9], thus requiring qubits that have similar electrical behavior to avoid this technological limitation. To maintain the desired bias voltage applied to the QD gate, the switched-capacitor charge needs to be refreshed periodically which introduces an additional power consumption in the few tens of nanowatts and might require additional DACs. Meanwhile, TiO_2-based memristors [10] exhibit non-volatility, multilevel resistance state programming [11] and CMOS-compatible fabrication processes [12]. Its resistance value depends on its internal state. This resistance state is tuned by external stimuli, such as dc sweeping or voltage pulses, which enables the voltage programmability of the dc source. Moreover, the conduction mechanisms and temperature-dependent dc behavior of memristors based on transition metal oxides have been studied at cryogenic temperatures down to 1.5 K [13], [14], hinting at hybrid CMOS-memristor control circuits for quantum systems. The co-integration of a memristor-based biasing circuit and QDs will benefit from the recently demonstrated operation of spin qubits at 1 K [4] relaxing the power dissipation restrictions. This approach would make it possible to control the applied voltage on the gates by changing the resistance of the memristors in a non-volatile manner. This ON-chip co-integration would require a single I/O to bias several QDs, thus paving the way for scalable quantum computers on silicon.

In this article, we propose a memristor-based dc source set to operate at 4 K to bias the gates of a silicon QD cooled to $\sim$10 mK. However, the perspective of spin qubits at 4.2 K in the near future would allow a co-integration enabling scalability as both technologies are CMOS-compatible [1], [12]. Using a feedback resistance tuning algorithm, we experimentally demonstrate the multilevel resistance programmability of Al_2O_3/TiO_{2-x} memristor crosspoints [12] at 4.2 K. In addition, we conduct extensive hardware-based simulations of a memristor-based programmable gain amplifier (PGA) to optimize the design of the memristor feedback resistor, and

show that this approach meets the voltage range and resolution criteria for biasing of QDs.

II. Concept

Fig. 1(a) shows a typical experimental setup for spin qubits that operate at 1 K or below with optimal operation at 10 mK. DC biases are generated by rack-sized electronics at room temperature and routed by dc lines to the qubits in the dilution refrigerator. This approach imposes a limit on the number of biasing lines that can be integrated. We propose a PGA as a biasing solution where the variable feedback resistor is based on a memristor circuit [see Fig. 1(c) and (d)]. To simplify the design and limit the wiring bottleneck, we propose to use a passive memristor crossbar instead of a 1T1R architecture used to reduce the sneak path current and increase the programming accuracy. The resistance of each memristor can be tuned individually due to the analog behavior of memristors using write pulses. In the context of the PGA, these pulses can be applied using a low-dissipation cryogenic FPGA [15]. A single dc source that provides a fixed voltage at room temperature is required to supply multiple PGA circuits placed at the 4 K-stage [see Fig. 1(b) and (c)] limiting the control electronic at room temperature and thus limiting the number of cables going in the cryostat.

Based on the circuit parameters in Fig. 1(c), we can determine the theoretical electrical characteristics of the memristor-based dc source. The output voltage is determined by the amplification factor $A_R = R_{\text{tot}}/R_{\text{L}}$, where the load resistor R_{L} is constant. With a common supply voltage V_{in} supplied to all of the horizontal lines of the memristor crossbar array, the total resistance of the crossbar is given by $R_{\text{tot}} = (\sum_{i,j} G_{ij})^{-1}$, where (i, j) represent the position of a memristor in the crossbar and G_{ij} its conductance. By programming N_s distinct resistance states for each memristor, the feedback resistor R_{tot} can take a maximum of $N_s^{N_m}$ distinct resistance values, where $N_m = a \times b$ is the number of memristor in a $a \times b$ crossbar array. This crossbar can be a square array, a non-square array when $a \neq b$ or a line array ($a \times 1$) when N_m is a prime number. Finally, we can define the theoretical voltage range ΔV and the optimal voltage resolution δV_{opt} of the memristor-based dc source derived from a DAC maximum voltage resolution for a given number of states

$$\Delta V = V_{\text{max}} - V_{\text{min}} = V_{\text{in}} \frac{R_{\text{HRS}} - R_{\text{LRS}}}{R_L N_m} \tag{1}$$

$$\delta V_{\text{opt}} = \Delta V \big/ N_s^{N_m} \tag{2}$$

where $R_{\text{LRS}} = 1.8$ kΩ and $R_{\text{HRS}} = 16$ kΩ are the resistance of the memristor in the lowest resistance state and the highest resistance state, respectively. These values are tied to our memristor technology. We use $R_L = 300$ Ω and $V_{\text{in}} = 0.3$ V (See Fig. 2). While we aim for a constant resistance step, the effective voltage resolution δV_{eff} will be an average resolution with a variable voltage step converging toward δV_{opt} due to the non-linearity introduced by the memristors placed in parallel.

III. Thermal Budget and Power Dissipation

The power dissipated by the circuit in the dilution fridge is an important consideration when designing cryogenic control electronics for quantum systems. For the memristor-based dc source, the two sources of dissipation are the operational amplifier and the memristors in the feedback loop placed at 4.2 K. The most recent custom cryogenic operational amplifier from [16] dissipates 1 μW but is currently unsuitable with the large output current of our circuit. While the TLC271 amplifier characterized at 4.2 K is expected to dissipate ≈500 μW in the medium-bias mode [17].

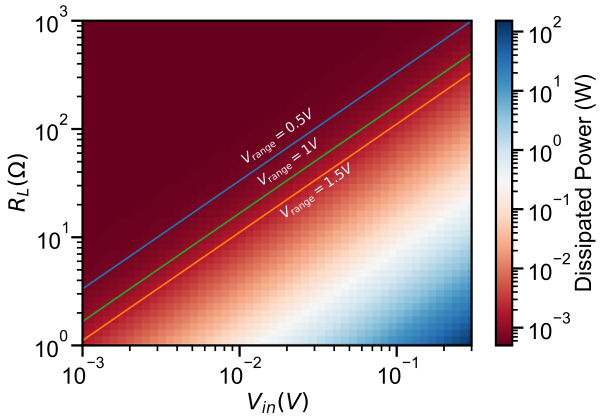

Fig. 2. **Simulation of the maximum static power dissipation of a dc source with respect to the input voltage and the load resistor.** The colored lines indicate the suitable configuration to reach a given output voltage range.

The power dissipated by the memristors is introduced by the Joule heating proportional to the current flowing V_{in}/R_L in the feedback loop and is maximum at the maximum output voltage $P_{\text{mem}}^{\text{max}} = (V_{\text{in}}/R_L)^2 R_{\text{tot}}^{\text{max}}$ where $R_{\text{tot}}^{\text{max}} = R_{\text{HRS}}/N_m$. Our memristors feature a 16 kΩ-HRS, leading to a power dissipation of 1.77 mW for a feedback current $I_{\text{fb}} = 1$ mA and a feedback resistor of nine memristors required to achieve a 1.5 V supply range and a lower dissipation for smaller ranges (See Fig. 2). Hence, the total power dissipation of a single memristor-based dc source is in the order of a milliwatt. If we assume that this power is entirely dissipated ON-chip, then ≈800 memristor-based dc source could be placed at the 4.2 K stage assuming 1.5 W cooling power. This number is bottlenecked by the low HRS of our devices. Increasing these resistances would allow to increase the PGA voltage gain A_R while decreasing the current flowing in this loop ($I_{\text{fb}} = V_{\text{in}}/R_L$) to maintain the same voltage output specifications ($V_{\text{out}} = A_V \times V_{\text{in}}$). Thus it will enable lower power dissipation. For example, $R_{\text{LRS}} = 10$ kΩ and $R_{\text{HRS}} = 100$ kΩ resistances have been demonstrated for the same TiO_2 memristor technology in [18], it would allow to reduce the maximum power dissipation down to ≈110 μW. The maximum power dissipation is decreased approximately tenfold when the HRS resistance is increased tenfold.

IV. Experimental Results

Demonstrating reversible, non-volatile, and linear resistance programming of resistive memory devices at cryogenic temperatures would offer opportunities for hybrid memristor-CMOS cryogenic electronics. To accurately tune resistance states, we use a feedback algorithm from [11].

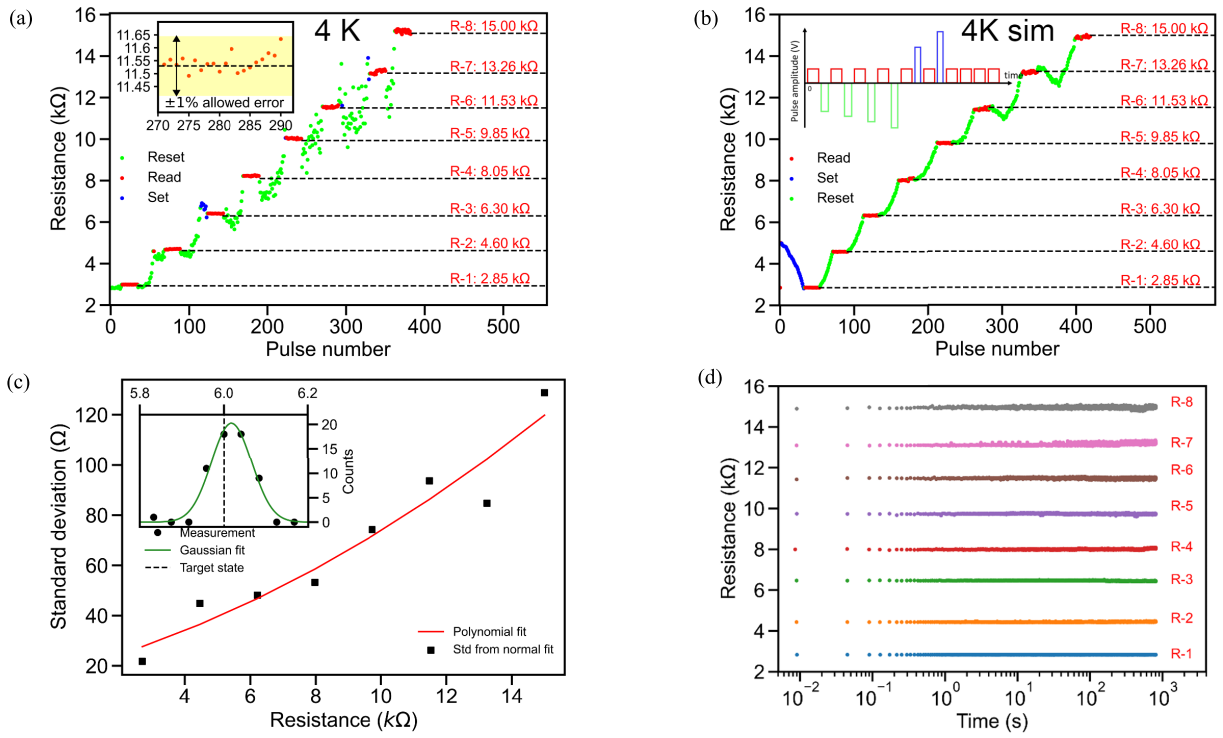

Fig. 3. **Electrical characterization of a TiO_2 memristor.** **(a)** Experimental and **(b)** simulated programming of eight equally spaced resistance states within a 1% allowed error at 4.2 K. Negative pulses are applied to the memristor to increase its resistance, while positive pulses decrease its resistance. These operations are, respectively, named RESET and SET. $V_p^{\min} = 1.0$ V and $V_n^{\min} = -1.0$ V were chosen as initial pulse amplitudes with an amplitude step of 0.02 V. The inset is a zoom-in on the 11.53 kΩ state readout within the 1% allowed error. The simulation uses our data-driven model [19]. The inset shows the typical pulse scheme used for multilevel programming. The pulsewidth is fixed to 200 ns for write pulse (green or blue pulses) and to 1 μs for read pulse (red pulses). **(c)** State programming noise at 4.2 K based on the programming standard deviations of the eight resistance states. The multilevel programming cycle is repeated ten times in a double sweep for five different memristors. The programming standard deviation is Gaussian-fit for each programming round. **(d)** Long-term stability of the eight states programed at 4.2 K. Each state is measured for 800 s every 35 ms while being biased at 0.2 V. The programed states are non-volatile for the entirety of the measurement.

At each step, we apply a 200 ns write pulse of negative amplitude to increase the resistance of the device or a positive amplitude to decrease its resistance, followed by a 1 μs/200 mV read pulse to measure the memristor resistance. The write pulse amplitude is increased linearly by 20 mV-step, starting from an initial positive amplitude $V_p^{\min}$ or negative amplitude $V_n^{\min}$ depending on the initial resistance of the memristor [see inset of Fig. 3(b)]. Once the desired resistance is reached within the relative allowed error set to 1%, the resistance is read 20 times to ensure state stability [see inset of Fig. 3(a)]. A relative allowed error yields to faster programming of the resistance states by easing the tuning conditions of higher resistance states at the cost of programming accuracy which will be compensated using a servo algorithm in the dc source context.

Measurements were conducted at 4.2 K using a Keysight B1500A semiconductor analyzer with a 200 Msamples/s waveform generator module (WGFMU) on a Lakeshore CRX-VF cryogenic probe station. The TiO_2 memristors were formed beforehand at 300 K. We demonstrate eight equally spaced resistance states (≈1.7 kΩ step) at 4.2 K, programed with approximately 50 write pulses for each state within a 1% allowed programming error. We observe that the resistance can decrease instead of increasing when applying negative write pulses which could be imputed to the larger temperature gradient in the vicinity of the conductive filament [20]. Moreover, at cryogenic temperatures, the competition between thermal- and field-activated effects is increased and could lead to additional variability during the thermally-activated RESET operation [13]. This phenomenon is more important at larger resistance values and can be defined as programming noise. One can also note reading variability from the inset of Fig. 3(a), which can be associated with mainly $1/f$ noise rising from trapping and detrapping of electrons in the vicinity of the filament and thermal noise induced by the memristor conduction modes. We evaluate a sub-1% read variability on our devices with a minimum of 0.13% at LRS and 0.4% at HRS at 4.2 K, which allows for precise and stable resistance states. By measuring the power spectral density of the memristor using an SR780 network analyzer, we calculated that the $1/f$ noise accounts for roughly 45% of the total read variability at 4.2 K. Another source of noise for memristors is random telegraph noise which our devices do not exhibit in histogram measurements. Additionally, we fit a programming noise model at 4.2 K, which accounts for cycle-to-cycle variability and device-to-device variability, by repeating multilevel programming ten times for five devices. The median value of the programming variability reported in Fig. 3(c) is 0.79% for our TiO_2 memristors in the [2.85, 15.0] kΩ-range. It indicates that the higher RESET variability at higher resistance for the first few pulses is mitigated with the simple multilevel

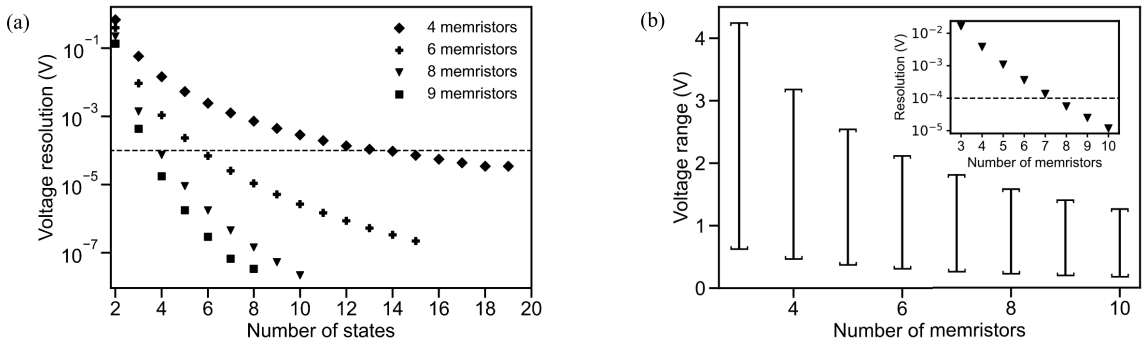

Fig. 4. **Simulated performances of the memristor-based programmable dc source.** **(a)** Evolution of the voltage resolution of the memristor-based dc source with respect to the number of states and the number of memristors in the circuit. Each memristor has its own resistance state distribution to avoid doubling resistance configurations: the ith resistance state of the jth memristor is given by $R_{\text{LRS}} + (i-1) \times (R_{\text{HRS}} - R_{\text{LRS}})/N_s + (-1)^j \times \lfloor j/2 \rfloor \times (R_{\text{HRS}} - R_{\text{LRS}})/(8N_s)$ with $i \in [\![1, N_s]\!]$ and $j \in [\![1, N_m]\!]$ where N_s is the number of resistance states and $N_m = a \times b$ the number of memristors in a $a \times b$ crossbar array. A supply voltage $V_{\text{in}} = 300$ mV, a resistance load $R_L = 300\ \Omega$, a minimum resistance $R_{\text{LRS}} = 1.8$ kΩ and a maximum resistance $R_{\text{HRS}} = 16$ kΩ were used. **(b)** Maximum voltage range and optimal resolution for a given number of memristors for five states.

programming algorithm. A better programming accuracy can be reached using a smaller voltage step for pulse amplitude and a smaller allowed error at the cost of programming time (i.e., more write pulses). Finally, we simulated the multilevel programming of our TiO_2 memristors [see Fig. 3(b)] by fitting a data-driven model [19] at 4.2 K replicating the pulsed response transient of a memristor which enables the design of cryogenic memristor circuits. This model closely replicates the programming of the resistance states, which allows hardware-based simulations of the dc source in the following section while the experimentally fit read variability is slightly underestimated in Fig. 3(b) compared to the experimental measurements Fig. 3(a) due to different B1500 configurations used for read variability measurements and multilevel programming.

We investigated the long-term stability of the TiO_2 memristors to guarantee the voltage output stability of the dc source over time. We reported a multilevel state retention over 8 h at 300 K previously in [12]. We characterized this aspect at 4.2 K to verify the non-volatility of memristors at cryogenic temperature. We report a 3-bit retention over 800 s [see Fig. 3(d)] which is $\approx 10^5$ times longer than the coherence time of current spin qubits which is in line with our previous longer-term retention measurements at room temperature.

V. Simulations and Discussions

Using the Data-Driven memristor model [19] parameters fit on our experimental data at 4.2 K, the simulated memristors are programed with simulated read/write pulses similar to experimental pulses using the same voltage-based algorithm. By varying the number of memristors in the circuit and the number of distinct resistance states, we can test several configurations and benchmark the performance of the memristor-based dc source such as the voltage resolution and the voltage range. We initially consider the circuit with no read or write variability to assess the optimal voltage resolution and range achievable in Fig. 4(a) and (b), then we added an experimentally-fit read variability and programming noise [see Fig. 3(c)].

Fig. 4(a) shows the evolution of the voltage resolution of the memristor-based dc source with respect to the number of states and the number of memristors. A higher number of resistance states leads to a better voltage resolution, experimentally limited by the device. By programming five states on nine memristors, we ideally reach a voltage resolution of $\approx 1\ \mu$V, which is well below the 100 μV target resolution required for QDs biasing. This five-state distribution is used for the following simulations. Fig. 4(b) specifies the basic electrical characteristics of the dc-source with respect to the number of memristors used. This figure shows the trade-off between the voltage resolution and the range as the number of memristors increases, this trend is explained by (1) and (2). For an increasing number of memristors, the voltage range decreases while the resolution increases exponentially. To comply with the 100 μV voltage resolution and 1 V-range requirements for QD biasing, a circuit of at least eight memristors is needed for five resistance states. In the remainder of this article, we consider a nine-memristor circuit to utilize the denser and more common 3×3 memristor-crossbar footprint.

In the preceding simulations, we chose to consider the memristors as discrete multistate resistors. This allows for efficient programming because a simple feedback resistance algorithm can be used to tune the crossbar array. Using this discrete programming approach, the output voltages depend on the resistance targets that we initially set, limiting our control of the output voltage. Instead, the dc source can be controlled to reach an arbitrary voltage to enable precise control of the PGA output voltage by exploiting the fully analog behavior of the memristors. We propose a servo algorithm, which programs the memristor crossbar to reach the target voltage accordingly. The crossbar resistance configuration is chosen in a pre-computed dataset, where the keys are the target output voltages. We converge toward this optimal resistance configuration by performing a first coarse round of programming for each memristor to roughly reach the configuration using the feedback algorithm for multilevel programming [see Fig. 3(a) and (b)]. During a second round of programming, the resistance of the last memristor of the crossbar is finely tuned with a smaller voltage step and programming tolerance

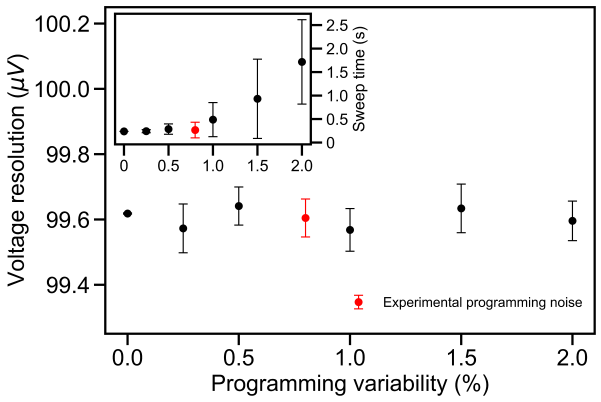

Fig. 5. **Impact of the memristor variability on the dc source voltage resolution.** A circuit of nine memristors operated by the servo algorithms is simulated. The simulations were repeated 100 times for each programming variability value to allow for statistical analysis. The voltage resolution stays constant, but the time required to program the 25 mV-sweep increases.

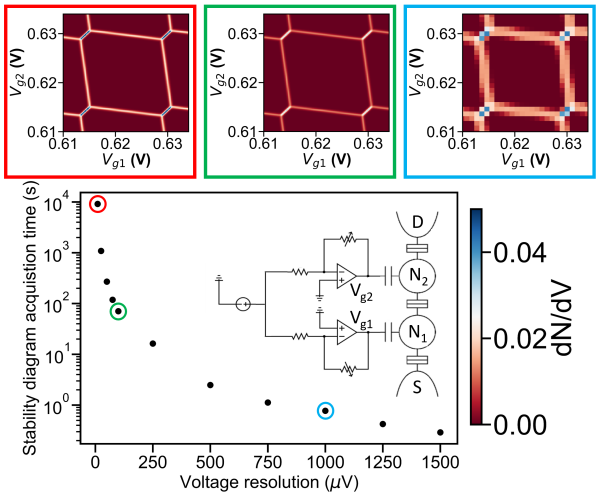

Fig. 6. **Simulation of the co-integration of a DQD and the memristor-based dc source.** Stability diagram acquisition time required with respect to the voltage resolution using two memristor-based cryogenic dc sources with a programming noise of 0.8%. The three color-framed insets show, respectively, the stability diagram obtained for a 10 μV, 100 μV and 1 mV voltage resolution. The co-integration simulations were conducted with a DQD placed at 10 mK and the dc source at 4 K using the electrical circuit depicted in the inset. The QD parameters for these simulations are $C_{g1} = C_{g2} = 1.03$ aF, $C_m = 0.4$ aF from [22].

to a new target resistance that is computed to balance the programming inaccuracy of the initial fast programming. We investigate the robustness of this algorithm by introducing variability during the programming phase of the dc source. Fig. 5 shows the voltage resolution of a nine-memristor dc source with respect to the programming variability. As the simulated programming noise increases, the voltage resolution of the dc source remains almost constant. This suggests that the memristor variability has a negligible impact on the voltage resolution of the memristor-based dc source. However, the sweep time (for a 25 mV-sweep) is increased as it takes more time to finely tune the memristor resistances. This servo algorithm allows for memristor variability robustness and a constant 100 μV step size within a 0.2% voltage resolution error using a nine-memristor circuit at 0.8% programming noise. Controlling the memristor-based dc source to reach an arbitrary voltage offers a smaller voltage resolution when compared to the resistance-driven operation mode. However, the proposed memristor-based programmable dc source still satisfies the 100 μV for the same circuit parameters and is more suitable for in situ use of the dc source.

Finally, the output voltage noise of the dc source is introduced by the memristor read variability and is given by: $(V_{\mathrm{mem}}(R))/\sqrt{N_m}$ where $V_{\mathrm{mem}}(R)$ is the read variability as a function of the memristor resistance. At 0.6 V, i.e., the sweep voltage used for the simulated stability diagrams, the output voltage noise is $(0.21/\sqrt{9}) \times 0.6 \approx 420$ μV which is comparable with the voltage noise of dc sources used in QD setups, typically in the order of 1%.

Now that we have explained the working principle of our memristor-based dc source and demonstrated how it can be operated to reach a voltage, next we simulate its co-integration with a double QD (DQD) to validate its compatibility with quantum systems. Stability diagrams are used as a standard benchmark measurement to verify the performance of a QD system. We simulated the electron transport through a DQD with respect to the voltages applied to its gates while biased by two memristor-based cryogenic dc source using equations from [21]. Two important metrics to consider for a QD biasing solution are the voltage resolution and the stability diagram acquisition time, which is estimated by counting the number of write and read pulses needed to program the memristor circuit during the simulation of the charge stability diagram. This acquisition time increases with better voltage resolution, leading to a trade-off between speed and accuracy (see Fig. 6). The insets of Fig. 6 show the derivative of a charge stability diagram to highlight the transition between the electronic regimes of the simulated DQD. We can identify the transition and occupations of the DQD for the three voltage resolutions—that is, 1 mV, 100 μV and 10 μV—thus demonstrating the control of a simulated DQD by the proposed memristor-based dc source. Although the dc source can conveniently deliver voltage resolution from 10 mV to below 1 μV, a 100 μV resolution is sufficient to clearly observe the honeycomb pattern and its triple-point. It also allows for a fast 70 s-scanning of the stability diagram. Moreover, when scaling up the dc-sources for a large number of DQDs, the stability diagram measurement can be performed in parallel. This allows to scan all DQDs within 70 s using a 100 μV resolution.

VI. Conclusion

In conclusion, we propose a memristor-based cryogenic programmable dc source for scalable in situ QD control. We demonstrate that this control approach fulfills the baseline requirements for QD biasing (i.e., a 100 μV-resolution over a 1 V-range) while keeping a limited number of memristors, allowing for a scalable biasing solution. We demonstrated the effective biasing of a simulated DQD using a non-ideal TiO_2/Al_2O_3 memristor model, pointing out that memristor

variability will not cause electronic regime changes that would be detrimental to quantum computation. We reported successful multilevel pulsed programming of TiO_2-based memristor at 4.2 K. Moreover, the scalability is limited by the total power dissipation of the dc source but still hints at a feasible integration of a few hundred of dc sources at 4.2 K. More resistive memristors would allow to decrease the power dissipation by limiting the current flowing in the feedback loop in order to close the gap with the switched-capacitor demonstrating sub-nanowatt dissipation [8].

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Data Availability: The Python library that was developed to simulate the control performed by the proposed dc source is available at GitHub. Data supporting this work will be uploaded to an online repository.

Author Contributions: Pierre-Antoine Mouny and Sébastien Graveline performed the experiment; Abdelouadoud El Mesoudy, Raphaël Dawant, Pierre Gliech, and Serge Ecoffey fabricated the memristor devices; Pierre-Antoine Mouny analyzed and post-processed the measurement and simulation data; Pierre-Antoine Mouny, Sébastien Graveline, and Marc-Antoine Roux developed the simulation framework; Yann Beilliard, Michel Pioro-Ladri, and Dominique Drouin conceived and supervised the project; and Pierre-Antoine Mouny wrote the manuscript with input from all of the authors.

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