High-Performance Top-Gated and Double-Gated Oxide–Semiconductor Ferroelectric Field-Effect Transistor Enabled by Channel Defect Self-Compensation Effect

Chun-Kuei Chen, *Graduate Student Member, IEEE*, Sonu Hooda, Zihang Fang, Manohar Lal, Zefeng Xu, Jieming Pan, Shih-Hao Tsai, *Graduate Student Member, IEEE*, Evgeny Zamburg, *Member, IEEE*, and Aaron Voon-Yew Thean, *Senior Member, IEEE*

***Abstract*— In this article, we demonstrate a low-thermal budget defect-engineered process to achieve top-gated (TG) oxide–semiconductor ferroelectric field-effect transistors (FeFETs). The demonstrated TG FeFETs, with the channel length scaled down to 40 nm, exhibit a highly stabilized ferroelectric memory window (MW) of 2 V and a high current ON/OFF ratio of 10^6. This is achieved by an engineered $InGaZnO_x$ (IGZO) and $InSnO_x$ (ITO) heterojunction channel that produces the defect self-compensation effect to passivate the intrinsic oxygen-deficient defects, existing in the indium-gallium-zinc-oxide (IGZO) channel interface and bulk. Effective interface/bulk defects passivation with good control of defect-induced channel carrier concentration has been notoriously difficult to achieve. Hence, realizing performant TG oxide-based FeFETs with back-end-of-line (BEOL) thermal budget constraints remains a fundamental challenge. Our study shows that heterojunction channel engineering on FETs and FeFETs can be a reliable solution to overcome this challenge. With such a technique, we can now enable double-gated (DG) ITO–IGZO FeFET and FETs. Such devices can enable BEOL-compatible reconfigurable nonvolatile logic switches that provide extremely low off-state leakage, high switch conductance ratio, and memory read-write disturb-free features.**

***Index Terms*— Double gated (DG), ferroelectric, ferroelectric field-effect transistors (FeFETs), FETs, HfZrO, InGaZnO, InSnO, nonvolatile logic, oxide–semiconductor, top gate (TG).**

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The authors are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117582, and also with the Singapore Hybrid-Integrated Next-Generation μ-Electronics (SHINE) Centre, Singapore 117583 (e-mail: Aaron.Thean@nus.edu.sg).

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I. Introduction

MONOLITHIC 3-D (M3-D) integration of reconfigurable nonvolatile logic circuits can enable ultraenergy-efficient 3-D ICs by bringing memory elements closer to compute components and providing highly flexible system run-time reconfiguration capabilities that are difficult to achieve solely with conventional VLSI [1], [2], [3], [4]. Growing reports have also shown that oxide–semiconductors, such as amorphous indium-gallium-zinc-oxide (IGZO), can replace the conventional silicon (Si)-based transistor channel [5], [6], [7], [8]. This offers exciting M3-D integration possibilities that overcome the back-end-of-line (BEOL) low-*k*/Cu low thermal-budget process constraints owing to its low-temperature process, excellent wafer-scale deposition uniformity, and modestly high electron mobility [9]. Moreover, IGZO transistors have been shown to be compatible with ferroelectric memory materials, such as Zr-doped HfO_2 (HZO), to realize BEOL-compatible ferroelectric field-effect transistors (FeFETs) [10], [11], [12].

Despite the maturity of IGZO thin-film transistors, the interface/bulk defects are less well understood compared to Si transistors, especially in the context of high-*k* gate-stack interaction with IGZO interfaces and defects, which contributes to the transistor instability issues. It has been reported from experiments and theoretical calculations that the defects in the as-deposited IGZO film may be of varied origins, such as interstitial oxygen atoms [13], [14], weakly bonded oxygen atoms [15], [16], oxygen vacancies (V_o) [17], [18], dangling bonds [19], [20], undercoordinated metals [21], [22], and H-related defects [23], [24]. The resultant defect energy states can distribute from shallow to deep levels in the band gap of IGZO channel bulk and interfaces [25]. In particular, Nakashima et al. [26] have reported that the origin major donor state of the IGZO channel is H atom occupancy of V_o (V_oH).

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Given that V_oH acts as the major electron donor, the IGZO channel usually becomes heavily n-doped after atomic-layer-deposition (ALD)-based ferroelectric top-gated (TG) dielectric deposition since the ALD deposition chamber is typically hydrogen abundant [27], [28]. Although different postdeposition annealing (PDA) treatments for defects passivation or channel carrier concentration modulation for IGZO-based devices have been widely studied [29], [30], [31], the high sensitivity and complexity of the channel interface/bulk defects formation as a function of different process ambients (e.g., H_2, N_2, or O_2) render the PDA effects unreliable. In this respect, achieving a balance between oxygen-related defects passivation and V_oH-induced carrier concentration control for TG IGZO-based FETs is especially difficult. For example, utilizing PDA in an oxygen ambient to reduce the IGZO channel carrier concentration may lead to excessive interstitial oxygen atoms or weakly bonded oxygen defects generation. To deposit a low-defectivity high-k gate dielectric on the IGZO channel would require a difficult balance between the PDA defect passivation effects on the high-k dielectric and the defect concentration sensitivity of the IGZO. Therefore, a performant BEOL TG IGZO-based FeFET has yet to be realized to date, and most reported BEOL-compatible oxide-based FeFETs are bottom-gated (BG) structures, where the IGZO channel is deposited after the ferroelectric dielectric deposition [10], [11], [32], [33], [34].

Due to the use of top–down lithography and patterning, self-aligned BG devices are difficult to manufacture in high densities, and their gate and contact dimensions are challenging to scale [35], [36], [37]. Nonself-aligned BG devices tend to suffer from gate–source/drain (G–S/D) misalignment issues that influence the source-side carrier injection energy barrier, consequently leading to the current drive variation and gate delay degradation [38]. To ensure a higher current drive and reduce device fluctuations, the bottom gate should be designed large enough with sufficient gate-contact overlap margin. However, the penalty of extra gate-channel-S/D overlap parasitic capacitance arises, making BG-based devices inadequate for dense high-speed circuits [39], [40]. Thereby, establishing a reliable TG process for oxide-based FeFET is necessary to enable its G–S/D self-aligned capability and the further scaling of transistor feature size.

To this end, we show that TG and double-gated (DG) IGZO FeFETs with stable ferroelectric memory performance can be realized within a low-thermal budget. This is achieved through the use of an $InSnO_x/InGaZnO_x$ (ITO–IGZO) heterojunction channel that triggers defect self-compensation effect to intrinsically passivate IGZO channel interface/bulk defects. With such a method, the channel-interface-stabilized TG and DG ITO–IGZO FeFETs exhibit superior memory properties, including large and stable memory window (MW), good memory retention estimated over ten years, and decent memory programming/erasing endurance of 10^7 cycles. Especially, our FeFETs show a significant enhancement of drive current and the electrostatic control on the transistor channel, such as competitively high electron effective mobility of 57 cm^2/Vs, the normally-off feature, an minimum subthreshold swing (SS) of 68 mV/decade, and I_{on}/I_{off} ratio of 10^7, setting performance precedence for oxide-based FeFETs to be leveraged for nonvolatile logic applications. More details and a comprehensive analysis of heterojunction channel engineering, defect self-compensation effect, and carrier concentration control based on the FETs and FeFETs are also provided.

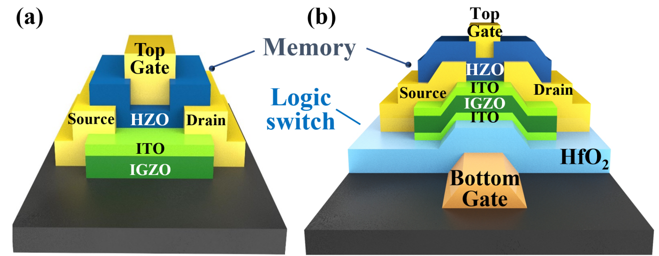


Fig. 1. Schematic of the fabricated (a) TG FeFETs and (b) DG FeFETs.

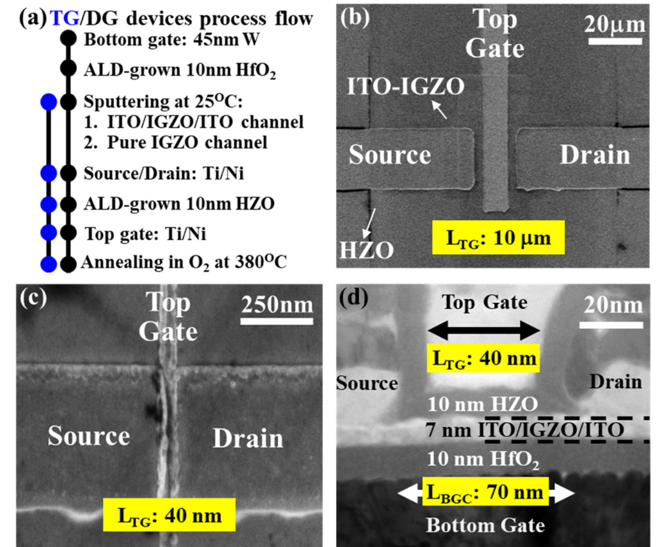


Fig. 2. (a) Key process flow for TG FeFETs and DG FeFETs. (b) SEM image of the TG FeFETs with L_{TG} of 10 μm and (c) L_{TG} of 40 nm. (d) Cross-sectional TEM image of the fabricated short channel DG FeFETs.

II. Experimental Procedure

A. Device Fabrication

Fig. 1(a) and (b) illustrates the schematic cross-sectional structure of the fabricated TG and DG transistors, where the top gate stacks are both designated to be HZO-based ferroelectric memory components. We integrate the TG FeFET and BG FETs into a combined DG architecture, in which the BG terminal with HfO_2 high-k gate-stack as a conventional nonmemory transistor channel can enable a separate memory-read electrode or additional logic switching functionality. This allows the DG device to be reconfigured between memory and logic modes, alleviating the memory read/write disturb issue, that challenges the single-gated FeFETs. Fig. 2(a) shows the device key fabrication steps common to TG and DG devices. For defect passivation, a thin-film ITO is integrated into the top and bottom channel interface. In contrast, the control FeFETs IGZO-only channel (without ITO) is also fabricated for comparison. Notably, the TG and DG FeFETs'

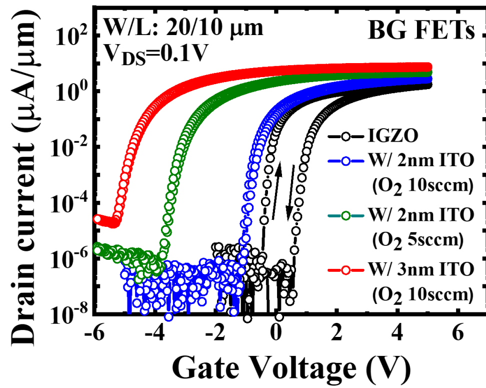


Fig. 3. Measured $I_{DS} - V_{GS}$ curve of BG FETs with different channel configurations (black: 30-nm IGZO-only; blue: 2-nm ITO (O_2 of 10 sccm)/30-nm IGZO; green: 2-nm ITO (O_2 of 5 sccm)/30-nm IGZO; red: 3-nm ITO (O_2 of 10 sccm)/30-nm IGZO).

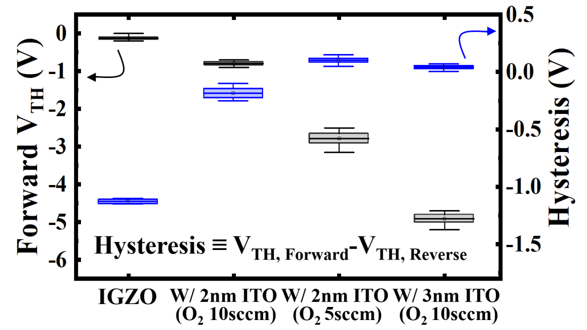


Fig. 4. Statistical distribution of forward threshold voltage ($V_{TH,\ Forward}$) and hysteresis of the BG FETs with different channel configurations.

maximum thermal processes are limited to 380 °C, ensuring their suitability as BEOL nonvolatile memory. Fig. 2(b) shows the top-view scanning electron microscope (SEM) image of the TG FeFETs with an L_{CH} of 10 μm. We also fabricated short-channel DG devices with a top-gate length (L_{TG}) of 40 nm to investigate the impact of channel length scaling on the defect self-compensation effect [Fig. 2(c) and (d)]. The bottom-gate channel length (L_{BGC}) was defined as 70 nm, equal to the source-to-drain length.

B. ITO–IGZO Heterojunction Channel Engineering

Since stoichiometric bulk-phase ITO is too conductive and not suitable as a transistor channel, a nonstoichiometric ultrathin ITO is developed for our transistor integration. The sheet resistance of ITO film is monitored and carefully tuned by oxygen ambient during physical deposition. We start by optimizing different compositions of the ITO–IGZO heterojunction channels with a BG FET test structure, irrespective of the consequence of the ferroelectric polarization. This allows us to investigate the sole impact of the ITO layer on defect passivation and channel carrier doping. The heterostructure channel was sputtered at room temperature (RT), starting with the ultrathin ITO film, followed by a 30-nm IGZO. The conductivity of ITO film was tuned by controlling O_2 gas flow (down to 5 sccm) during sputtering deposition. Here, BG FETs were fabricated with the four different channel configurations as follows: 1) 30-nm IGZO-only; 2) 2-nm ITO (O_2 of 10 sccm)/30-nm IGZO; 3) 2-nm ITO (O_2 of 5 sccm)/30-nm IGZO; and 4) 3-nm ITO (O_2 of 10 sccm)/30-nm IGZO. The IGZO film was deposited with a controlled thickness of 30 nm and an O_2 gas flow of 10 sccm.

Fig. 3 shows the measured transfer characteristics ($I_{DS}-V_{GS}$ curve) of these BG FETs with an L_{CH} of 10 μm. Here, the direction of hysteresis is defined as the V_{TH} difference between the forward ($V_{TH,Forward}$) and reverse ($V_{TH,Reverse}$) sweeping. For the IGZO-only FETs, we observe a clockwise $I_{DS} - V_{GS}$ hysteresis loop that typically implies a serious defect-induced electron trapping/detrapping phenomenon at the channel–dielectric interface or the channel bulk of the n-channel FETs, which is undesired [41]. On the other hand, the hysteresis-free loop is obtained in the device with a channel of 2-nm ITO (O_2 of 10 sccm)/30-nm IGZO, and the $V_{TH,Forward}$ shifts negatively. This gives us the first hint that depositing a thin ITO film along the interface between the IGZO and gate insulator can mitigate the undesired trapping/detrapping events. However, the channel carrier concentration, dominating V_{TH} of a transistor, will increase with the presence of the ITO thin film. A serious negative shift of $V_{TH,Forward}$ is observed from the measured $I_{DS} - V_{GS}$ curves of the FETs with a 2-nm ITO (O_2 of 5 sccm)/30-nm IGZO channel. This suggests that the ITO film conductivity increases with the reduced O_2 gas flow during deposition. We also notice that further increasing the ITO thickness to 3 nm (O_2 of 10 sccm) leads to an abrupt negative shifting of $V_{TH,Forward}$ of FETs. Also, the off-state current of the device increases, resulting in a degraded current on/off ratio. Fig. 4 shows the statistical measurement results based on four channel types. The trend of the channel carrier concentration increasing with thicker ITO film or lower O_2 flow is further certified. These results fit well with our observations from hall measurements [Fig. 5(a)]. The as-deposited channel carrier concentration will increase from 7×10^{16} to 2×10^{18} cm^{-3} after increasing the ITO film thickness from 2 to 3 nm. Notably, an enhancement mode transistor operation, namely, a normally-off feature, is wished to simplify gate drive circuit design and reduce the leakage power consumption [42]. Since the undesired clockwise hysteresis loop can be offset for all the bilayer channels, the above results suggest that an ITO layer deposited under the O_2 flow of 10 sccm with a thickness of 2 nm is the optimized condition to be integrated with the IGZO channel. Fig. 5(b) compares the measured drain–current–voltage transfer characteristics ($I_{DS}-V_{DS}$ curve) of the FETs with IGZO-only channel and 2-nm ITO (O_2 of 10 sccm)/IGZO channel, in which the V_{GS} is increased from 0 to 5 V with a step of 0.5 V. An obvious drive current boosting is achieved with the FET with ITO–IGZO channel.

III. Results and Discussion

A. Channel Defects Self-Compensation Effect on TG ITO–IGZO FeFETs

We applied the learning from heterojunction channel engineering to stabilize top-channel FeFETs performance. Here, we fabricated TG FeFETs based on the optimized ITO–IGZO

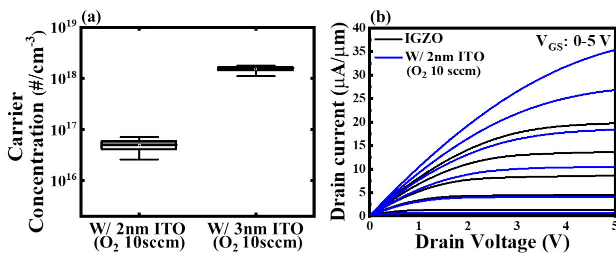


Fig. 5. (a) Extracted carrier density of 2-nm ITO (O_2 of 10 sccm)/30-nm IGZO and 3-nm ITO (O_2 of 10 sccm)/30-nm IGZO substrates based on Hall measurements. (b) Measured $I_{DS} - V_{DS}$ curve of BG IGZO-only FETs and the optimized BG ITO–IGZO FETs, in which ITO is deposited at O_2 of 10 sccm.

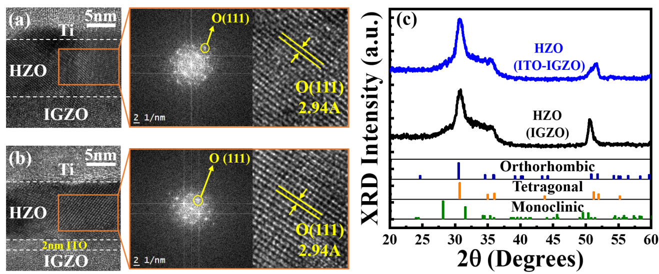


Fig. 6. (a) HR TEM images of low-temperature processed TG IGZO FeFETs. (b) TG ITO–IGZO FeFETs. The electron diffraction patterns for both devices were obtained through the fast Fourier transform from the HR-TEM image. The measured interatomic distance was approximately 2.94 Å, indicating the existence of HZO ferroelectric orthorhombic (111) on both devices. (c) GI-XRD analysis of HZO/IGZO/SiO_2 and HZO/ITO/IGZO/SiO_2 samples.

channel configuration and the control TG IGZO-only FeFETs. High-resolution transmission electron microscopy (HR-TEM) analysis reveals the polycrystalline morphologies of the HZO dielectric layer on both channel types [Fig. 6(a) and (b)]. The lattice-fringe analysis is utilized to capture the HZO polycrystallization phase. We first obtain the electron diffraction patterns through the fast Fourier transform analysis from the HR-TEM image. After that, the interatomic distance was measured at approximately 2.94 Å, corresponding to the d-spacing value of HZO ferroelectric orthorhombic (111). Fig. 6(c) shows the X-ray diffraction (XRD) spectroscopy analysis based on HZO/IGZO/SiO_2 and HZO/ITO/IGZO/SiO_2 samples. We observe the clear diffraction peaks centered at 30.6° and 35.0° that correspond to the peak position of orthorhombic (111) and orthorhombic (200), respectively. Thus, we can validate the successful HZO ferroelectric phase formation on top of ITO–IGZO and IGZO-only substrates.

Nevertheless, we find out that a stable MW is only present for the TG ITO–IGZO FeFETs, while the TG IGZO FeFETs show a loss of hysteresis or clockwise $I_{DS} - V_{GS}$ transfer loop [Fig. 7(a)]. As mentioned earlier, the clockwise hysteretic loop typically represents the undesired interfacial/bulk electron trapping/detrapping events, which can offset the desired ferroelectric anti-clockwise hysteretic loop. In such a case, the expected MW in the TG IGZO FeFETs is unfortunately lost. This tendency is further confirmed by the device statistical measurements of SS and hysteresis, as shown in Fig. 7(b) and (c). Most TG ITO–IGZO FeFETs exhibit a stable MW

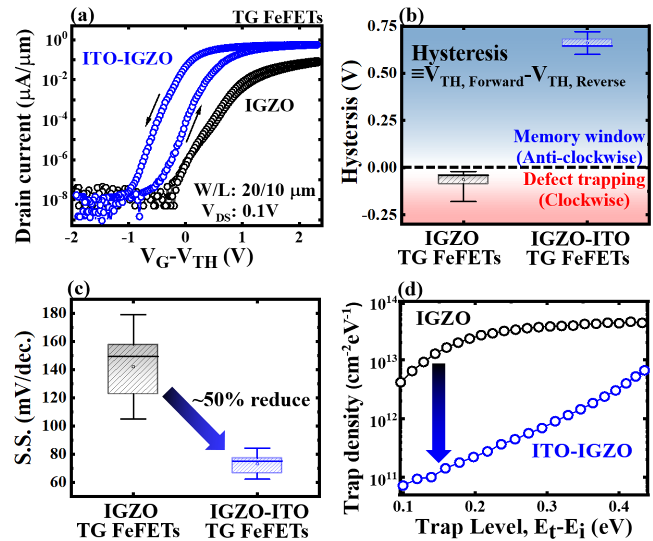
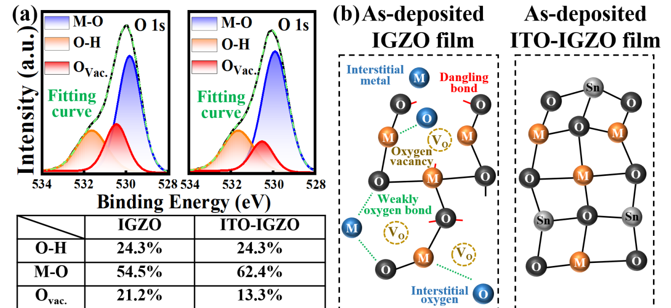


Fig. 7. (a) Measured $I_{DS} - V_{GS}$ transfer curve of TG IGZO FETs and TG ITO–IGZO FETs. The transfer curves were compared by normalizing V_{GS} with respect to V_{TH}. (b) Statistical distribution of clockwise hysteresis of TG IGZO FeFETs and anti-clockwise hysteresis MW of TG ITO–IGZO FeFETs. (c) Statistical distribution of SS extracted from both TG FeFETs. (d) Extracted defect density of TG IGZO FeFETs and TG ITO–IGZO FeFETs.



	IGZO	ITO-IGZO
O-H	24.3%	24.3%
M-O	54.5%	62.4%
$O_{vac.}$	21.2%	13.3%

Fig. 8. (a) O_{1s} XPS spectra of the as-deposited ITO–IGZO and IGZO samples. (b) Illustrated as-deposited ITO and ITO–IGZO film, showing the mechanism of the channel defect self-compensation effect. Introducing metal ions (i.e., Sn^{2+}) with higher BDE with oxygen atoms can suppress the oxygen-deficient species defect and undercoordinated metals at the oxide–semiconductor channel bulk and interface.

from 0.57 to 0.75 V. Also, the average SS is improved by 50% in the TG FeFETs with the ITO–IGZO heterojunction channel. The poor SS in the n-channel transistor has been attributed to the deep-level defects [43]. Here, the ITO layer contributes to deep-level defect passivation. This is further attested by the extracted bulk/interface defect density results based on the high–low-frequency capacitance–voltage (C–V) technique [44]. Flat band voltage is estimated by the second derivative method [45]. Fig. 7(d) shows the extracted defect density of states based on the measured frequency-dispersive C–V characteristics [46]. The results indicate that the deep-level interface/bulk defect is highly passivated within the ITO–IGZO heterojunction channel.

We further explore the role of ITO film from the material perspective by conducting an X-ray photoelectron spectroscopy (XPS) analysis. Fig. 8(a) shows the XPS O_{1s} spectra of the as-deposited IGZO and ITO–IGZO substrates. The

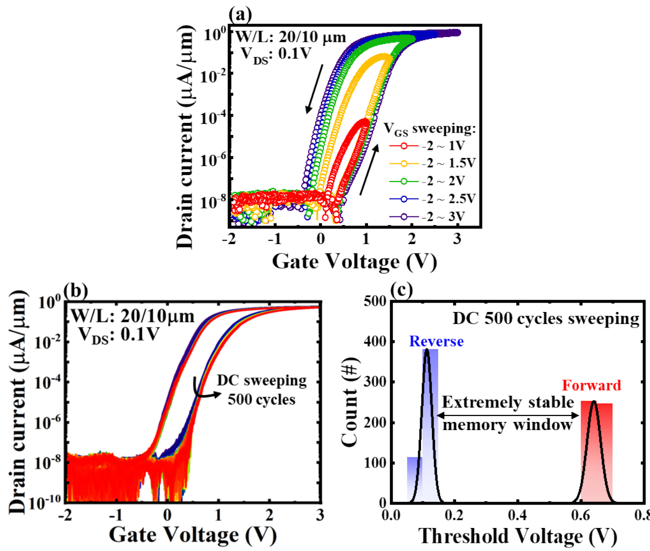


Fig. 9. (a) Measured $I_{DS} - V_{GS}$ transfer curve of TG ITO–IGZO FeFETs with the fixed $V_{GS,\ Negative}$ of −2 V and the $V_{GS,\ Positive}$ varied from 1 to 3 V. (b) Measured $I_{DS} - V_{GS}$ transfer curve of TG ITO–IGZO FeFETs sweeping for 500 dc cycles. (c) Statistical distribution of $V_{TH,\ Forward}$ and $V_{TH,\ Reverse}$ during the dc voltage sweeping experiment.

data-fitting results show that the peak intensity of the O–H bond remains the same for both channels. However, the M–O bond peak intensity is increased from 54.5% to 62.4%, while the oxygen vacancy peak intensity is reduced in the ITO–IGZO sample. This result indicates that the IGZO channel defects originating from interstitial oxygen atoms, weakly bonded oxygen atoms, undercoordinated metals, and oxygen vacancies have been suppressed by integrating with a thin ITO film. This phenomenon has been reported as the channel defect self-compensation mechanism that happens when different oxide–semiconductor channels are stacked [47]. In such a bilayer channel system, the intrinsic oxygen-related, metal-related defects can be passivated by the M^{+} ions with a higher bond dissociation energy (BDE) with oxygen atoms. In our ITO–IGZO heterojunction channel, the BDE of Sn–O bond is reported at 528 kJ/mol, significantly higher than In–O (320 kJ/mol), Zn–O (159 kJ/mol), and Ga–O (285 kJ/mol) bonds [48]. Thus, oxygen-deficient defects, widely distributed from shallow to deep states in the IGZO bandgap, can be efficiently suppressed by Sn^{2+} ions, as shown in Fig. 8(b). As a result, we observe the improved SS and drive current of the TG ITO–IGZO FeFETs. This mechanism has also been discovered in the terbium-incorporated indium oxide ($Tb{:}In_2O_3$) channel system [49].

B. High-Performance BEOL-Compatible TG FeFETs

The electrical characterization is further carried out on TG ITO–IGZO FeFETs with an L_{CH} of 10 μm. Fig. 9(a) plots the measured anti-clockwise $I_{DS} - V_{GS}$ transfer loop with the fixed V_{DS} of 0.1 V, $V_{GS,\ Negative}$ of −2 V, while $V_{GS,Positive}$ is varied from 1 to 3 V. The result shows an increase of MW with a higher $V_{GS,Positive}$. The MW will eventually saturate under $V_{GS,Positive}$ of 3 V. This has been explained due to a gradual ferroelectric domain switching with the increasing V_{GS} applied on

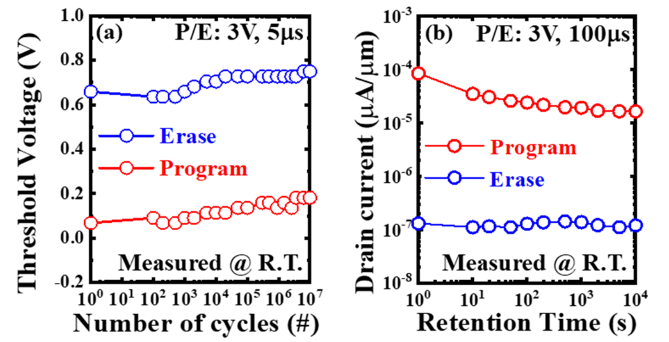


Fig. 10. (a) Measured endurance and (b) retention performance of TG ITO–IGZO FeFETs at RT. Our TG ITO–IGZO FeFETs exhibit a high endurance of 10^7 cycles and a sustainable I_{ON}/I_{OFF} ratio $> 10^2$ after 10^4 s.

FeFETs [50]. Fig. 9(b) depicts the extremely stable $I_{DS} - V_{GS}$ transfer loop of our TG devices during the dc voltage sweeping for 500 cycles. The TG ITO–IGZO FeFETs show an extremely stable MW, a high I_{on}/I_{off} ratio, low substrate leakage, and an unchanged normally-off feature. More notably, no degradation of SS is observed, indicating a negligible interface/bulk defect generation. Fig. 9(c) summarizes the statistical distribution of $V_{TH,Forward}$ and $V_{TH,Reverse}$ during dc voltage sweeping test, in which both V_{TH} variation is within 0.1 V.

We further characterize the memory nonvolatility and read–write reliability of our TG ITO–IGZO FeFETs by performing the retention and endurance measurement at RT. For the endurance test, alternating square programming/erasing pulse with the pulse amplitude of ±3 V and period 5 μs was applied. Fig. 10(a) shows a stable MW over 10^7 endurances cycling on the devices. For the retention test, a prolonged square programming/erasing pulse of ±3 V and period 100 μs was applied to the TG, while the source and drain terminals were grounded. After the memory was programmed to be on/off state, the channel current was monitored at V_{GS} of 0 V and V_{DS} at 0.1 V over time. We observed a robust channel I_{on}/I_{off} ratio, which was estimated to be 10^2 after ten years by extrapolating the retention time scale [Fig. 10(b)]. The above results support the proposition of applying the channel defect self-compensation effect to stabilize and enhance the TG ferroelectric memtransistor performance.

C. Ultrascaled BEOL-Compatible DG FeFETs

Next, we investigate the fabricated short-channel DG devices with the symmetry and ultrathin ITO–IGZO–ITO channel, shared by TG FeFETs and BG FETs. Fig. 11(a) plots the measured $I_{DS} - V_{GS}$ curve of TG ITO–IGZO FeFETs, showing a large MW of 2 V, a high I_{on}/I_{off} ratio of 10^6, an I_{on} of 1 μA/μm at V_{DS} of 0.1 V, and the normally-off feature. Fig. 11(a) plots the I_{on}/I_{off} of the TG ITO–IGZO device as a function of the memory programming pulse amplitude and width, ranging from 2 to 5 V and 1 μs to 10 ms, respectively. The 2-D contour shows a tunable memory state of the I_{on}/I_{off} ratio from 10 to 10^7. We have also measured the $I_{DS} - V_{GS}$ curve of short-channel BG ITO–IGZO FETs, as shown in Fig. 11(c). The transfer curve features hysteresis-free, similar

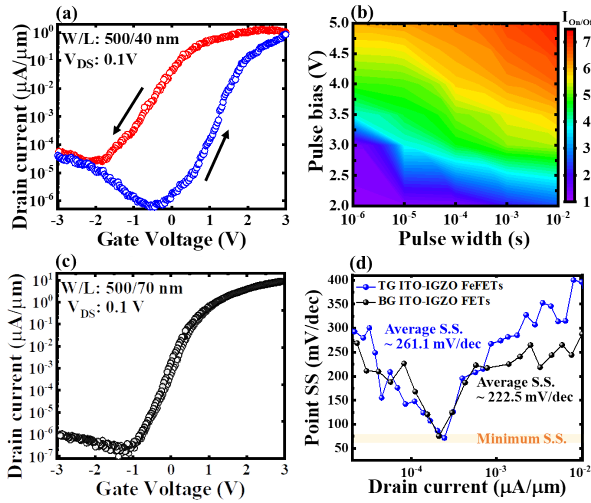


Fig. 11. (a) Measured $I_{DS} - V_{GS}$ transfer curve of TG ITO–IGZO FeFETs with a channel length scaled down to 40 nm. (b) Two-dimensional contour summarized the I_{ON}/I_{OFF} of TG ITO–IGZO FeFETs as a function of the memory programming pulse amplitude and width. (c) Measured $I_{DS} - V_{GS}$ transfer curve of BG ITO–IGZO FETs with a channel length scaled down to 70 nm. (d) Extracted SS of short-channel TG ITO–IGZO FeFETs and BG ITO–IGZO FET.

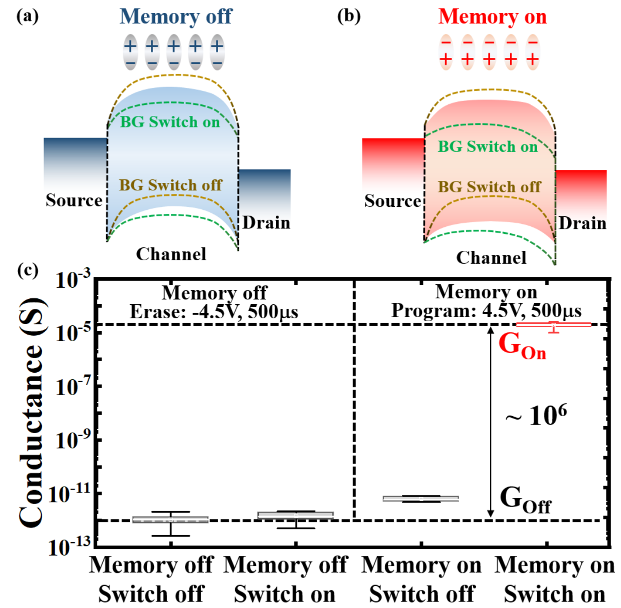


Fig. 12. Illustrated source–channel–drain band diagram of the DG device based on the four operation modes as follows: (a) Memory-OFF/Switch-OFF, Memory-OFF/Switch-ON. (b) Memory-ON/Switch-OFF, Memory-ON/Switch-ON. (c) Four operation reconfigurability test of DG switch with a statistical distribution of the channel conductance.

to what we observed from the long-channel ITO–IGZO FETs. Our BG devices also show excellent drive characteristics, such as a high I_{on}/I_{off} ratio of 10^7 and a high I_{on} of 10 μA/μm at V_{DS} of 0.1 V. Fig. 11(d) shows the extracted point SS of TG FeFETs and BG FETs. By engineering the symmetry ITO–IGZO–ITO heterostructure channel, a minimum SS value of 68 mV/decade is found in both devices. Given that the extracted shallow level bulk/interface Dit is still in the range of 10^{12}–10^{13} cm^{-2}eV^{-1}, the average wide-range SS of both ITO–IGZO devices is still poor. Therefore, the passivation of the shallow-level bulk/interface defects and the scaling of the gate dielectric thickness are still necessary to further improve the overall transfer curve of the transistor.

D. BEOL-Compatible DG FeFETs With Reconfigurable Nonvolatile Logic Operation

The fabricated DG device is designed to be a dual-mode memory-logic device. Here, we discuss the operation of the DG device as a nonvolatile logic switch and its technological advantages. Fig. 12(a) and (b) illustrates the source–channel–drain band diagram of the DG device based on the operation modes. Given that both TG FeFET and BG FET share the ITO–IGZO–ITO channel, the initial transistor channel potential state will be determined by the encoded TG memory ferroelectric polarization field. The BG FET, on the other hand, will control the final switch conductance state. By separating the memory and logic transistor gate terminals, the nonvolatile memory state encoded on the TG FeFET can be disturbance-free from the BG FET operation. Based on the operation method mentioned above, our DG device exhibits the reconfigurability between the following four modes: 1) memory-off/switch-off; 2) memory-off/switch-on; 3) memory-on/switch-off; and 4) memory-on/switch-on.

Fig. 12(c) shows the four-modes reconfigurability test results. The programming/erasing pulse amplitude and time were decided to be ±4.5 V and 500 μs. First, the programming/erasing pulse is applied to the TG with the S/D grounded. Afterward, we turn on the BG FET to read the channel conductance state at V_{BG} of 0.5 V and V_{DS} of 0.1 V. When the TG FeFET is erased to the memory -off state, the switch exhibits the channel conductance of 10^{12}S, indicating an efficient TG ferroelectric memory field effect on the shared channel. Thus, the power consumption for those DG switches that are not operated can be reduced. After the programming operation, our DG switch becomes a memory-on state, and the BG FET can control the channel conductance. Fig. 12(c) shows an excellent controllability of BG FET over the DG switch with the G_{on}/G_{off} ratio of 10^6.

We next characterize the compatibility of our DG devices as a nonvolatile memory switch array based on the V/2 bias scheme, as shown in Fig. 13(a). The word and bit lines are connected to the TG and BG terminals, respectively. In such a scheme, the memory state of the selected DG switch can be programmed or erased through the TG FeFET at V_{TG} of write voltage (V_W), while the BG FET will be grounded. The applied V_W pulse amplitude and period are the same as we utilized in the reconfigurability test. Thus, the selected switch can be programmed to the on-state with a G_{on}/G_{off} ratio of 10^6 [Fig. 13(b)]. The results show that those switches in the half-selected rows, columns, and unselected cells are disturbance-free during the programming operation. The same disturbance-free feature is obtained during the erasing operation [Fig. 13(c)]. We have also investigated the sneak path leakage currents in our switch fabric. The sneak path leakage has been reported as a typical issue in a two-terminal

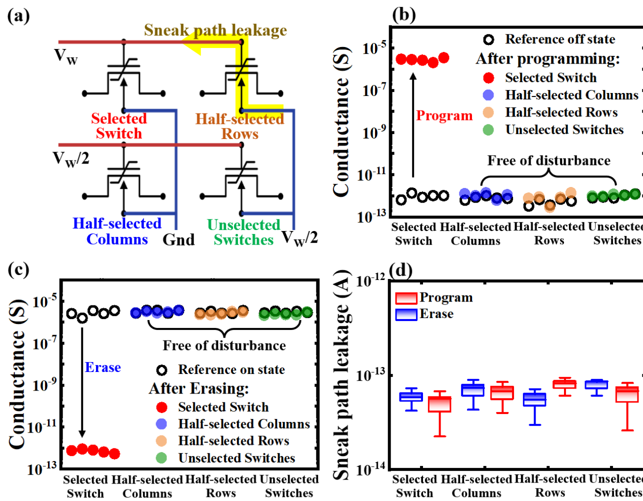


Fig. 13. (a) Illustrated write operation of DG memory switch in a nonvolatile switch array fabric based on the commonly used V/2 bias scheme. (b) Measured programming operation. (c) Erasing operation for the selected cell in the switch array fabric. The memory write disturbance of the half-selected rows, columns, and unselected cells is investigated as well. (d) Measured sneak path leakage of all the switches during the programming and erasing operation.

memristor-based memory array, leading to severe memory array performance degradation [51]. In our switch fabric, the sneak path leakage is extremely low for all the switches during the programming and erasing operation [Fig. 13(d)]. This is explained by a much longer and unlikely sneak path for the DG switch, in which the electron has to pass through the ALD-based BG and TG high-quality gate insulator layers to contribute to leakage. Hence, our nonvolatile DG switch is intrinsically free of sneak path leakage in the array fabric operation.

IV. Conclusion

In this article, we demonstrate that a reliable ultra-scaled low-thermal budget oxide-based top-channel FeFET can be attained by introducing the channel defect self-compensation effect. We provide the study of channel defect self-compensation through a comprehensive material study and electrical characterization of the heterojunction channel engineering on both FeFETs and FETs. With such a method, the memory and drive characteristics of the TG oxide-based FeFETs are considerably enhanced. We further integrate the FeFET and FET into a combined DG structure and demonstrate its potentials and advantages as a nonvolatile switch, pushing the boundary of BEOL FeFETs toward dense M3-D integration of memory and reconfigurable nonvolatile logic circuits applications.

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