Record RF Power Performance at 94 GHz From Millimeter-Wave N-Polar GaN-on-Sapphire Deep-Recess HEMTs

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***Abstract*— In this article, N-polar GaN-on-sapphire deep-recess metal–insulator–semiconductor (MIS)-high-electron-mobility transistors (HEMTs) with a breakthrough performance at *W*-band are presented. Compared with prior N-polar GaN MIS-HEMTs, a thin GaN cap layer and atomic layer deposition (ALD) ruthenium (Ru) gate metallization were used along with high-quality GaN-on-sapphire epitaxy from Transphorm Inc. Before SiN passivation, 94 GHz large signal load–pull shows that the transistor obtains a record-high 9.65 dB linear transducer gain and demonstrated 42% power-added efficiency (PAE) with associated 4.4 W/mm of output power density at 12 V drain bias. By biasing the drain at 8 V, the device shows an even higher PAE of 44% with an associated 2.6 W/mm of output power density. After SiN passivation, the fabricated N-polar GaN-on-sapphire HEMTs show a high PAE of 40.2% with an associated 4.85 W/mm of output power density. Furthermore, a very high output power density of 5.83 W/mm with 38.5% PAE is demonstrated at a 14 V drain bias. This power performance shows significant efficiency improvement over previous N-polar GaN-on-SiC and demonstrates a combined efficiency and power density beyond what has been reported for Ga-polar devices, in spite of the low-thermal-conductivity sapphire substrate. This shows that N-polar GaN-on-sapphire technology is an attractive candidate for millimeter-wave power amplifier applications with simultaneous high efficiency and power density.**

***Index Terms*— Efficiency, gain, GaN-on-sapphire, high-electron-mobility transistor (HEMT), millimeter-wave, N-polar, *W*-band.**

I. Introduction

GaN-BASED high-electron-mobility transistors (HEMTs) have emerged as a leading technology for mm-wave power amplifier applications. While the traditional Ga-polar GaN (0001 orientation) utilizing AlGaN/GaN heterojunctions have shown good performance in *W*-band [1], [2], its performance has saturated in part due to the dc-RF dispersion caused by the trapping effect and limits on device gate-to-channel distance because of the required AlGaN barrier thickness. As an alternative, the N-polar (000-1) GaN technology has shown a significantly higher 94 GHz power density than Ga-polar devices. N-polar devices have shown the highest combined output power density and efficiency at 94 GHz [4], [5], [6] and have shown good linearity [7] by using the unique advantages enabled by the reversed polarization field. Those benefits include the charge-inducing AlGaN back-barrier that can maintain charge density independent of gate-to-channel distance and the unintentionally doped (UID) GaN cap layer, which can enhance the conductivity of the access regions and provide good dc-RF dispersion control simultaneously [3], [4].

Implementing these advantages into device designs, the N-polar GaN deep-recess HEMTs have demonstrated a record power density of 8.85 W/mm with associated power-added efficiency (PAE) of 27% [5] and high PAE of 33.8% with associated 6.2 W/mm power density [6] at 94 GHz. However, GaN-based RF transistors would still benefit significantly from higher gain to further improve the device performance at mm-wave frequencies, especially at *W*-band and higher. Simultaneously, low-cost solutions can drive widespread market adoption.

GaN-on-sapphire is a very attractive RF electronics platform that builds upon a wider ecosystem. The availability of low-cost, large-area sapphire substrates has driven the ubiquity of GaN-based LEDs and vice versa. GaN-on-sapphire is also used in power-switching electronics, including a recent demonstration extending lateral GaN power-switching devices to 1200 V [8]. For mm-wave electronics, N-polar has already shown a good *W*-band power density of 5.1 W/mm at 14 V bias [9], but the low small-signal gain under power-matched conditions of 6 dB limited the power-added efficiency to 22.3%.

In this work, optimizations have been proposed and implemented on both HEMT epitaxy and device fabrication compared to previous N-polar GaN deep-recess HEMTs works to increase the gain and efficiency of the transistors.

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The fabricated devices demonstrated record high gain at 94 GHz with high efficiency and high output power. With the fabricated state-of-art device, this work also evaluated the device's S-parameters and large signal performance at different passivation stages to check the impact of passivation on device gain. These results demonstrate the great potential of N-polar GaN-on-sapphire for mm-wave frequency transistors application with high performance and lower cost.

II. HEMT Design

The N-polar GaN deep-recess HEMT is proven to be well suited for mm-wave frequency application with advantages provided by the natural back-barrier and UID GaN cap layer enabled by the N-polar GaN orientation. Because of the charge-inducing barrier below the GaN channel, N-polar GaN HEMT gets a built-in back-barrier. This natural back-barrier can provide 2-dimensional electron gas (2DEG) confinement from the back and maintains charge density independent of gate-to-channel distance, which is beneficial for achieving low contact resistance and helps N-polar GaN HEMT vertical scaling.

For the UID GaN cap layer, as shown in the band diagram (Fig. 1), the introduction of GaN cap reduces the vertical electric field in the GaN channel which causes the 2DEG charge density to increase and the centroid of 2DEG to move further away from the back-barrier which improves the mobility. Together, these boost the conductivity in the channel in the access region, reducing the on-resistance. The introduction of the GaN cap layer on the top also replaces the typical ex-situ SiN passivation in Ga-polar devices with an in-situ epitaxially grown GaN cap, providing excellent dispersion control. This is sometimes [5], [6] also augmented by an additional thin ex-situ SiN passivation for environmental protection and improved dispersion control for higher voltage operation. Here, the performance was characterized before and after thin SiN passivation was deposited.

Previous N-polar GaN deep-recess HEMT used a 47.5 nm [4], [6] GaN cap layer in the device design and demonstrated great power performance at W-band. The use of that thick GaN cap layer with the slanted gate recess sidewall and additional SiN passivation provided very good dc-RF dispersion control, but the dielectric loading also adds extra gate capacitance and lowers the device gain. Moreover, the E-beam evaporated Cr/Au gate metallization had problems with narrow gate trench filling when the device gate length was smaller than around 60 nm [6], limiting the ability to increase gain and efficiency by reducing the gate length.

To improve the device gain, a thinner UID-GaN cap layer and a SiN passivation layer were used here, and the gate metallization process was optimized for a more highly scaled device geometry [6].

A. Epitaxy Growth

The N-polar GaN HEMT sample reported in this article was grown as a 100 mm wafer on a commercial metal-organic chemical vapor deposition (MOCVD) platform at Transphorm on a 635 μm-thick miscut sapphire substrate [10], [11]. The

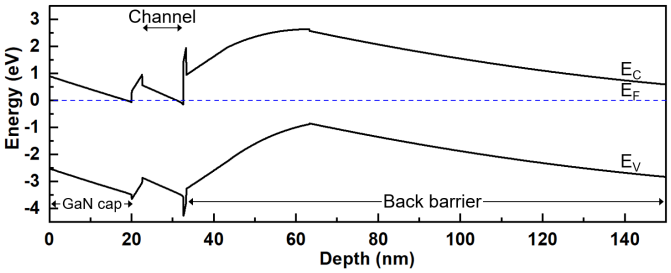

Fig. 1. Electron band diagram of the N-polar GaN deep-recess HEMT with a thin 20 nm GaN cap.

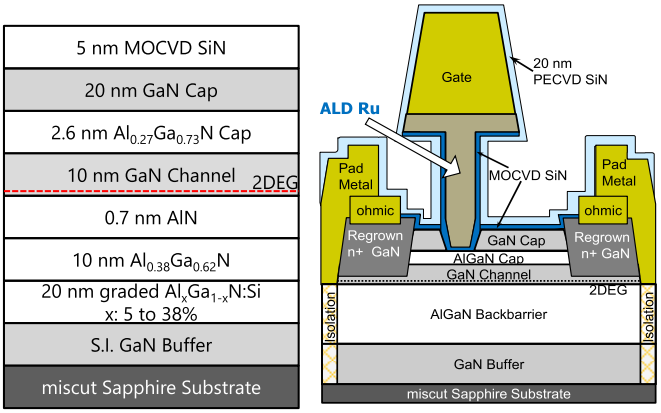

Fig. 2. Epitaxy layer structure of the reported N-polar GaN deep-recess HEMT. Cross-section schematic of the reported device.

sample epitaxial structure is shown in Fig. 2(a). The layer structure consists of, from bottom to top, a semi-insulating GaN buffer, a 20 nm graded and Si-doped AlGaN back-barrier with a 10 nm $Al_{0.38}Ga_{0.62}N$ spacer, a 0.7 nm aluminum nitride (AlN) interlayer, a 10 nm GaN channel, a 2.6 nm $Al_{0.27}Ga_{0.73}N$ cap layer, a thin 20 nm GaN cap layer, and a 5 nm in-situ MOCVD SiN film for the protection of the sample surface.

Compared with previous N-polar deep-recess devices [3], [4], several modifications in the epitaxy layer have been made to improve device gain. First, the GaN cap thickness was reduced to 20 nm to lower the fringing capacitance [12] while still maintaining the high access region channel conductivity and good dispersion control. Second, the GaN-on-sapphire epi used in this work provides exceptional electron mobility in the GaN channel. Using the TLM and capacitance–voltage (CV) measurements, the GaN-capped access region shows a low sheet resistance of 245 Ω/sq with 2DEG mobility being close to 2000 $cm^2/(V{\cdot}s)$, which is important for achieving a high gain. Lastly, the GaN channel thickness was also adjusted from conventional 12 to 10 nm for a smaller gate-to-channel distance which is important to obtain electrostatic control for scaled gate lengths.

B. Device Fabrication and Details

The device fabrication replaces the E-beam evaporated Cr/Au gate with the atomic layer deposition (ALD) ruthenium (Ru) gate metallization [6]. After the completion of 5 nm MOCVD SiN gate dielectric deposition, the sample is loaded into the ALD chamber for the deposition of Ru. Then, after

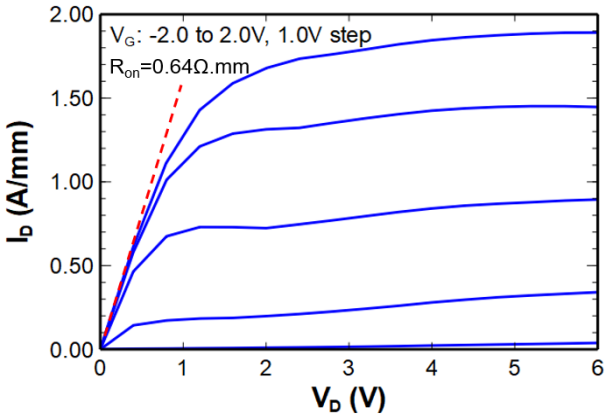

Fig. 3. Device DC output performance with V_{GS} from −2 to 2 V.

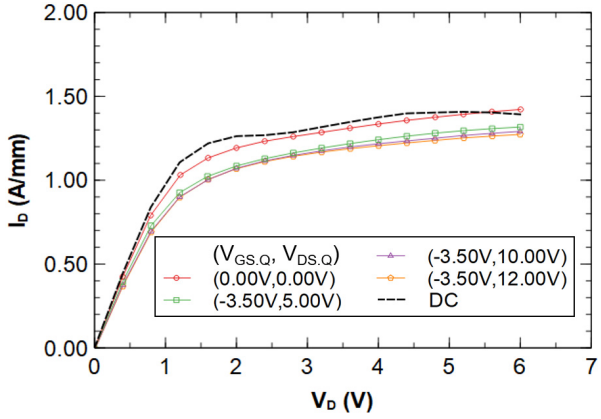

Fig. 4. DC curve and pulsed *I–V* measurements of V_{GS} = 1 V with 650 ns pulsewidth and 0.065% duty cycle under $V_{GS,Q}$ = –3.5 V and $V_{DS,Q}$ up to 14 V.

the definition of the top gate using similar electron beam lithography (EBL) and *E*-beam evaporation in [4], the ALD deposited Ru outside the gate trench was removed by etching. The rest of the device fabrication follows the self-aligned process flow as described in [4]. The ALD Ru gate process is incorporated to support narrow gate stem filling and reduce gate resistance of highly scaled T-gate [6].

For the final passivation, a thin 20 nm plasma enhanced chemical vapor deposition (PECVD) SiN passivation was deposited to passivate the sample surface and reduce the impact on fringe capacitance instead of the previous 40 nm SiN passivation. The fabricated device structure is shown in Fig. 2(b). Using *CV* measurements, the equivalent oxide thickness is extracted to be 15 nm with a dielectric constant normalized to GaN.

All device measurements were performed on-wafer with the full-thickness sapphire substrate with coplanar waveguide probe pads. All devices feature a 2 × 25 μm gate width with a 24 μm gate pitch, a 57 nm L_G (defined as the physical dimension of the base of the GaN cap recess), a 75 nm gate-to-source spacing (L_{GS}), and 420 nm source to drain spacing (L_{SD}). The contact resistance is measured to be 0.18 Ω·mm from probe pad metal to 2DEG.

III. Results and Discussion

To evaluate the device performance at different passivation stages and check the impact of 20 nm SiN passivation on device gain, the small-signal S-parameter measurement and *W*-band large-signal load–pull measurement have been taken both before and after SiN passivation.

A. Devices DC and Breakdown Performance

The dc characteristics of the device are shown in Fig. 3. The peak extrinsic transconductance (g_m) was measured to be 700 mS/mm at a V_D of 3 V with a subthreshold swing of 110 mV/dec. The device shows a high current density (I_D) of 1.86 A/mm at 5 V V_D and 2 V V_G. A low on-resistance of 0.64 Ω·mm was measured at 2 V V_G. The excellent dc performance is attributed to the high mobility in the device channel and device scaling.

The breakdown voltage, measured on a separate test device with 1 × 25 μm gate width and the same nominal dimensions (L_G, L_{GS}, and L_{SD}) after SiN passivation, was 42 V at 1 mA/mm I_D using a constant drain current injection method described in [13].

B. Pulsed IV Results

To check the dc-RF dispersion of the fabricated N-polar GaN-on-sapphire metal–insulator–semiconductor (MIS) HEMT with SiN passivation, dual-pulsed *I–V* measurements with a 650 ns pulsewidth and 0.065% duty cycle were conducted on the device. The device was biased in pinch off ($V_{GS,Q} = -3.5$ V) and a $V_{DS,Q}$ up to 12 V. As shown in Fig. 4, the dc-RF dispersion was low with a small deviation (less than 11%) from the dc measurement. This shows the effectiveness of the dispersion control provided by the 20 nm GaN cap layer and a 20 nm PECVD SiN passivation layer.

C. Small-Signal Performance

The bias-dependent S-parameters were measured from 250 MHz to 67 GHz and calibrated using line-reflect-reflect-match (LRRM) on a separate impedance standard substrate. On-wafer open and short structures were used for de-embedding the probe pad. The peak oscillation frequency f_{max} and current-gain cut-off frequency f_T were extrapolated using a 20 dB/decade fitting line on $|h_{21}|^2$ and unilateral gain.

As shown in Fig. 5(a) and (b), the S-parameter measurements on the un-passivated device show a high f_{MAX} of 306 GHz with a corresponding f_T of 122 GHz (10 V V_D, 485 mA/mm I_D) and a peak f_T of 132 GHz with a corresponding f_{MAX} of 286 GHz (V_D = 5.9 V, I_D = 677 mA/mm) as shown in Fig. 5(a) and (b). After 20 nm SiN passivation, the devices demonstrated an f_{MAX} value of 291 GHz with a corresponding f_T value of 109 GHz (V_D = 10 V, I_D = 647 mA/mm). The peak f_T of the device after passivation is measured to be 115 GHz with a corresponding f_{MAX} of 269 GHz (V_D = 6 V, I_D = 565 mA/mm) as shown in Fig. 6(a) and (b). The reduction in f_T and f_{MAX} after SiN passivation is attributed to the gate capacitance with increased gate–source capacitance (C_{gs}) being the major factor [9] and

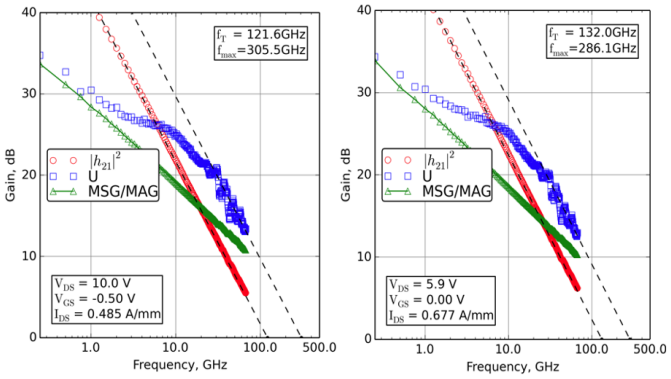

Fig. 5. Small-signal RF performance of the un-passivated device.

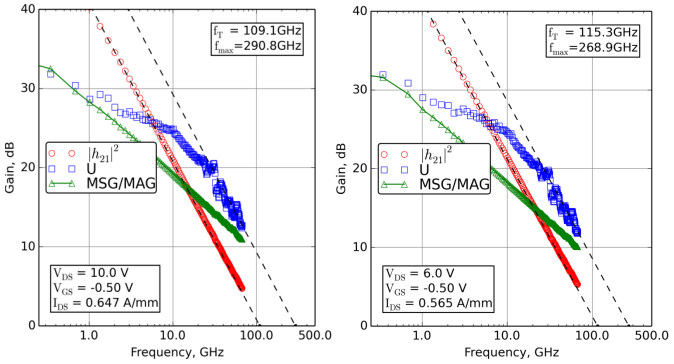

Fig. 6. Small-signal RF performance of the passivated device.

C_{gs} extracted from small-signal equivalent circuit analysis shows a 3.5 f_F increase after the addition of the 20 nm SiN passivation.

D. 94 GHz Large-Signal Performance

To evaluate the device power gain at W-band and check the impact of SiN passivation on device power performance, uncooled passive continuous-wave (CW) large-signal load–pull measurement [14] was performed at 94 GHz both before and after SiN passivation with careful load–pull system calibration as described in [14].

The device was biased in class AB condition at a lower quiescent drain current ($I_{DS,Q}$) of 260 mA/mm to maximize PAE when compared with previous N-polar GaN HEMTs works [4], [5], [6]. For the un-passivated device, the large signal performance at 94 GHz for $V_{DS,Q}$ of 8 and 12 V are presented in Fig. 7(a) and (b). Fig. 7(a) shows that at 8 V V_D, a high PAE of 44% was measured with an associated saturated output power, P_o of 2.6 W/mm. Increasing the V_D to 12 V, as shown in Fig. 7(b), a peak PAE of 42% with an associated output power density of 4.4 W/mm was measured on the device. This remarkable high-efficiency performance is attributed to the record 9.64 dB gain achieved on the devices.

After the SiN passivation, the load–pull power sweeps at 94 GHz for $V_{DS,Q}$ of 12 and 14 V are presented in Fig. 8(a) and (b), respectively. As shown in Fig. 8(a), the fabricated device demonstrates a peak PAE of 40.2% with an associated output power P_o of 4.85 W/mm at 12 V V_D. Increasing the V_D to 14 V, as shown in Fig. 8(b), a peak

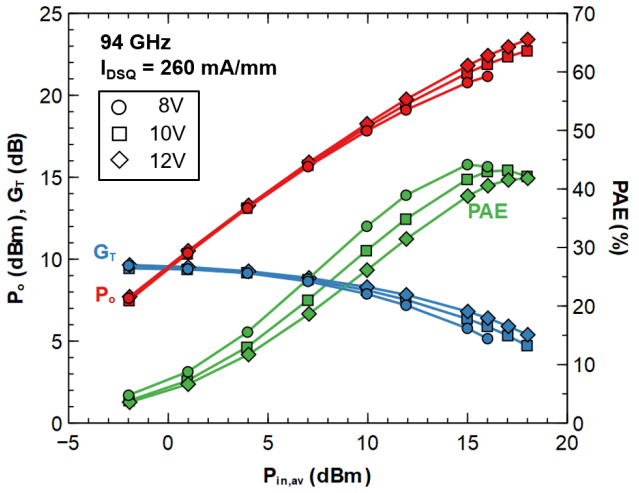

Fig. 7. 94 GHz load–pull power measurements at 260 mA/mm with 8, 10, and 12 V, at 8 V a peak PAE of 44% was measured with associated 2.6 W/mm output power density. At 12 V, the peak P_o of 4.4 W/mm was measured with an associated 42% PAE.

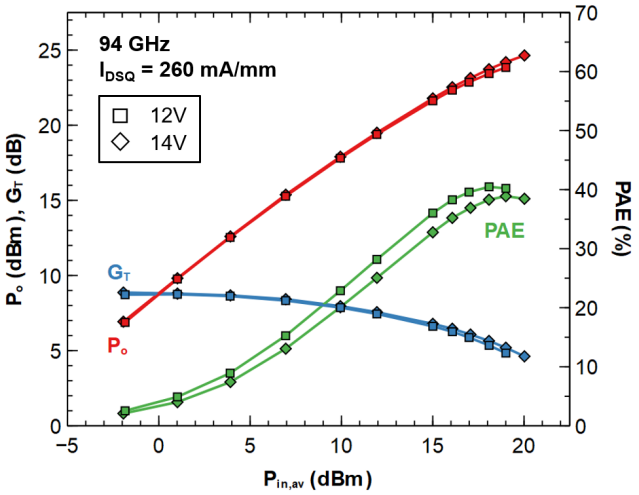

Fig. 8. 94 GHz load–pull power measurements at 12 V with 260 mA/mm $I_{DS,Q}$ demonstrating >40% PAE and 4.85 W/mm associated P_{out} and at 14 V with 260 mA/mm $I_{DS,Q}$ demonstrating 5.83 W/mm P_{out} with associated 38.5% PAE.

PAE of 38.5% with an associated output power density of 5.83 W/mm is achieved at this bias. A maximum total output power of 24.6 dBm (291 mW) is achieved on this N-polar GaN-on-sapphire deep-recess device. Both source and load impedance were limited by the available tuning range of the passive load–pull system. The key results of the 94 GHz load–pull measurement are summarized in Table I.

The Cripps power amplifier analysis method [15] has been used to validate the power and drain efficiency at saturation, under the assumption of a second harmonic short at the device output. Using the knee voltage and current of 1.8 V V_{knee} and 1.75 A/mm I_{knee} for V_{DD} = 12 V and V_{GS} = 2 V from the pulsed I–V and the quiescent current density of 260 mA/mm, the calculated drain efficiency and P_o are 60% and 4.75 W/mm as shown in Fig. 9, which fit the measured passivated device data very well.

TABLE I
SUMMARY OF 94 GHz LARGE SIGNAL RESULTS

	$V_{DS,Q}$ (V)	Γ_{load}	$G_{T,max}$ (dB)	Peak *PAE* P_o (W/mm)	*PAE* (%)	*DE* (%)	G_T (dB)
w/o SiN	8	-0.23+0.56j	9.6	2.61	43.8	63.0	5.2
	10	-0.15+0.60j	9.4	3.73	42.1	63.5	4.7
	12	-0.07+0.62j	9.7	4.38	41.8	58.8	5.4
w/ SiN	12	-0.15+0.60j	8.7	4.85	40.2	59.9	4.8
	14	-0.07+0.62j	8.9	5.83	38.5	58.7	4.6

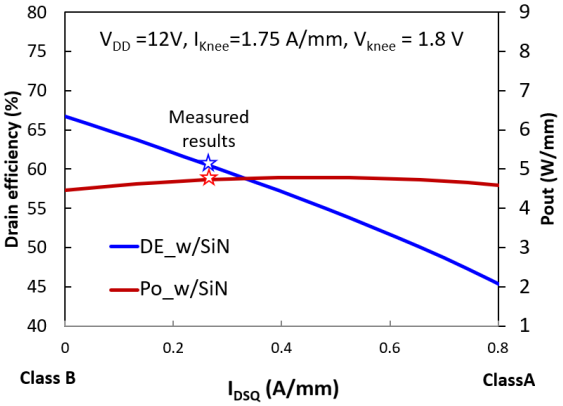

Fig. 9. Calculated output power density and drain efficiency as a function of quiescent current density and class of operation.

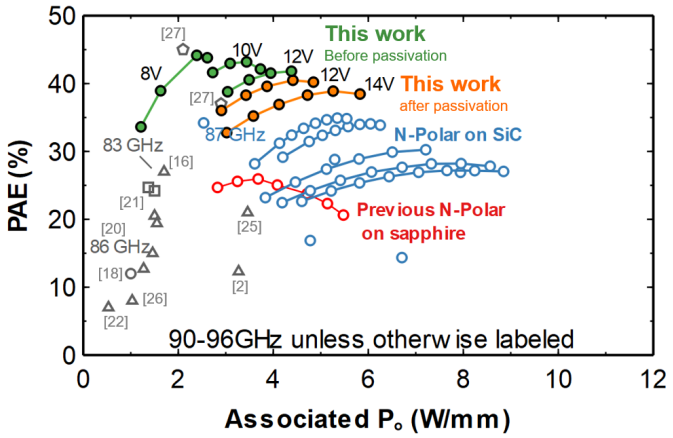

Fig. 10. Benchmark plot of PAE-P_o for this work relative to prior N-polar GaN-on-sapphire and GaN-on-SiC results as well as Ga-polar devices and MMICs from literature.

To compare the device results with those reported in the literature, the benchmark plots about 94 GHz large signal results are shown in Fig. 10 with our previous works on N-polar GaN-on-sapphire devices [9] and N-polar GaN-on-SiC devices [3], [4], [5], [6], [7] along with Ga-polar devices and MMICs [2], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27]. The N-polar GaN-on-sapphire deep-recess HEMT reported in this work shows a great PAE improvement over previous N-polar GaN-on-sapphire [9] and GaN-on-SiC [3], [4], [5], [6], [7] HEMTs, as well as Ga-polar device and MMICs, which is attributed to the high gain achieved in this device while simultaneously capable of delivering high power density. Furthermore, this device also

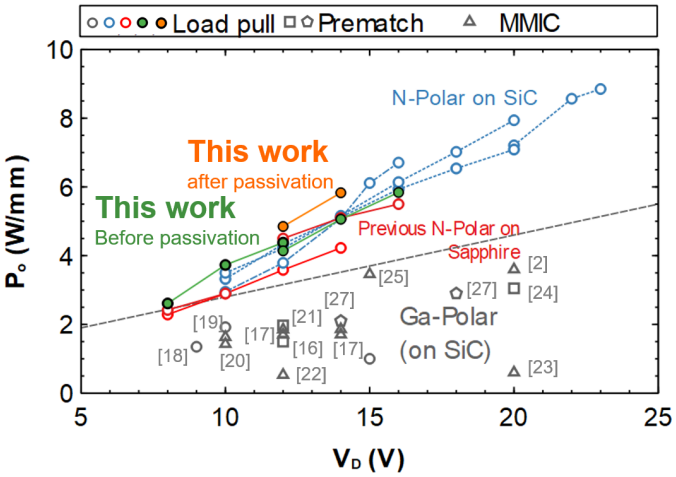

Fig. 11. Comparison of *W*-band P_o at a given V_D for this work relative to prior N-polar GaN-on-sapphire and GaN-on-SiC results as well as Ga-polar literature. From 8 to 12 V V_D, this device shows comparable or slightly higher performance relative to previous N-polar GaN-on-SiC.

achieved very high output power density while using sapphire as the substrate. The fact that this excellent performance is achieved with the sapphire substrate is encouraging, suggesting the performance of the device is still limited by gain instead of the thermal conductivity of the substrate for the given device size for the bias conditions explored. This statement is corroborated in Fig. 11 where *t* is the performance of the N-polar GaN-on-sapphire device in this work is comparable to or slightly higher power performance as those observed on N-polar GaN-on-SiC for the bias range considered.

The device after SiN passivation shows around 0.8 dB loss of linear gain at 94 GHz, which is attributed to the introduction of fringing capacitance. The impact on the gain from 20 nm SiN might be enlarged because of the highly scaled device structure with narrow spacing between the gate and the source. The high efficiency with a high output power of the un-passivated device also shows that ex-situ SiN passivation is not always required for N-polar deep-recess devices.

After the 20 nm SiN passivation, as shown in Fig. 11, the device shows a higher effective RF current at the same V_D bias when compared with the un-passivated device, showing that the SiN passivation on top of the GaN cap improves the dispersion control at these higher V_D values. The drop in efficiency with higher quiescent V_D bias is still under investigation. The possible reasons are increased dispersion at higher V_D or a drop in performance from self-heating as the power dissipation increases at higher V_D. The thermal effect with sapphire substrate might start to limit the device performance at high V_D with high output power.

Such exceptional performance validates the design and processing of the fabricated device. It also shows that high device gain, which in turn enhances efficiency, is a major tool to achieve exceptionally high performance from GaN-based RF transistors on a less thermally conductive (than SiC) substrate. And for higher power dissipation density applications, higher thermal conductivity SiC substrates [4], [5], [6], [7] and

diamond heat sinks on sapphire and SiC [28] can be used, enabling a technology choice based on application.

IV. Conclusion

Over 40% PAE with high output power density at 94 GHz has been demonstrated with N-polar GaN-on-sapphire deep-recess devices. Due to the excellent 9.65 dB linear gain at 94 GHz at a low 260 mA/mm current density bias, the reported N-polar GaN-on-sapphire HEMTs shows a very high PAE of 42% with associated 4.4 W/mm output power density at 94 GHz. The highest PAE measured on the device is 44% with 2.6 W/mm associated output power density. After SiN passivation, the fabricated N-polar GaN-on-sapphire HEMTs show a very high output power density of 5.83 W/mm with a record 38.5% PAE at 94 GHz. To increase the device gain, a 20 nm GaN cap layer and ALD Ru gate metallization have been implemented with the high channel mobility provided by high-quality N-polar GaN-on-sapphire epi provided by Transphorm Inc. The deep-recess structure obtains good dc-RF dispersion control with the thin GaN cap and PECVD SiN passivation. This work shows the great potential of sapphire for mm-wave GaN power amplifier application as a low-cost substrate.

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