Self-Organized Germanium Quantum Dots/Si_3N_4 Enabling Monolithic Integration of Top Si_3N_4-Waveguided Microdisk Light Emitters and p-i-n Photodetectors for On-Chip Sensing

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***Abstract*—Using a coordinated combination of lithographic patterning and self-assembled growth, Ge spherical quantum dots (QDs) were controllably generated within host layers of Si_3N_4 as active medium for Si photonics. A significant fabrication advantage of our approach is the high-temperature thermal stability of Ge QDs that are formed by thermal oxidation of poly-SiGe lithographically patterned structures at 800 °C–900 °C, offering flexibility in the waveguide (WG)-material choices, co-design, and integration of Ge photonic devices. Our Ge QDs enable monolithic integration of microdisk light emitters and p-i-n photodetectors (PDs) with top-Si_3N_4 WG-coupled structures using standard Si processing. Low dark current of 0.3 mA/cm^2 at 300 K and 0.2 μA/cm^2 at 77 K in combination with 3-dB frequency of 12 GHz for Ge-QD PDs and low threshold power of 0.6 kW/cm^2 for optically pumped Ge QD/SiN microdisks light emission evidence the high degree of crystallinity of our Ge QDs being an effective building block for 3-D SiN photonic integrated circuits.**

***Index Terms*—Ge, microdisks, photodiodes (PDs), quantum dot (QD), top-Si_3N_4 waveguides (WGs).**

I. Introduction

THE holy grail for Si photonic integrated circuits (PICs) is to achieve seamless, monolithic integration with CMOS electronics using robust Si processing technology, realizing on-chip optical interconnects for improving power consumption and latency as well as expanding the versatility and functionality for on-chip sensing [1], [2], [3]. The major technical challenges for practical realization of monolithic Si-based electronic-PICs lie in three aspects at least. First, the difficulty in growing sufficiently thick, high-quality Ge films on top of Si layers for light absorption and emission applications due to the large lattice mismatch (4.2%) between Ge and Si. Bottom Si-waveguided Ge lasers [4] and photodiodes (PDs) [5] have been experimentally demonstrated on 2-D silicon-on-insulator (SOI) platforms using exquisite epitaxy techniques in combination with strain engineering. However, low thermal budgets are required for subsequent fabrication processes so as to prevent the generation of detrimental generation–recombination centers resulting from lattice relaxation and to minimize fast Si–Ge interdiffusion, setting limitations on the flexibility and versatility of Si PIC applications [6]. Hence, the high threshold for Ge lasing and the large dark current of Ge PDs remain as challenging problems to be solved. Second, Si waveguides (WGs) are opaque in the visible band and suffer strong optical nonlinearity due to two-photon absorption in the infrared (IR) band, resulting in large propagation loss and poor optical-electrical conversion efficiency, respectively [7]. Third, the need of epitaxially growing Ge over Si layers results in bottom-WG-coupled structures, allowing only 2-D planar integration of Si PICs.

To complement and even outperform in materials characteristics and device performance to Si WGs, silicon nitride (SiN) WGs have gained spotlight because of their optical transparency properties over broadbands ranging from the IR to the visible spectrum. The fabrication feasibility of "stacking" SiN WGs using chemical-vapor deposition (CVD) processes, in particular, offers great promise for realizing 3-D PICs, advanced on-chip optical interconnects, and on-chip sensing applications [7]. However, it is a formidable task to epitaxially grow single-crystalline Ge films over bottom SiN WGs that are nominally amorphous. Top-Si_3N_4 WGs stacking over Ge films have been experimentally fabricated using low-temperature (~300 °C) plasma-enhanced CVD processes; however, a subsequent long-duration, high-temperature (>900 °C for at least hours) densification step [8] is generally required to drive

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out the excess hydrogen incorporated within the as-deposited Si_3N_4:H films so as to reduce the absorption loss. The key problem with such a high thermal-budget densification process is that the underlying Ge film is prone to crystalline defect formation due to lattice-strain relaxation at high temperatures, degrading the performance of photonic active devices [9], [10]. Hence, high photoresponsivity, low dark-current Ge PDs as well as high-efficiency, low threshold Ge light sources remain to be demonstrated on SiN-based integrated photonics platforms.

In contrast to the nature of the indirect bandgap transition in bulk Ge, low-dimensional Ge nanostructures allow direct bandgap luminescence and enhance light emission/absorption properties based on quantum confinement effects [11]. Localized carrier confinement and strong overlap of electron–hole wave functions, in particular, within small-sized quantum dots (QDs) greatly increase the oscillator strength for optical transitions to occur within an otherwise indirect bandgap semiconductor (such as Si or Ge) and, consequently, relax the k-conservation rule for direct bandgap emission in bulk materials [12]. Importantly, embedding QDs within resonant cavities further boosts the spontaneous emission rate based on quantum electrodynamics [13].

Our previous reports have already demonstrated a CMOS-compatible approach for the controllable growth of self-assembled Ge QDs embedding within CVD-Si_3N_4 layers in a self-organized manner [14], [15], [16], [17], [18], [19], [20], [21]. The key engineering advantages of our combined lithographically patterned and self-organized Ge QD/Si_3N_4 approaches lie in the high degree of scalability, uniformity, and reproducibility in the Ge QD size, allowing experimental demonstration of size-tunable photoluminescence (PL) peak wavelengths ranging from 350 to 1550 nm [20], [21], [22], [23]. Fabrication by thermal oxidation at 800 °C–900 °C, our self-organized Ge QD/Si_3N_4 systems also come with the inherent advantage of high-temperature thermal stability that has allowed monolithic integration of SiN bus-waveguided Ge QDs microdisk (μ-disk) light emitters and top-waveguided p-i-n PDs on top of SOI (Fig. 1) [24]. In this work, we reported detailed design and analysis of fabricated SiN/Si WGs, Ge QD light emitters, and Ge QD p-i-n PDs via extensive simulations and structural examinations.

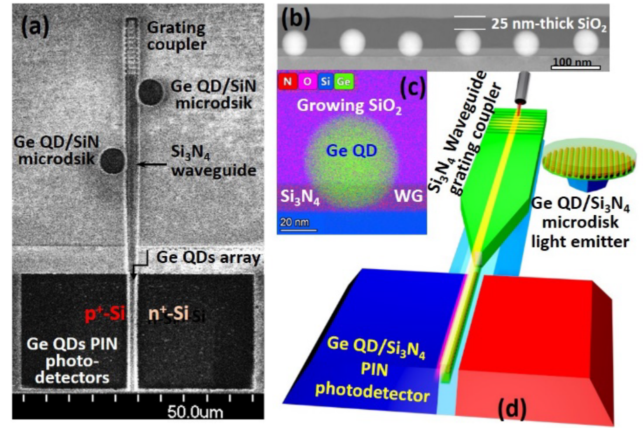

Fig. 1. (a) SEM, (b) TEM, and (c) EDS map micrographs. (d) Schematic showing monolithic integration of Si_3N_4 waveguided Ge QD/Si_3N_4 μ-disk light emitters and p-i-n photodetectors.

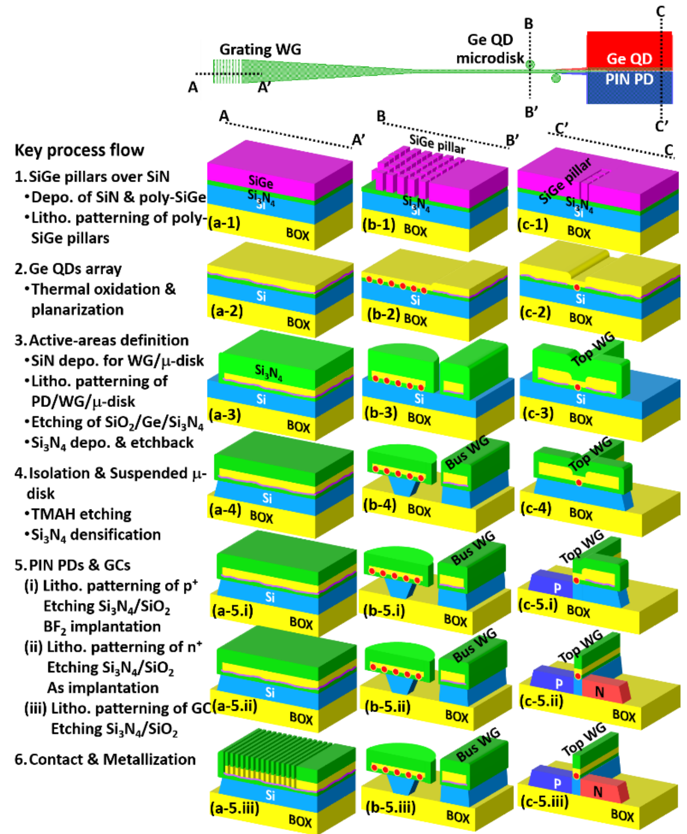

Fig. 2. Process flow and schematic diagrams of monolithic integration of SiN-waveguided Ge QDs/Si_3N_4 μ-disk light emitter and p-i-n PDs. (a) WGs/GCs, (b) Ge QD microdisk, and (c) Ge QD PIN PD. Key process modules for the integration including (1) poly-SiGe pillar array over SiN, (2) Ge QDs array, (3) Active-area definition for WG, m-disk, and PD, (4) Isolation of WG, m-disk, and PD using TMAH etching, and (5) p-i-n PDs and GCs.

II. Experiments

A. Formation of Ge QD Arrays

Fig. 2 shows our proposed process flow for monolithic integration of Si_3N_4-waveguided Ge QDs μ-disk light emitters and p-i-n PDs. Bilayers of 18-nm-thick Si_3N_4 and 60-nm-thick poly-$Si_{0.85}Ge_{0.15}$ were sequentially deposited using low-pressure CVD (LPCVD) on SOI substrates with 200-nm-thick, p-type (10^{13} cm^{-3}) top single-crystalline Si layers and 400-nm-thick buried oxide (BOX) layers. Arrays of poly-$Si_{0.85}Ge_{0.15}$ pillars with pillar width/spacing of 100/20 nm were lithographically patterned using electron-beam lithography (EBL) in combination with SF_6/C_4F_8 plasma etching [Fig. 2(a-1), (b-1), and (c-1)]. Areas of poly-SiGe pillar arrays for light emitters and PDs are 10 × 10 μm^2 and 0.12–2.4 × 50 μm^2, respectively. Next, thermal oxidation at 900 °C within an H_2O ambient preferentially converted the Si content of poly-SiGe pillars to capping layers of SiO_2. During the selective oxidation of poly-SiGe pillars, released Ge ultimately coalesces into a single Ge QD with a diameter of 50 nm per oxidized pillar. Following the formation of self-organized Ge QD/capping SiO_2 arrays, LPCVD-SiO_2 layers were deliberately deposited to fill in gaps between the oxidized pillars and then etched back for the planarization of Ge QD array

[Fig. 2(b-2) and (c-2)]. Ultimately, the thickness of the remaining SiO_2 layer over Ge QD arrays is 25 nm [Fig. 1(b)]. The resulting Ge QD arrays are readily applicable for the fabrication of Si_3N_4-embedded Ge-QD μ-disk light emitters and PDs.

B. Active-Areas Definition for μ-Disks, PDs, and WGs

A 280-nm-thick, LPCVD Si_3N_4 layer was deposited over the Ge QDs/SiO_2 array, forming the core materials of both μ-disks and WGs. Subsequently, the active areas of Si_3N_4-embedded Ge QDs μ-disks, Si_3N_4-embedded Ge QDs PDs, and Si_3N_4 bus WGs with linear taper evanescent-wave coupled to PDs [Fig. 2(a-3), (b-3), and (c-3)] were produced using EBL in combination with CHF_3-based two-step plasma etching processes. That is, the first-etching process of CHF_3/CH_4/Ar plasma removes 280-nm-thick Si_3N_4 and 75-nm-thick SiO_2 layers followed by the second-etching process of CHF_3 plasma etching away 12-nm-thick, condensed Ge and 18-nm-thick, buffer Si_3N_4 layers. Next, a 20-nm-thick Si_3N_4 layer was conformally deposited and then directly etched back using CHF_3 plasma to wrap all around the fabricated photonic devices.

C. Isolation and Formation of Cantilevered Kylix μ-Disks

Following the production of active areas for μ-disks, PDs, and WGs, the Si layer in-between devices was removed by dipping in 2.38% tetramethyl ammonium hydroxide (TMAH, $C_4H_{13}NO$) solution at 75 °C for few minutes since TMAH etching on Si has high etching selectivity to SiO_2 and Si_3N_4 and has high compatibility with the CMOS fabrication processes [25]. Concurrent with the device isolation [Fig. 2(a-4), (b-4), and (c-4)], the underlying Si layers of fabricated devices were partially etched within the SOI substrates as a result of TMAH anisotropic etching, thus, particularly forming Si pedestals supporting the cantilevered Kylix (upward-bending) μ-disks [Fig. 2(b-4)] A postanneal process at 900 °C for 30 min densified Si_3N_4 in terms of a reduction in thickness from 280 nm of as-deposited Si_3N_4 to 230 nm of densified Si_3N_4 layers.

D. Formation of p-i-n Implantation and Grating Coupler

Sequential lithographic-patterning and plasma etching processes are combined with ion implantation of BF_2 (5×10^{15} cm^{-2} and 30 keV) and As (3×10^{15} cm^{-2} and 30 keV) generating the p^+- and n^+-regions, respectively, required for p-i-n PD construction [Fig. 2(c-5.i) and (2c-5.ii)]. Subsequently, rapid-thermal annealing (RTA) at 900 °C for 30 s activated the implanted dopants, forming the adjacent p^+-Si and n^+-Si regions that are self-aligned with the Ge QD/Si_3N_4/Si heterostructure. Next, grating-couplers (GCs) at the input terminal of Si_3N_4 WGs were lithographically patterned and etched using CHF_3/CH_4/Ar plasma [Fig. 2(a-5.3)]. Finally, contact and metallization processes completed the device fabrication.

III. Results and Discussion

A. Ge QD p-i-n Photodetectors

Cross-sectional transmission-electron microscopy (TEM) micrograph [Fig. 3(a)] shows that during the thermal oxidation

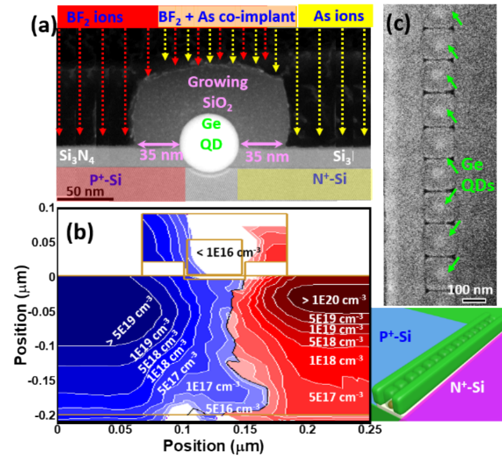

Fig. 3. (a) Schematic and TEM micrograph showing sequential lithography in combination with BF_2 and As ion implantation processes for forming self-aligned p^+-Si/Ge QD/n^+-Si PDs. (b) Calculated dopant profiles of BF_2 and As ions following RTA at 900 °C for 30 s. (c) 120-nm-wide Ge-QDs array.

process for forming Ge QDs, our Ge QDs are indeed able to decompose the solid layer of buffer Si_3N_4, migrate through the entire layer of Si_3N_4, and ultimately get in touch with the Si layer in the solid state. Concurrent with the QD penetration, a ~2-nm-thick, conformal shell of SiO_2 is simultaneously formed and separates the penetrating Ge QD from surrounding layers of Si_3N_4 and Si. Our extensive TEM and energy dispersive X-ray spectroscopy (EDS) observations have already elucidated the fundamental mechanisms responsible for the Ge QD migration within the Si-containing layers as well as the formation of the SiO_2 shell surrounding the penetrating Ge QD [16], [18]. In addition, our as-formed Ge QD comes automatically embedded within a 75-nm-thick and 120-nm-wide thermally grown layer of SiO_2 by virtue of the selective oxidation of the Si content of the original poly-SiGe pillar as shown in Fig. 3(a). The growing SiO_2 layer encapsulating Ge QDs not only provides passivation but also serves as inherent hard masks for enduring the subsequent co-ion implantation of BF_2 and As, respectively, for forming p^+-Si and n^+-Si regions adjacent to the Ge QDs array.

Calculated doping profiles of BF_2 and As using TCAD simulation [Fig. 3(b)] show that following a subsequent RTA process, p^+-Si and n^+-Si regions nearly self-align with the Ge QD array. Fig. 3(c) shows that an intrinsic Ge QD region as thin as 120 nm was produced due to the fabrication advantage of the growing SiO_2 layer being able to endure co-ion implantation of BF_2 and As. Our approach for fabricating Ge-QD p-i-n PDs eliminates the need of high-resolution EBL for controlling the overlay alignment and complicated chemical–mechanical polishing (CMP) processes required by Lische et al. [26], in which an extremely high overlayer accuracy of <10 nm and multiple CMP processes are required for producing a 100–120-nm Ge-fin laterally sandwiched between doped p^+-Si and n^+-Si regions as well as Si nano-WGs.

To directly gain insight on photosensitivity of our proposed Ge-QD PDs, we have also fabricated normal-incidence Ge-QD p-i-n PDs with no top SiN WGs. Fig. 4(a) and (b) shows

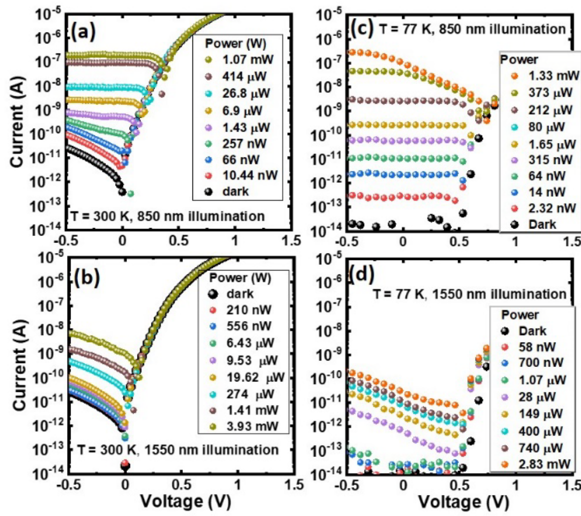

Fig. 4. *I–V* characteristics of Ge-QD p-i-n PDs with *L*/*W* of 0.12/50 μm measured in the dark and under (a) and (c) 850- as well as (b) and (d) 1550-nm illuminations at 300 and 77 K, respectively.

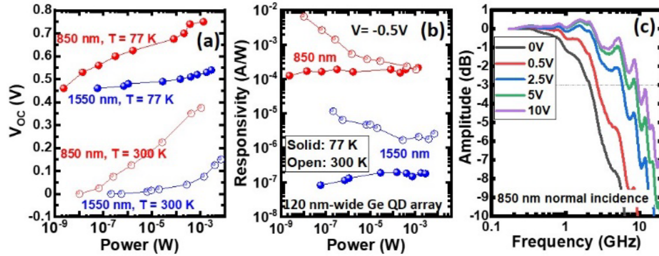

Fig. 5. Power-dependent (a) V_{OC} and (b) photoresponsivity of Ge-QD p-i-n PDs under 850- and 1550-nm illuminations at 300 and 77 K. (c) Frequency response under 850-nm illumination at 300 K.

that Ge-QD p-i-n PDs exhibit low dark current density of 0.3 mA/cm^2 at -0.5 V and 300 K, which is much lower than that of >10 mA/cm^2 for p-i-n PDs with Ge films grown by using either direct deposition [27] or selective-area heteroepitaxy [28]. Measured dark current density of our Ge-QD p-i-n PDs is comparable to that (0.25 mA/cm^2) of PDs with Ge films grown on top of 10-μm-thick SiGe compositionally graded buffer layers [29], which is unfortunately too thick to be integrated with Si-based electronic circuits. Another important finding of notes is that lowering temperature from 300 to 77 K results in a large reduction in dark current by three orders (<0.16 μA/cm^2 at 77 K in Fig. 4(c) and (d)) in magnitude. The fact of very low dark current of Ge-QD p-i-n PDs is a testament to high-degree crystalline quality in our Ge-QDs that are surrounded by a thin SiO_2 shell, suggesting the detectivity of our Ge-QD p-i-n PDs for sensing low-level illuminations.

It is clearly seen from Fig. 4 that normal incidence of 850- and 1550-nm illuminations produces considerable photocurrent accompanied by a positive shift in open-circuit voltage (V_{OC}), leading to a significant photocurrent gain at zero bias (0 V). It is important to note that lowering temperature increases V_{OC} from 0 to 0.4 V at 300 K to 0.4–0.7 V at 77 K [Fig. 5(a)] and enhances photocurrent linearity as evidenced by a wide dynamic range of

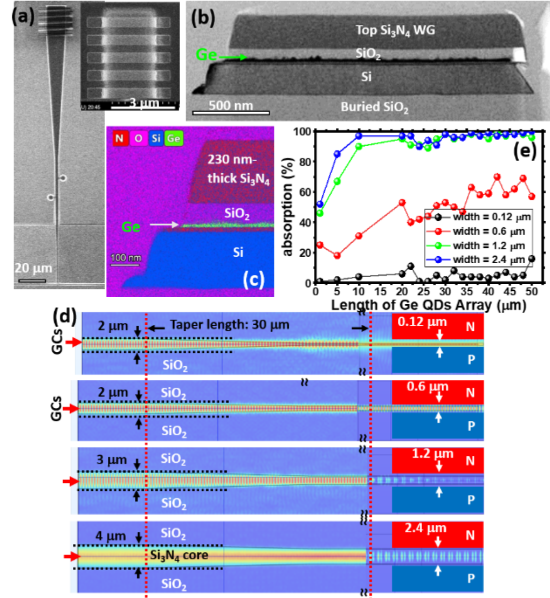

Fig. 6. (a) Plan-view SEM, (b) cross-sectional TEM, and (c) EDS mapping micrographs of top Si_3N_4 WGs with a GC and linear taper. (d) Simulated plan-view TE modes for Si_3N_4 WG/SiO_2 cladding with SiN thickness of 300 nm. (e) Absorption as a function of PD length from 0.12- to 2.4-μm-wide WGs evanescent-wave coupled to Ge-QD PDs.

photoresponsivity ($\Re = 0.2$ mA/W at 850 nm and 0.15 μA/W at 1550 nm) invariant with an incident optical power (P_{IN}) of 1 nW–10 mW at 77 K [Fig. 5(b)]. Not only dark current but also photocurrent is reduced in magnitude by lowering temperature from 300 to 77 K. This is because both generation–recombination processes and absorption coefficient [30] are reduced simultaneously at low temperatures, leading to an enhancement in photocurrent gain but a reduction in photoresponsivity. Dash and Newman [30] have reported that decreasing temperature from 300 to 77 K, absorption coefficient of bulk Ge at 1550 nm appears to have a large reduction from 320 to 7.0 cm^{-1}, whereas a slight decrease in absorption coefficient from 3160 to 2220 cm^{-1} is measured at 850 nm. 3-dB frequencies ($f_{3\,dB}$) of 2.2 and 12 GHz are achievable at zero bias and E-field of 10^5 V/cm, respectively [Fig. 5(c)].

B. Top SiN-Waveguides With Grating Coupler and Linear Taper

Fig. 6(a)–(c) shows the densified SiN top-WGs with thickness/width/length of 230 nm/2–4 μm/50–150 μm. GC of period/spacing = 1.1 μm/480 nm [Fig. 6(a)] in combination with linear WG taper (length of 30 μm and width changing from 4 to 0.12–2.4 μm) is fabricated to couple the light from optical fiber to GCs and couple the WG to Ge PDs, respectively [Fig. 6(d)]. It is clearly seen from EDS mapping micrograph in Fig. 6(c) that below the top SiN WGs, there are 75-nm-thick SiO_2 and 10-nm-thick condensed Ge layers generated by virtue of the thermal oxidation of 60-nm-thick poly-$Si_{0.85}Ge_{0.15}$ layer over 18-nm-thick buffer Si_3N_4 on top of SOI substrates with a 200-nm-thick Si layer. In this way, we demonstrated an evanescent-wave coupling structure for SiN/Ge/Si-waveguided Ge PDs [Fig. 1(a)].

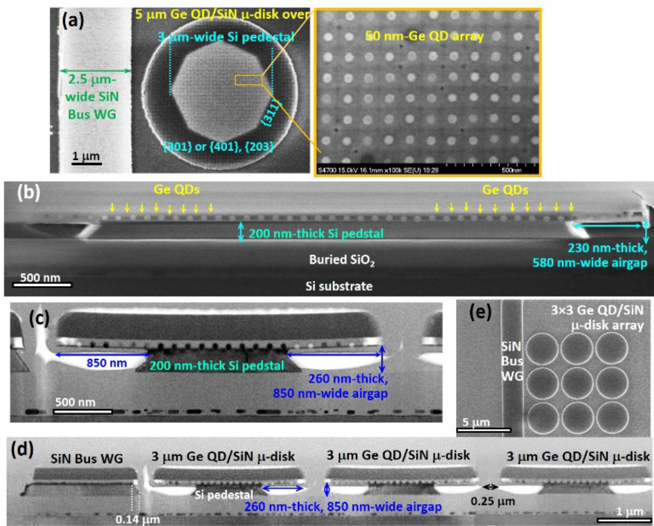

Fig. 7. (a) Plan-view and (b) and (c) cross-sectional SEM/TEM micrographs of a single 5-/3-μm Si_3N_4-embedded Ge-QD μ-disk with SiN bus-WG. (d) and (e) Cross-sectional/plan-view TEM/SEM micrographs of 3 × 3 Si_3N_4-embedded Ge-QD μ-disks array with SiN-bus WG.

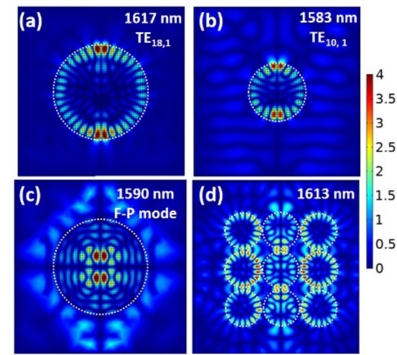

Fig. 8. Simulated TE modes for single Ge QDs/Si_3N_4 μ-disks with diameters of (a) and (c) 5 and (b) 3 μm, and for (d) array of 3 × 3 μ-disks with a diameter of 3 μm and interdisk spacing of 300 nm.

We analyzed transverse electric-field (TE) mode of fabricated SiO_2-wrapped SiN/Ge/Si WGs using commercially available, 3-D simulation software, COMSOL Multiphysics. Fig. 6(d) shows the plan-view, calculated E-field distribution along the WG taper with the width linearly changing from 4 to 2.4 μm, within which TE modes are well confined for 1550-nm light propagation. Our simulation also shows TE modes spreading to cladding SiO_2 when WGs become narrow (0.12–0.6 μm). Fig. 6(e) shows that over 95% absorption from WGs evanescent-wave coupled to Ge-QD PDs is achievable when the WG width (i.e., the absorption width of the Ge QD PDs) is larger than 1.2 μm and the PD length is longer than 10–20 μm.

C. Ge QD/Si_3N_4 μ-Disk Light Emitters

Our technique of Si_3N_4-embedded Ge QDs is readily applicable for the fabrication of Si_3N_4-embedded Ge-QD μ-disk light emitters integrated with bus WGs. μ-disk light sources enable in-plane photonic integration due to the fact that radiation from the strongly confined whispering-gallery cavity modes (WGMs) around the disk resonators allows easy coupling of emitted light with bus WGs.

Plan-view [Fig. 7(a)] and cross-sectional [Fig. 7(b)] scanning-electron microscopy (SEM) micrographs show a single cantilevered, Si_3N_4-encapsulated Ge QDs μ-disk with a diameter of 5 μm being supported over SOI substrates by multifaceted Si pedestals. The faceted Si pedestals [Fig. 7(a)] were produced by TMAH etching that has highly anisotropic etch rates exposing slower etching crystal planes of Si. TMAH etches the (100), (110), and (311) crystalline planes of Si much faster than the (111) planes, which form the residual facet habits. [31] The resulting Kylix (bent-up cup-like) μ-disk is partially released from the underlying SOI substrate with a 200–230-nm-thick and 580-nm-wide air gap [Fig. 7(b)]. The upward-bending periphery of the cantilevered μ-disk induces a tensile stress within the Si_3N_4-embedded Ge QDs. In this way, excited Ge QD luminescence is effectively confined within the high refractive-index contrast, Si_3N_4-embedded Ge QDs/SiO_2 μ-disk heterostructure ($\varepsilon_{\text{Ge QD}} = 4.3$, $\varepsilon_{\text{SiN}} = 2$, and $\varepsilon_{\text{silicon oxide}} = 1.46$) for ultimately achieving low-threshold luminescence.

We have also advanced the fabrication of bus-waveguided 3 × 3 μ-disks array with a disk diameter of 3 μm and interdisk spacing of 250 nm [Fig. 7(c)–(e)] to improve radiative transfer between neighboring disks. An important finding of notes from Fig. 7(c) is that the upward bending of disk periphery in 3 × 3 μ-disks array appears to be much enhanced in comparison to that of a single, isolating 5-μm-diameter μ-disk. This is because TMAH etching on Si is not only anisotropic but also has strong dependency on geometrical conditions of exposed Si patterns, such as size, morphology, and interspacing [32]. For instance, the extent (~580 nm) of Si undercut below a single 5-μm μ-disk [Fig. 7(b)] is reduced as compared to that (~850 nm) of Si undercut underneath 3-μm-diameter disk [Fig. 7(c)]. Such a pattern-dependency of TMAH etching on Si is further exemplified in the case of SiN bus WGs, below which very small Si undercut of 0.14 μm is produced [Fig. 7(d)] and primarily determined by the slow etch rate of (111) planes.

TEM observation shows the presence of air gaps in-between the bus WG and μ-disks [Fig. 7(d)], possibly originating from artifacts caused by TEM sample preparation and/or poor conformity of passivation oxide layers. We expect to eliminate air gaps by suitably adjusting process parameters for depositing passivation oxide layers in order to improve coupling efficiency between the bus WG and μ-disks.

Both diameters of μ-disks and Ge QDs are important parameters influencing the ultimate lasing threshold, number of cavity modes, resonance positions, and optical confinement. Optimal design for coupling light emission from the Ge QDs and resonant modes of the μ-disk optical cavities is essential for enhancing Q factors. We calculated TE profiles and polarized modes of cantilevered, 200-nm-thick Ge QDs/Si_3N_4 μ-disks with diameters of 5 and 3 μm. The circular distribution of TE spots suggests that the Ge QD/Si_3N_4 μ-disks operate in the WGM regime. It is clearly seen that photon leakage out of the 5-μm disks [Fig. 8(a)] is

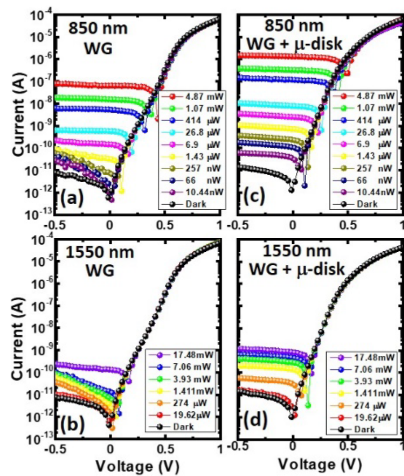

Fig. 9. *I–V* characteristics of Ge-QD p-i-n PDs with *L*/*W* of 2.4/50 μm measured at 300 K under illuminations at (a) and (c) 850 and (b) and (d) 1550 nm through 50-μm-long WGs/coupled to bus WG tapers that are in close proximity to Ge-QD μ-disks.

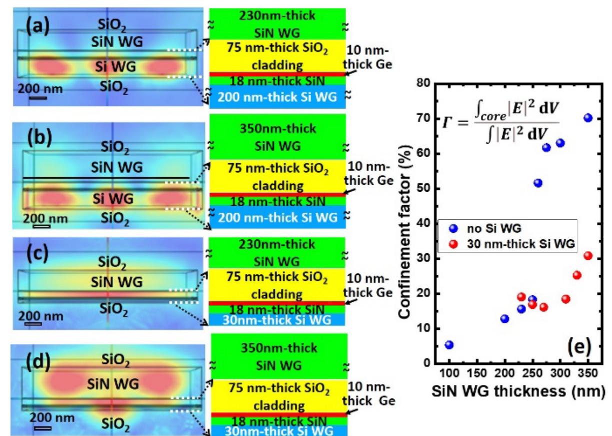

Fig. 10. Simulated cross-sectional TE profiles for (a) 230- and (b) 350-nm-thick Si_3N_4 WGs on top of 75-nm-thick SiO_2 cladding and 200-nm-thick Si WGs and (c) 230- and (d) 350-nm-thick Si_3N_4 WGs on top of 75-nm-thick SiO_2 cladding and 30-nm-thick Si WGs, showing thickness-dependent optical confinement of hybrid Si_3N_4/Si WGs. (e) Estimated confinement efficiency of composite WG structures of Si_3N_4/SiO_2 cladding/Ge/SiN/Si as a function of Si_3N_4 and Si thicknesses.

suppressed due to stronger optical confinement as compared to the case of 3-μm disks [Fig. 8(b)]. Within the 5-μm disks, however, not only the number of WGMs along the disk edge increases but also Fabry–Perot (FP) cavity modes in the center of disks become significant [Fig. 8(c)] due to the resonance formed by light propagation radially within the disk and reflection at the opposite edges of the disk. The 3-μm μ-disks indeed reduce the FP mode number due to their smaller sizes/mode volumes but have considerable radiative loss via evanescent fields spreading to regions outside the disks [Fig. 8(b)], degrading the *Q*-factors. To improve light confinement within 3-μm μ-disks, we have designed 3 × 3 μ-disks array with a disk diameter of 3 μm and interdisk spacing of 100–300 nm since a geometric configuration of μ-disk arrays [33], [34] has been proposed to facilitate near-field optical coupling and radiative transfer between neighboring μ-disks. Fig. 8(d) shows that the TE spots for all 3-μm-diameter μ-disks become brighter and more focused than that in a single μ-disk with 3 μm diameter, and in particular, the intensity of TE spots is much enhanced at the boundaries between disks due to strong interdisk coupling.

D. On-Chip Detection of SiN/Ge/Si WGs and Ge QD μ-Disk Light Emission

Our design allows on-chip detection of light emission from Ge-QD/SiN μ-disks and propagation loss within SiN/Ge/Si WGs using the integrated Ge-QD PDs [Fig. 1(a)]. Fig. 9(a) and (b) shows the typical *I–V* characteristics of waveguided Ge-QD p-i-n PDs with *L*/*W* of 2.4/50 μm under illumination at 850 and 1550 nm via 50-μm-long WGs.

In this work, studied WG lengths of 50–150 μm might be too short to ignore the coupling loss effect of GCs, leading to propagation loss being possibly overestimated. Estimated propagation losses of our WGs at 850 and 1550 nm are 512 and 38 dB/cm, respectively, which are relatively large in comparison to the values of 4.5–1.5 dB/cm for 1550-nm illumination in 10-μm-wide SiN WGs with a thickness of 250–500 nm reported by Melchiorri et al. [35]. This is because below top SiN WGs, there indeed comprises a 75-nm-thick SiO_2, 10-nm-thick Ge, 18-nm-thick buffer SiN, and 200-nm-thick Si layers on top of a 400-nm-thick BOX layer. Simulated cross-sectional optical TE modes distribution of the composite SiN/Ge/Si WG structures is shown in Fig. 10. It is clearly seen that most of the WG modes occur to the bottom, 200-nm-thick Si layers [Fig. 10(a) and (b)], whereas the optical field is confined within SiN and Ge/Si layers when the underlying Si layer is thinned to 30 nm in thickness [Fig. 10(c) and (d)]. A bottom Si layer and top SiN layers form a hybrid WG structure, in which the mode field could be engineered and primarily confined within top SiN WGs by increasing the thickness of top SiN layers greater than 300 nm and thinning the underlying Si layer [Fig. 10(e)]. Ultrathin Si-padded Si_3N_4 WGs consisting of a 30-nm-thick Si slab underneath a 220-nm-thick Si_3N_4 strip separated by a 200-nm-thick SiO_2 layer have been reported, demonstrating WG propagation loss of 0.055 dB/cm at 1310 nm [36]. Hong et al. [37] have reported thickness dependency on coupling efficiency of SiN GCs and observed that optimal coupling efficiency is achievable in the SiN thickness of 300–350 nm. Our simulation shows that optical confinement within the top SiN WG significantly improves when its thickness is greater than 300 nm, below which confinement efficiency drops because optical modes extend to regions outside SiN layers.

In fact, our Ge QD approach is essentially based on the thermal oxidation of poly-SiGe lithographically patterned structures on top of buffer SiN layers. Therefore, the thickness of the Si layer on top of SOI substrate could be reduced as thin as possible. We have already experimentally demonstrated that Ge QDs could be produced on top of 20-nm-thick Si layers on SOI substrates [18], [38]. Therefore, we expect to improve propagation loss in our SiN/Si WGs by increasing the SiN thickness from 230 to 350 nm, thinning the underlying Si

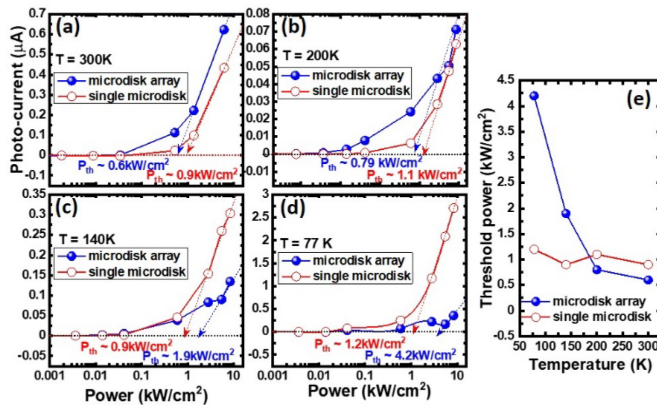

Fig. 11. Dependence of emission intensity in terms of photocurrent of Ge QD PDs versus optical pumping power showing thresholds for both single Ge-QD/SiN μ-disks and arrays of 3×3 Ge-QD/SiN μ-disks at $T =$ (a) 300, (b) 200, (c) 140, and (d) 77 K. (e) Temperature dependency of thresholds for light emission from single and arrays of 3×3 Ge-QD/SiN μ-disks.

layers to less than 30 nm, and increasing the BOX thickness to more than 2 μm.

Fig. 9(c) and (d) shows the photocurrent of Ge-QD p-i-n PDs coupled to bus WG tapers that are in close proximity to a single Ge-QD μ-disk and an array of 3×3 Ge-QD μ-disks under variable power 850 nm and 1550 illumination, respectively. Fig. 11(a) shows that at room temperature, threshold power densities of 0.6 and 0.9 kW/cm^2 for optically pumped light emission are achievable within an array of 3×3 Si_3N_4-embedded Ge-QD μ-disks and a single Si_3N_4-embedded Ge-QD μ-disk, respectively. Both of these threshold power values are lower (by 3–5 fold) than the 3-kW/cm^2 threshold power density required for optically pumped lasing in highly strained Ge nanowires [39]. Another important finding of notes is that threshold power densities for a single Ge-QD/SiN μ-disk are nearly invariant with temperature in the range of 77–300 K, whereas a large increase in threshold power densities was observed for an array of 3×3 Si_3N_4-embedded Ge-QD μ-disks by decreasing temperature from 200 to 77 K. Detailed analysis on the temperature dependence of threshold power density for light emission from Ge-QD/SiN μ-disks array is ongoing.

IV. Conclusion

An ingenious combination of lithography and self-assembled growth has allowed accurate control over the geometric conditions of our "designer" Ge QDs with high-temperature thermal stability. This significant fabrication advantage has opened up the possibility of 3-D integration of top-SiN waveguided Ge photonics for on-chip ultrafine sensing and optical interconnect applications.

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