Understanding the Excess 1/f Noise in MOSFETs at Cryogenic Temperatures

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***Abstract*— Characterization, modeling, and development of cryo-temperature CMOS technologies (cryo-CMOS) have significantly progressed to help overcome the interconnection bottleneck between qubits and the readout interface in quantum computers. Nevertheless, available compact models still fail to predict the deviation of 1/f noise from the expected linear scaling with temperature (*T*), referred to as "excess 1/f noise," observed at cryogenic temperatures. In addition, 1/f noise represents one of the main limiting factors for the decoherence time of qubits. In this article, we extensively characterize low-frequency noise on commercial 28-nm CMOS and on research-grade Ge-channel MOSFETs at temperatures ranging from 370 K down to 4 K. Our investigations exclude electron heating and bulk dielectric defects as possible causes of the excess 1/f noise at low temperatures. We show further evidence for a strong correlation between the excess 1/f noise and the saturation of the subthreshold swing (SS) observed at low temperatures. The most plausible cause of the excess noise is found in band tail states in the channel acting as additional capture/emission centers at cryogenic temperatures.**

***Index Terms*— 1/f noise, cryo-CMOS, MOSFET, quantum computing, traps.**

I. Introduction

QUANTUM computers represent a promising disruptive technology able to solve algorithms that are computationally unfeasible on classical computers (e.g., prime number factorization) [1]. Implementing a system with thousands of logical qubits would greatly advance fields such as cryptography, artificial intelligence, and physics simulations [2], [3], [4]. In most applications, the qubits operate at temperatures of a few mK, while the control electronics are placed outside the cryostat and operate at room temperature. In such an implementation, long wires between qubits and the control electronics increase the latency, noise, and complexity of the system. Wiring is thus a major bottleneck in realizing quantum computers with many qubits [5]. Significant improvements could be obtained by placing the qubit control electronics in a chamber at 4 K next to the quantum processor. CMOS technology is the preferred candidate for this task due to its excellent performance, availability, and low cost [6]. However, requirements for controlling numerous qubits are stringent, especially in terms of power consumption and noise [7]. Several cryo-CMOS qubit controllers have been demonstrated [8], yet more accurate noise characterization and modeling at low temperatures are needed to further improve their performance. Moreover, 1/f noise is one of the limiting factors for the decoherence time of qubits [9], [10]. Identifying the origin of the 1/f noise at cryogenic temperatures in MOSFETs could eventually lead to improved decoherence times in qubits. A better understanding of the 1/f noise at low temperatures is thus fundamental for both cryo-CMOS and qubits.

Based on carrier number fluctuations (CNFs) with correlated mobility fluctuations (MFs) [11], the expression for the input-referred 1/f drain current noise ($S_{vg} = S_{id}/g_m^2$) is

$$S_{vg} = \frac{qkTN_{BT}}{WLC_{ox}^2\alpha} \cdot \frac{1}{f} \cdot \left(1 + \Omega\frac{I_D}{g_m}\right)^2 \quad (1)$$

where N_{BT} is the volumetric gate dielectric trap density per unit energy, g_m is the transconductance, I_D is the drain current, C_{ox} is the gate capacitance per unit area, f is the frequency, α is the exponent of wentzel–kramers–brillouin (WKB) tunneling probability for a rectangular barrier, Ω is a parameter related to MF, and W and L are the width and length of the channel, respectively. Equation (1) predicts a linear temperature scaling when CNF dominate ($\Omega I_D/g_m \ll 1$), while noise measurements on a single device [12], [13] and the noise figure of circuits operating at 4 K [8] show that the noise is significantly higher than this prediction. Currently, the behavior of 1/f noise at low temperatures is not explained by any available 1/f noise model. Moreover, there is a lack of extensive noise characterization data at cryogenic temperatures needed to develop dependable and accurate noise models.

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In this article, we measure commercial 28-nm CMOS devices and research-grade Ge MOSFETs down to cryogenic temperatures, and we critically analyze many possible causes of this excess noise at low temperatures. The article proceeds as follows. Section II introduces the experimental setup and the measurement conditions, while Section III presents the experimental results and discussion. Finally, Section IV summarizes the main outcomes.

II. Experimental Setup

DC and noise measurements from 370 K down to 4 K were performed with a Lakeshore CRX-4 K cryogenic probe station and a Keysight E4727A noise analyzer.

We measured foundry 28-nm bulk MOSFETs with ultralow V_T and different areas. Ge-channel MOSFETs with $W = 10\ \mu$m and $L = 1\ \mu$m fabricated at imec [14] extend the analysis to alternative channel materials.

Great care has been taken to ensure a stable temperature during the noise characterization and to avoid any drift of the contact resistance. The same gate voltage overdrive ($V_{ov} = V_{gs} - V_T$, where V_T is extrapolated from the linear $I_D - V_{gs}$ curve at the point of maximum g_m [15]) was kept across different temperatures when measuring noise above the threshold to maintain the same inversion condition. On the other hand, we kept the same drain current when measuring in the subthreshold.

III. Results and Discussion

In this section, we first present the DC, AC, and noise characterization across temperatures of the devices introduced in Section II. After that, we extensively discuss possible causes of excess 1/f noise. Finally, we investigate the correlation between 1/f noise and band tail states.

A. DC and AC Characterization

The transfer characteristics, transconductance, and gate capacitance of MOSFETs in 28-nm technology with $W = 1\ \mu$m and $L = 0.5\ \mu$m from 370 K down to 4 K have been reported in [16]. Fig. 1 shows the temperature trends of I_{on} (defined as I_D at $V_{gs} = 0.9$ V and $V_{ds} = 20$ mV), $g_{m,MAX}$, $|I_G|$, and $|V_T|$. The I_{ON} current and the maximum transconductance $g_{m,MAX}$ increase at decreasing temperatures, while Fig. 1(c) shows that $|I_G|$ is essentially unvaried with T. The $|V_T|$ increases by approximately 150–200 mV when going from 300 to 4 K. As shown in [16], the gate capacitance of these devices does not vary when going from 295 K down to 4 K. Therefore, the value of C_{ox} does not introduce any additional temperature dependence in the S_{vg} [see (1)].

B. Temperature Scaling of 1/f Noise

To analyze how the noise scales with temperature, we fit S_{vg} measured at $V_{ds} = 20$ mV with a dedicated 1/f curve for each temperature; this is motivated by the fact that low-frequency noise in large-area devices exhibits an essentially 1/f dependence in the explored frequency range (10 Hz to 10 kHz). In the CNF model, $S_{vg} \cdot f$ has no dependence on I_D, while in the MF model it has a $(I_D/g_m)^2$ dependence [see (1)]. Fig. 2 shows $S_{vg} \cdot f$ versus I_D for $T = 300$ K and $T = 4$ K, and for $|V_{ov}|$ ranging from 0 to 0.6 V with a 0.1 V step (both nMOS and pMOS). As one can see, at low I_D (small V_{ov}) CNF describe the noise better, especially in the nMOS, while at high I_D (large V_{ov}), MF dominate. Notice that the dominant mechanism (CNF or MF) for a given V_{ov} is the same at $T = 300$ K and $T = 4$ K.

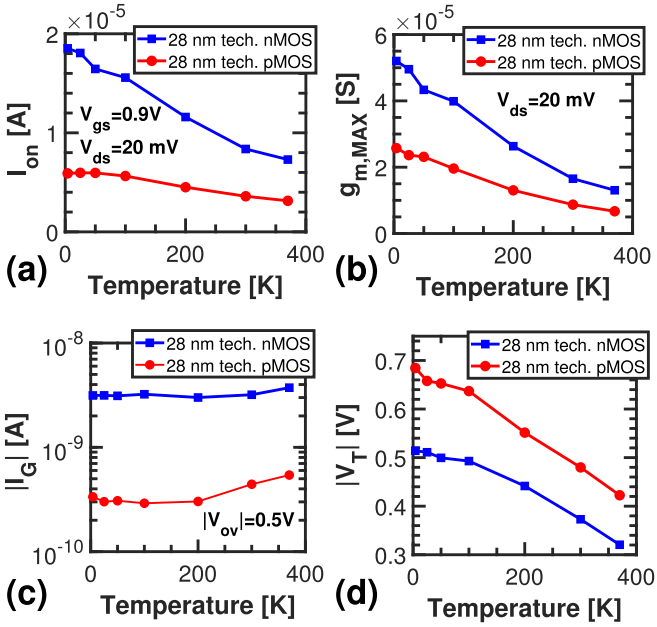

Fig. 1. Plot of (a) I_{on}, (b) $g_{m,MAX}$, (c) $|I_G|$, and (d) $|V_T|$ against temperature for the 28-nm technology nMOS and pMOS.

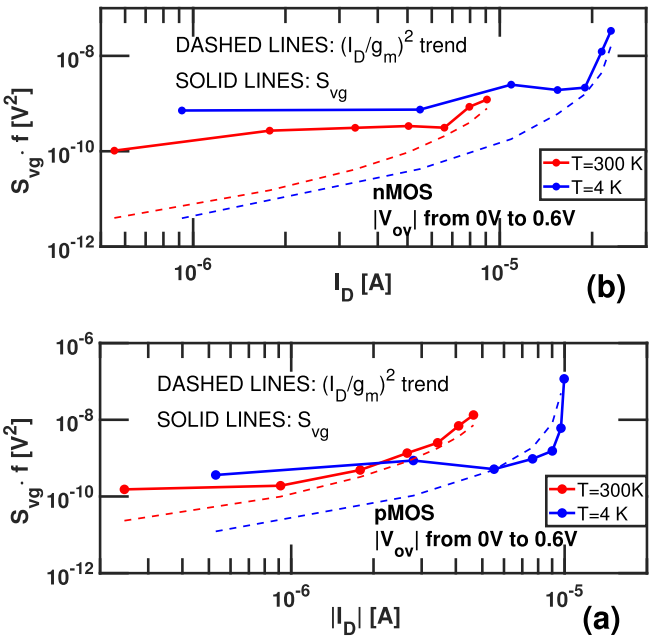

Fig. 2. Plot of $S_{vg} \cdot f$ (solid) and $(I_D/g_m)^2$ trend (dashed) as a function of I_D for the 28-nm technology (a) nMOS and (b) pMOS at $T = 300$ K and $T = 4$ K. Each point corresponds to a $|V_{ov}|$ that goes from 0 to 0.6 V with a 0.1 V step. At low I_D (low V_{ov}), CNFs dominate the noise, while MFs dominate at high I_D (high V_{ov}); see (1).

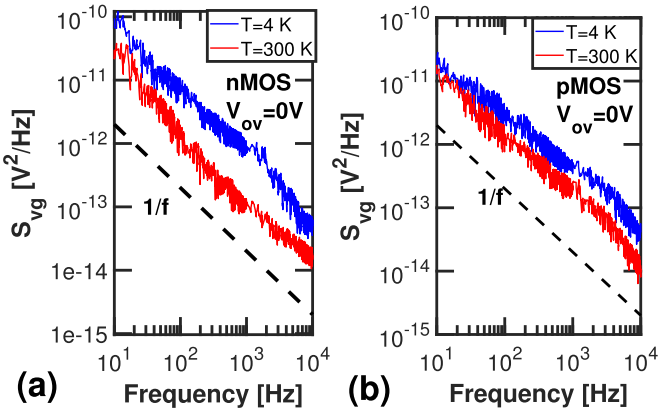

Fig. 3. S_{vg} measurements on the 28-nm technology (a) nMOS and (b) pMOS at 300 and 4 K for $V_{ov} = 0$ V and $V_{ds} = 20$ mV. Notice that the noise amplitude at 4 K is higher than the one at 300 K, contradicting the linear temperature dependence of (1).

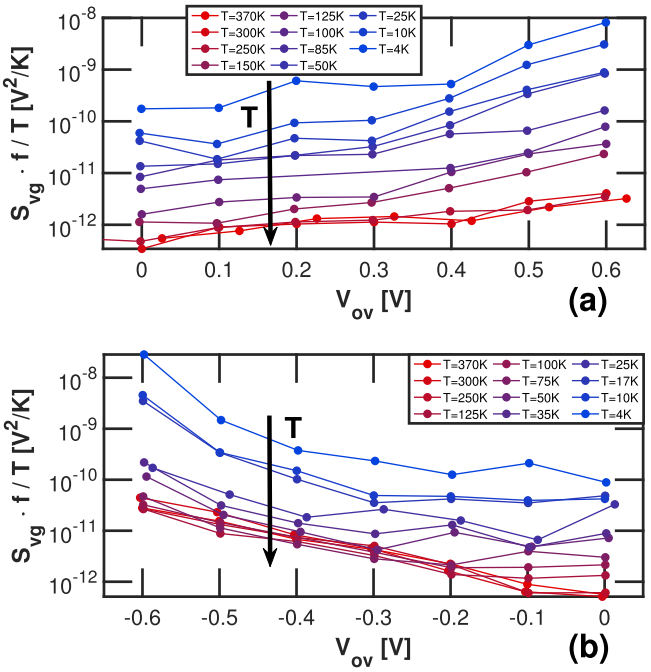

Fig. 4. Plot of $S_{vg} \cdot f/T$ as a function of V_{ov} for the 28-nm technology (a) nMOS and (b) pMOS at different temperatures and $V_{ds} = 20$ mV. Notice that $S_{vg} \cdot f/T$ increases at decreasing temperatures, contrary to the prediction of (1).

Fig. 3 compares S_{vg} measured at 300 and 4 K on the 28-nm technology MOSFETs at $V_{ov} = 0$ V where CNF dominate. The noise at 4 K is higher than at 300 K; therefore, S_{vg} does not scale linearly with T as predicted by the commonly used model of (1). We examine the temperature dependence of S_{vg} at different V_{ov} for a more comprehensive analysis. If the 1/f noise scales with T, one should obtain the same value of $S_{vg} \cdot f/T$ across different temperatures for a given V_{ov}. Fig. 4 reveals clearly that at low temperatures, the curves do not longer overlap (as they instead do at temperatures above 100 K) for neither n- and p-MOSFETs, and an excess 1/f noise of approximately two orders of magnitude appears at 4 K compared to room temperature. In addition, the excess

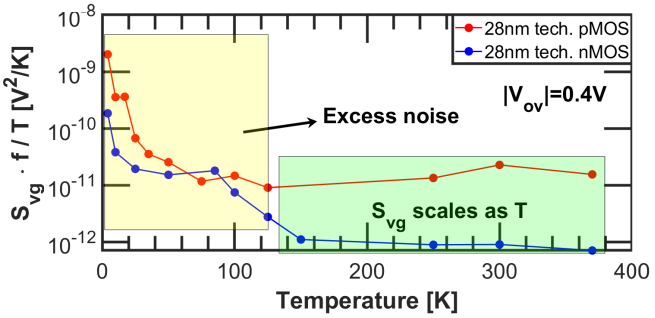

Fig. 5. Plot of $S_{vg} \cdot f/T$ versus temperature at $|V_{ov}| = 0.4$ V for the 28-nm technology nMOS and pMOS. S_{vg} scales as T [in accordance with (1)] down to approximately 100 K. Below that, the S_{vg} has an unexpected increase.

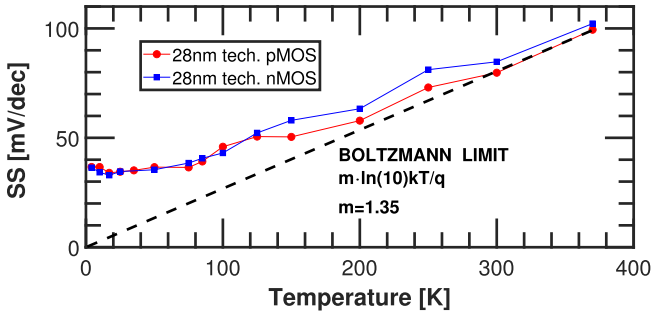

Fig. 6. Comparison between the SS extracted at $I_D \approx 10$ nA for the 28-nm technology nMOS and pMOS with $W = 1$ μm and $L = 0.5$ μm at different temperatures and the Boltzmann limit. We found that the SS starts saturating around $T = 100$ K.

noise observed in Fig. 4 is present for all the V_{ov} values, indicating that the excess 1/f noise shows up in both CNF and MF regimes. Therefore, the excess noise is independent of the noise mechanism (CNF or MF) dominating the 1/f noise.

Focusing the analysis on $|V_{ov}| = 0.4$ V in Fig. 5, we see that the noise scales with T down to approximately 100 K. Below that T, there is a significant increase not predicted by (1). Notice that the subthreshold swing (SS) saturates around 100 K as well (Fig. 6), consistently with [17], suggesting a strong correlation between this phenomenon and the excess 1/f noise.

Fig. 7 confirms the area scaling of the noise amplitude at 4 K by plotting $S_{vg} \cdot WL$ of devices with different areas at $|V_{ov}| = 0.1$ V. The $S_{vg} \cdot WL$ partly overlap, suggesting that the same defects are contributing to the noise. The S_{vg} of small-area devices is missing some noise contributions when compared to S_{vg} of large-area devices as the number of defects in each device starts to become countable.

C. Investigating the Origin of the Excess Noise

Several physical mechanisms are possible candidates to explain this excess 1/f noise. Since this effect is observed on a single-channel device in the linear region with low dissipated power ($P_{diss} \leq 3$ μW), self-heating can be safely excluded [18].

The linear T-scaling of (1) originates from the integral $\int_{-\infty}^{+\infty} f_T(1 - f_T) dE_T$ [19], where f_T is the near-equilibrium

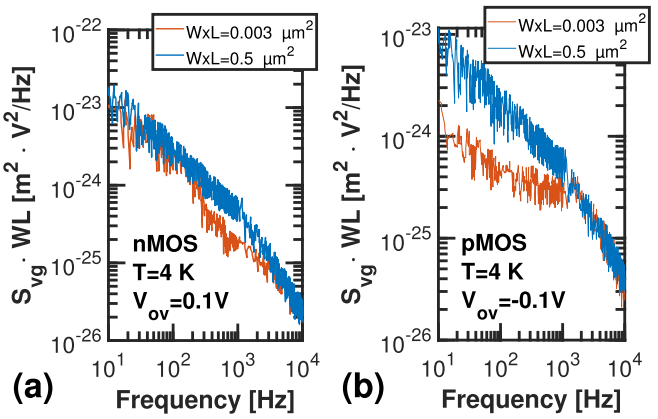

Fig. 7. Comparison between $S_{vg} \cdot WL$ of a large-area ($WL = 0.5\ \mu m^2$) and small-area ($WL = 0.003\ \mu m^2$) (a) nMOS and (b) pMOS at $T = 4$ K and $|V_{ov}| = 0.1$ V.

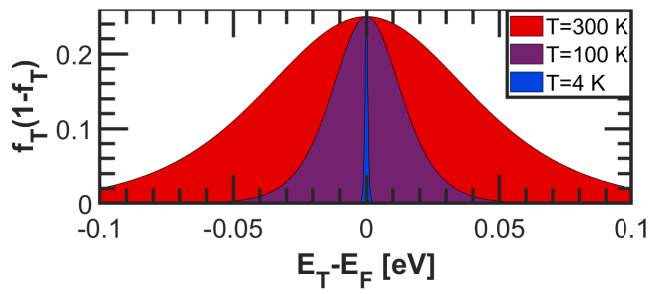

Fig. 8. Plot of $f_T(1 - f_T)$ versus $E_T - E_F$ for different temperatures. The colored area under the curves represents the integral and is equal to kT.

occupation function of the dielectric traps. Assuming that f_T is described by a Fermi function with Fermi level E_F, the integral above is the area under a bell-shaped function centered at $E_T = E_F$ (Fig. 8). The value of this integral is at most equal to kT but never larger than that. Therefore, it cannot predict the excess noise observed in Figs. 3–5. However, notice that the T going into f_T represents the *electron* temperature, which can be higher than the *lattice* and *ambient* temperatures as electrons gain kinetic energy drifting along the channel. To check whether the electron temperature plays a role in the observed phenomenon, we remeasured the same curves of Fig. 4 with an increased V_{ds} of 100 mV instead of the previously used V_{ds} of 20 mV. This voltage range maintains the FET in the linear region [as required by (1)] while increasing the lateral electric field in the channel and hence the average electron energy. As seen in Fig. 9, the $S_{vg} \cdot f/T$ scaling with temperature (for a fixed V_{ov}) is essentially independent of V_{ds}. Therefore, we can also rule out electron heating as the main cause behind the excess noise.

At low temperatures, the energy alignment between the channel Fermi level and dielectric traps could be different compared to room temperature, even at the same V_{ov}. If the dielectric trap distribution in energy is very narrow, a slight change in the energy alignment could increase N_{BT} seen in (1) and explain the excess 1/f noise. However, such a huge N_{BT} change would likely increase trap-assisted tunneling (TAT) and, therefore, the gate leakage current [20]. As shown in [16]

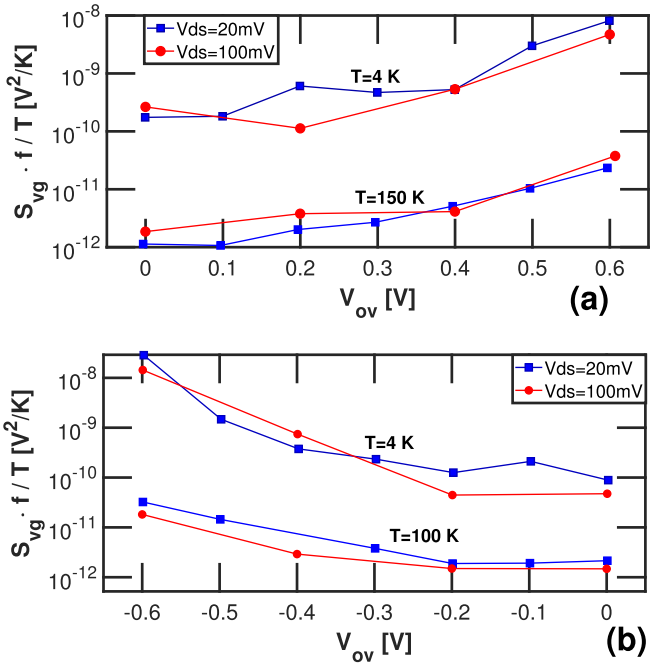

Fig. 9. Plot of $S_{vg} \cdot f/T$ versus V_{ov} for the 28-nm technology (a) nMOS and (b) pMOS at different V_{ds} and two different temperatures. The S_{vg} does not increase even if V_{ds} is increased by a factor of 5, ruling out electron heating as the main cause of excess noise.

and Fig. 1(c), I_G does not increase at low temperatures (it even slightly decreases for the pMOS). Furthermore, pMOS and nMOS are sensitive to different dielectric defect energies [21], [22]; hence, if the excess noise were related to N_{BT}, it would likely show different signatures for the two device types. However, we do not see any notable difference between the temperature noise scaling of nMOS and pMOS in Fig. 5. Therefore, we conclude that the excess noise cannot be attributed to an increased density of active traps in the bulk of the dielectric at low temperatures.

Incomplete ionization of the bulk doping could also induce additional fluctuations in the drain current at low temperatures. However, the foundry 28-nm pMOS and nMOS feature different bulk doping concentrations [23]. In particular, the nMOS channel doping concentration is one order of magnitude higher than the pMOS one, while we do not see this remarkable asymmetry in the excess noise behavior of Fig. 5. We can thus rule out incomplete ionization of bulk doping as the main source of 1/f excess noise.

To check whether the excess 1/f noise is related to the channel material, we repeat the noise measurements of Fig. 4 on Ge-channel MOSFETs. Fig. 10 shows that the excess noise appears at a similar temperature also in Ge MOSFETs. Consequently, the excess 1/f noise is not related to a particular channel material.

D. Relationship Between Band Tail States and 1/f Noise

As stated above, both the excess 1/f noise and the saturation of SS appear below 100 K. SS saturation is attributed to disorder-induced states (i.e., states created by interrupted crystalline periodicity, surface roughness, impurities, strain, etc.)

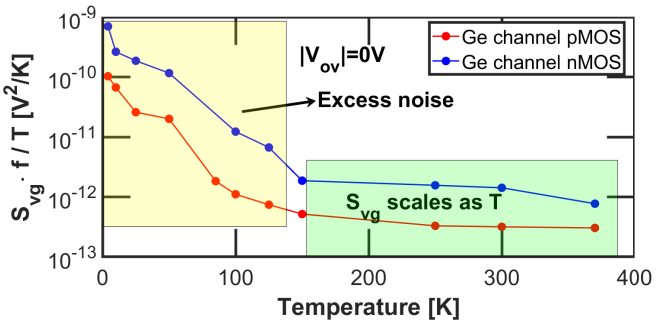

Fig. 10. Plot of $S_{vg} \cdot f/T$ versus temperature at $|V_{ov}| = 0$ V for Ge-channel nMOS and pMOS. S_{vg} scales as T [in accordance with (1)] down to approximately 100 K. After that, S_{vg} has an unexpected increase (similar to Fig. 5) even with Ge as channel material.

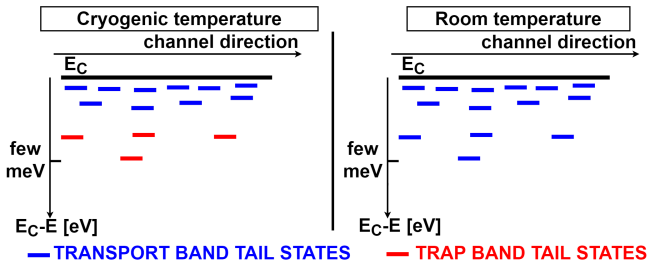

Fig. 11. Sketch of band tail states along the channel direction at cryogenic and room temperature.

with energies close to the conduction/valence bands of the channel. These so-called band tail states are often modeled with an exponentially decaying distribution in energy [17]. To comply with the observed trends of Figs. 5 and 10, the amount of band tail states that act as traps would need to increase at cryogenic temperatures. As sketched in Fig. 11, our measurements suggest that band tail states start to behave as traps at cryogenic temperatures. The definition adopted to distinguish "transport" and "trap" states is based on their occupation kinetics. Thus, a state is a trap if its occupancy fluctuates with a frequency low enough to be inside the noise measurement window (in our case 10 Hz–10 kHz). This behavior could be related to the temperature dependence of the hopping mechanism in band tail states [24]. The relationship between band tail states and excess noise is also suggested by [12] where a correlation is observed between SS saturation and an increase in 1/f noise at low T by varying the surface crystal orientation (hence, the surface density of Si atoms and thus of band tail states).

To check if these states can be responsible for the 1/f noise at cryogenic temperatures, we calculate S_{vg} for the CNF region according to the following expression [25], [26]:

$$S_{vg} = \frac{q^2}{WLC_{ox}^2} \iint \frac{4f_T(1-f_T)\tau}{1+(2\pi f\tau)^2} N_{BT} K(z)\, dE_T dz \quad (2)$$

where z is the direction perpendicular to the channel and τ is the trapping/de-trapping time implemented according to the nonradiative multiphonon (NMP) model with correction for cryogenic temperatures [23], [27]. Notice that τ increases exponentially with z due to electron tunneling from the channel into the dielectric. When the traps are in the channel, there is no electron tunneling barrier to reach the defects and therefore τ is smaller compared to the case of dielectric traps. The $K(z)$ term takes into account the electrostatic charge scaling between the trapped charge and the channel charge. It is equal to 1 when considering traps inside the channel (such as the band tail states), while it assumes a more complex form for dielectric traps in a gate-stack with an interlayer (see Table I in [25]). Considering an nMOS, we attempt to reproduce the effect of band tail states in the noise by inserting a trap distribution in the silicon channel with an exponential distribution in energy and space

$$N_{BT} = N_0 \exp\left(\frac{z-z_0}{\sigma_z}\right) \exp\left(\frac{E_T - E_C}{\sigma_E}\right) \quad (3)$$

if $z \leq z_0$ and $E_T \leq E_C$, and $N_{BT} = 0$ otherwise. N_0 is the surface ($z = z_0$) concentration at the band edge, E_C is conduction band energy, and z_0 and z are the positions of the Si/SiO_2 interface and of the band tail state, respectively, in the direction perpendicular to the channel. We first check the effect of band tail states on S_{vg} by using (3) into N_{BT} without inserting any dielectric trap. In this way, we highlight the contribution of band tail states to S_{vg}. This is shown in Fig. 12(a), where S_{vg} calculated with (2) at 300 and 4 K with only band tail states into N_{BT} is compared to the measurements of Fig. 3(a). These states induce very low noise at 300 K because their occupation kinetics are fast and we only observe the flat part of a Lorentzian spectrum in the 10 Hz–10 kHz frequency range. On the other hand, the fluctuations of band tail states show up as 1/f noise at cryogenic temperatures with an amplitude compatible with the measurements. Let us now insert also dielectric traps *in addition* to the band tail states into N_{BT}. Fig. 12(b) shows that the noise predicted by (2) at cryogenic temperature is only due to band tail states [same noise spectrum of Fig. 12(a)]. On the other hand, inserting dielectric traps into (2) reproduces the noise measurements of Fig. 3(a) at 300 K because the effect of dielectric traps dominates above cryogenic temperatures. This qualitative modeling approach supports the idea that band tail states can behave as traps at cryogenic temperatures, although more detailed analyses are necessary to reproduce all the features of low-temperature 1/f noise.

TABLE I
MAIN PARAMETERS USED TO CALCULATE S_{VG} WITH (2). THE PARAMETERS USED TO COMPUTE τ IN (2) ARE FROM [23] AND [27]

Parameter	Value in Eq. 2
C_{ox}	$2 \cdot 10^{-2}$ F/m^2
$W \cdot L$	0.5 μm^2
$E_C - E_F$	1 meV
N_{BT} in SiO_2	$5 \cdot 10^{18}$ cm^{-3} eV^{-1}
N_{BT} in HfO_2	$1 \cdot 10^{19}$ cm^{-3} eV^{-1}
N_0 (Band tail states)	$1 \cdot 10^{20}$ cm^{-3} eV^{-1}
σ_z (Band tail states)	5 nm
σ_E (Band tail states)	5 meV

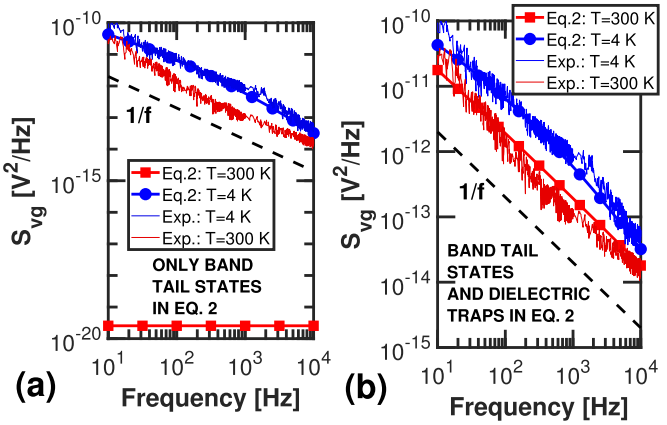

Fig. 12. Comparison between S_{vg} evaluated through (2) and the experimental results of Fig. 3(a) at $T = 300$ K and $T = 4$ K. In (a), we only have band tail states into N_{BT} of (2), while in (b), we also have dielectric traps in addition to the band tail states. The parameters used in (2) are listed in Table I.

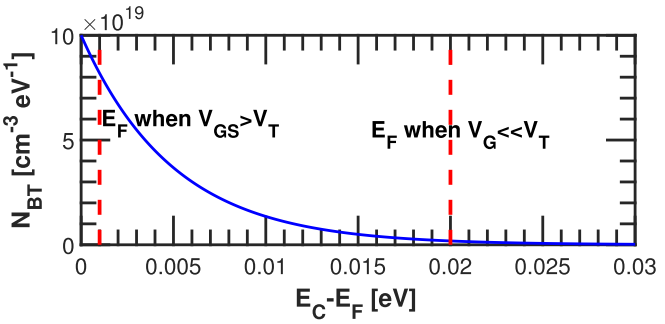

Fig. 13. Plot of the band tail states distribution in the energy. The Fermi level in inversion and far below the threshold are highlighted by dashed red lines. Notice that the amount of band tail states that fluctuate when $V_G \ll V_T$ is much smaller compared to $V_G > V_T$.

E. RTN Measurements in Subthreshold

According to the explanation above, devices operating well below V_T should not have excess noise at cryogenic temperature since the Fermi level of the channel would not probe the band tail states (Fig. 13). Unfortunately, measuring the noise in subthreshold on the large-area devices yields a noise amplitude comparable to the instrumentation noise due to the reduction of S_{vg} with the device area [see (1)]. Therefore, to test this explanation, we identified a small-area device ($W = 100$ nm and $L = 30$ nm) where the random telegraph noise (RTN) waveform of the same defect is traced from 4 to 35 K without any increase in $\Delta V_T = \Delta I_D/g_m$ (Fig. 14), where ΔI_D is the fluctuation of the drain current from the DC value. The measurements refer to a foundry 28-nm pMOS at $I_D \approx 30$ nA (≈200 mV below the threshold at 4 K). A similar RTN behavior is reported in [27] where it is shown that the capture/emission times of traps become independent of T at cryogenic temperatures (in line with Fig. 14). According to Fig. 4(a), one would expect a different S_{vg} going from 35 to 4 K also in a small-area device. However, the 4 and 35 K S_{vg} measured at the same bias conditions of the RTN traces overlap with each other (Fig. 15), consistent with the hypothesis that we do not probe band tail states when we are well below V_T. Notice that S_{vg} of these small-area devices

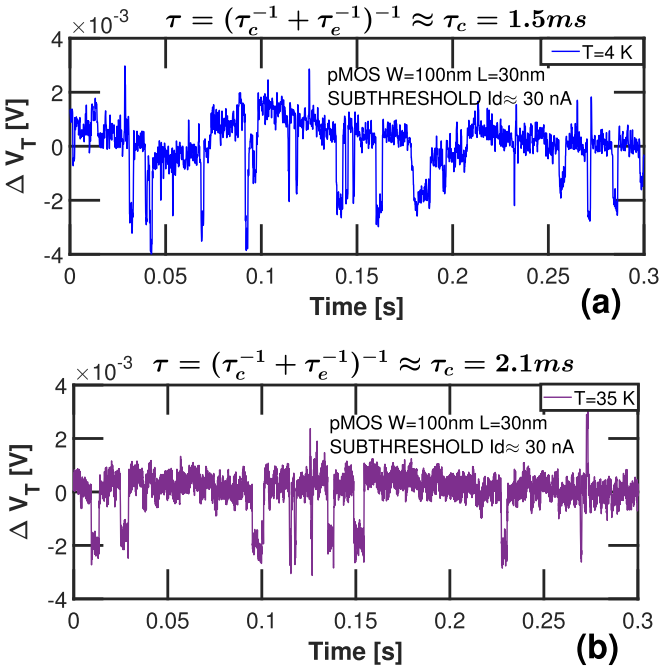

Fig. 14. Time trace of $\Delta V_T = \Delta i_d/g_m$ for the small-area ($W = 100$ nm and $L = 30$ nm) 28-nm technology pMOS at (a) $T = 4$ K and (b) $T = 35$ K. The trapping dynamics (i.e., capture/emission times) and the ΔV_T amplitudes are very similar.

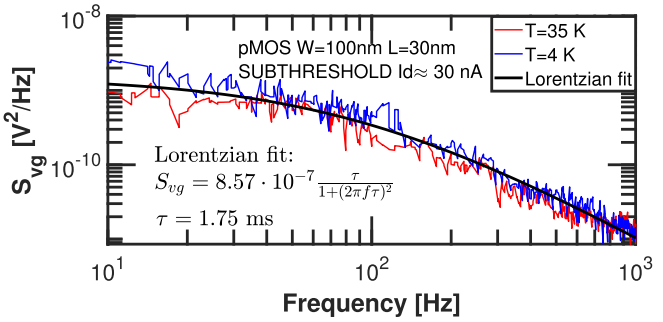

Fig. 15. Plot of S_{vg} versus frequency for a small-area ($W = 100$ nm and $L = 30$ nm) 28-nm technology pMOS at $T = 4$ K and $T = 35$ K. Notice that the two curves overlap and are fitted with a Lorentzian PSD with $\tau = 1.75$ ms (average between the τ extracted from the traces in Fig. 14).

do not scale as T, because only a few traps contribute to the noise, and the integral $\int_{-\infty}^{+\infty} f_T(1 - f_T)dE_T$ is replaced by a sum over discrete states not leading to kT.

IV. Conclusion

Noise measurements in a commercial 28-nm technology in the 370–4 K range show a significant excess 1/f noise at cryogenic temperatures, which cannot be explained by conventional noise models. This excess noise is present in both CNF and MF regimes. Our experiments exclude self-heating, electron heating, and the interaction with additional bulk dielectric defects as possible causes. Moreover, measurements of the same behavior on Ge-channel MOSFETs prove that this effect is not restricted to Si. This phenomenon strongly correlates with the SS saturation and the presence of

band tail states that could act as traps at low temperatures. RTN and spectral noise measurements on small-area devices further confirm that this excess noise is not present when the channel Fermi level is not probing the band tail states. Our experiments thus provide a fundamental understanding of the abnormal 1/f noise increase observed in MOSFETs at cryogenic temperatures and highlight that band tail states could well be at the origin of the observed excess 1/f noise.

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