Impact of Inherent Design Limitations for Cu–Sn SLID Microbumps on Its Electromigration Reliability for 3D ICs

Nikhilendu Tiwary, *Member, IEEE*, Glenn Ross, *Member, IEEE*, Vesa Vuorinen, and Mervi Paulasto-Kröckel, *Member, IEEE*

***Abstract*— Continuous scaling of package architectures requires small volume and high-density microbumps in 3D stacking, which often result in solders fully transforming to intermetallic compounds (IMCs). Cu–Sn solid–liquid interdiffusion (SLID) bonding is an attractive technology where the μbumps are fully composed of IMCs. In this work, test structures made up of Cu_3Sn IMC μbump with a lateral dimension of 25 μm $\times$ 25 μm and 50 μm $\times$ 50 μm, respectively, were manufactured on a pair of 4-inch Si wafers demonstrating wafer-level bonding capability. Electromigration (EM) tests were performed for accelerated conditions at a temperature of 150 °C for various current densities ranging from $\approx 2 \times 10^4$ to 1×10^5 A/cm^2. Scanning electron microscopy (SEM) and elemental dispersive spectroscopy (EDS) were employed to characterize the as-fabricated test structures. Due to Sn squeeze out, Cu_3Sn was formed at undesired location at the upper Cu trace. Both nondestructive [lock-in thermography (LiT)] and destructive techniques were employed to analyze the failure locations after EM tests. It was observed that the likelihood of failure spots is the current crowding zone along the interconnects in 3D architectures, which gets aggravated due to the formation of Cu_3Sn in undesirable locations. Thermal runaway was observed even in Cu_3Sn, which has been shown to be EM-resistant in the past, thus underlining inherent design issues of μbumps utilizing SLID technology.**

***Index Terms*— 3D ICs, Cu–Sn solid–liquid interdiffusion (SLID) bonding, electromigration (EM), failure analysis, heterogeneous integration.**

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I. Introduction

THE 3D stacking of discrete chips with different functionalities is a key requirement for advanced packaging solutions for realization of smart systems, high-performance computing systems, internet of things (IoT), or "More than Moore" technologies [1], [2]. Often, the requirement is on high density, fine pitch, and small-volume interconnects for power efficient, high bandwidth, low latency, and low system cost for 3D heterogeneous packaging technologies [2]. This brings stringent reliability requirements on the interconnects. One of the main failure mechanisms of ultra-fine interconnects is electromigration (EM), which occurs due to momentum transfer from moving electrons to the metallic atoms under the influence of an applied electric field [1], [3]. Moreover, due to the inherent complexities in 3D architectures, such as current crowding at turns, the combined effect of Joule heating and EM has been identified as a dominant failure mechanism in 3D ICs [3].

Small-volume interconnections (diameter <100 μm) mostly rely on flip chip (FC) bumping technology also known as the "workhorse for advanced packaging solutions" [1]. The FC bumps incorporates a solder layer, such as SnAgCu (SAC) alloys placed in between metallic contacts, Fig. 1(a). With continuous shrinking of the solder volume for high density and fine pitch interconnects, a large volume of solder μbumps gets transformed into intermetallic compounds (IMCs), Fig. 1(b) [4]. These IMCs (hard, high Young's modulus) then not only dominate the mechanical properties of the solders (soft, low Young's modulus), but also degrade their EM reliability performance by offering additional flux divergence paths within the μbump at the solder/IMC interface [5]. The flux divergence in a layer occurs due to different mass diffusivities across layers with different material properties and are the sites of EM failure at high current densities. In contrast, in solid–liquid interdiffusion (SLID) bonding technology, the interconnect formation depends on complete formation of IMCs, Fig. 1(c). These IMCs are metallic interconnects owing to its low resistivity. Moreover, it has been shown that full IMC μbumps offer better EM resistance compared with the solder μbumps [4], [6]. The critical product, which is a measure of the resistance to EM, is reported to be larger for IMC-based μbumps than for soft Sn-based solders [7].

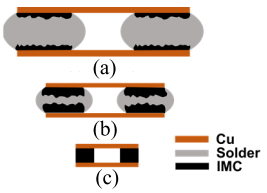

Fig. 1. Schematic of (a) FC bumps with diameter $D \approx 100$ μm and (b) with $D \approx 30$ μm, and (c) SLID bumps with $D < 30$ μm.

Although SLID utilizing various metal combinations has been demonstrated, such as Au–Sn, Ag–Sn, Cu–In, Cu–Sn, and Ni–Sn–Cu, the extensively researched is the Cu–Sn SLID system [8], due to its low cost, simple processing steps, and easy integration with Cu through silicon vias (TSVs) in the system. Here, the Sn layer is equivalent to the solder layer in FC bumps, sandwiched between Cu layers. In the Cu–Sn SLID bonding process, the low melting point (MP) T_L metal (Sn) is deposited on the higher MP T_H metal (Cu). The bonding occurs at temperature (≈300 °C), which is greater than T_L. As a result, Sn melts with subsequent Cu dissolution and formation of IMCs. At the typical bonding temperature of ≈300 °C, the IMCs that could form are Cu_6Sn_5 (MP—415 °C) and Cu_3Sn (MP—676 °C) [8]. The Cu_3Sn IMC is the thermodynamically stable phase, which forms entirely in the bond after which no more Cu is consumed. Since reduction in size of FC μbumps (diameter <30 μm) would often result in complete formation of IMCs in μbumps, it will ultimately resemble SLID μbumps, Fig. 1(c) [4]. Therefore, EM studies should be carried out on SLID IMC-based μbumps to examine the failures not only at lower current densities but also catastrophic failures at higher current densities to gain insights to avoid such failures in the real devices.

Limited studies are present in the literature on the EM reliability of fully Cu_3Sn IMC μbumps. A 20-nm Cu_3Sn IMC layer on Cu interconnect has been shown to block surface diffusion paths in Cu, thereby enhancing its EM reliability [9]. Moreover, a larger driving force is required to dissociate Cu or Sn atoms from Cu_3Sn intermetallic layer [9]. Labie et al. [10] demonstrated that fully formed IMC μbumps outperform standard solder bumps in reliability. In other work, Labie et al. [6] compared the EM reliability of two Cu/Sn/Cu samples manufactured with 3.5- and 8-μm thickness of Sn. The IMCs present were both Cu_6Sn_5 (at the middle of the μbump) sandwiched between Cu_3Sn, which then were connected to Cu under bump metallization (UBM). At the stringent test conditions of 1.1×10^5 A/cm^2 at 200 °C, the sample with 8-μm Sn layer survived the tests for initial 200 h, whereas the other one (3.5 μm of Sn) survived for more than 1000 h with no failures reported [6]. The failure in thick Sn samples was not attributed to the EM-induced damage, but Kirkendall void formation at the Cu/Cu_3Sn interface when Cu UBM is fully consumed. Chen et al. [4] performed EM tests at a current density of 2.1×10^5 A/cm^2 under 180 °C on a full IMC microjoint, and no EM-induced damage was observed for 5000 h of stressing. A negligible resistance increase (4%) after EM test in one of the samples was attributed to the damage in Al trace connecting the μbumps. Wang et al. [11] performed EM tests at 150 °C on Cu–Cu_3Sn–Cu microbumps manufactured with a solid-state-diffusion bonding process. For a current density of 5×10^4 A/cm^2, the resistance of the bumps was stable up to 140 h, but it showed an increase in the resistance value when the current density was increased to 1×10^5 A/cm^2. The resistance increase was attributed to the migration of copper layer, but it was not clarified how that increases the resistance. In other work, IMC bumps were EM tested at a current density of 4×10^5 A/cm^2 at 200 °C, and a resistance increase of 20% was measured within 1000 h of stressing time [7]. However, the morphology of the IMC contact remained stable, and the failure was related to the formation of Cu–Al IMCs at the lower Al level. In all the above studies, EM resistance capability of IMC μbumps was demonstrated to exceed in comparison with the solder μbumps. Also, the failures in the IMC μbumps were attributed to different mechanisms with mostly damage in the metallization contact layers, which are the current crowding locations [4], [6], [7].

Current crowding locations in 3D ICs have shown to be a major failure spot where thermal runaway problems typically arise as a combined effect of Joule heating and EM [3]. Thermal runaway resulting in local melting at current crowding locations has been reported earlier for eutectic PbSn-based solder [12]. In this work, test structures were fabricated by demonstrating wafer-level SLID bonding to study the reliability of Cu_3Sn IMCs with Cu at both top and bottom layers. The EM tests were conducted for various current densities at a temperature of 150 °C. Due to the combined effect of Joule heating and EM, thermal runaway was observed even in Cu_3Sn with a high MP of 676 °C, which was formed at upper Cu trace because of squeeze out and subsequent reaction of Sn during bonding. This work would examine this new failure mechanism not reported before in Cu_3Sn, which is formed at such undesired locations due to Sn squeeze out and which could easily aggravate in small-volume, fine-pitch SLID μbumps. This emphasizes the inherent limitations in SLID technology and the related design considerations for which the risk is rather underestimated.

II. Experimental Methods

A. Design of Test Structures

Various test structures, such as two bumps, daisy chain, and kelvin structures, were incorporated in the 4-in mask process. The μbumps were designed to be square in shape with the lateral dimensions ranging from 10 to 100 μm. A two-bump test structure was employed for this study. The advantage of this test structure is that the current flow from both top to bottom chip and bottom to top chip could be investigated with focus on just two μbumps. Fig. 2(a) shows the mask layout of the two-bump test structure along with the dimensions of the top and bottom chips. The bottom chip dimensions were 6 mm × 6 mm, and the top chip dimensions were 4 mm × 4 mm. The scribe lines used to dice the bonded chips are shown in red (partial cut) and blue (through cut).

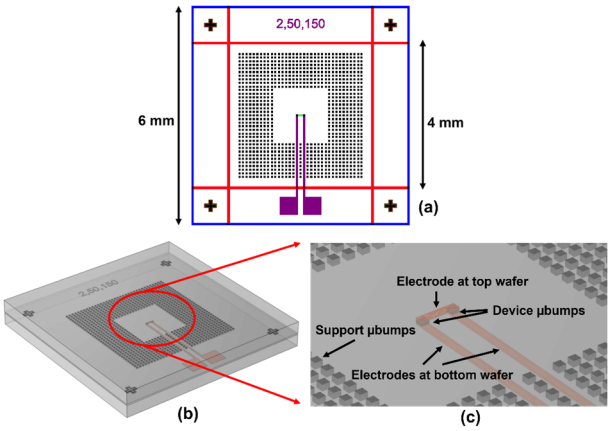

Fig. 2. (a) Layout of the chip with a two-bump test structure. Violet traces are the contacts on the bottom wafer, and green traces are the contacts on the top wafer. Bottom and top wafers are bonded through the bumps (black), (b) 3D schematic of the bonded chip, and (c) zoomed-in 3D schematic of the two-bump test structure.

The partial cuts denote the locations where only the top chip was diced to expose the Cu contact pads on the bottom chip for probing. The through cut denotes the locations where both top and bottom chips were diced. An array of support μbumps were also provided to mitigate the stress formed during the dicing process. Fig. 2(b) and (c) shows the 3D schematic of the bonded chip highlighting the device μbumps, support μbumps, and top and bottom Cu traces. In this work, the two-bump test structures, which were investigated, were of two lateral dimensions, i.e., 25 and 50 μm.

B. Device Fabrication

The fabrication of the test structures is a four-mask process. It starts with a pair of 4-inch double-sided polished (DSP) 100-orientated Si wafer. In the first step, the back-side patterning was carried out on the wafer pair, wherein the alignment marks and scribe lines were patterned using optical lithography and etched with reactive ion etching (RIE) tool with SF_6 as an etching gas for both bottom and top wafers, Fig. 3(a). A 15 nm of titanium tungsten (TiW) adhesion layer and a 100 nm of Cu seed layer were then sputter deposited on the front side of both the wafer pairs, Fig. 3(b) and (c). The front side of the wafer pair was then patterned to form the traces, contact pads, and support μbumps using an AZ15nXT (450 CPS) negative photoresist. The patterned wafer pair was treated with an oxygen plasma with an O_2 flowrate of 30 mL/min and an RF power of 100 W for 3 min to improve the wettability of the surface before electroplating. A 1 μm of Cu was then electroplated at a current density of 15 mA/cm^2 with NB SEMIPLATE CU 100 after which the resist was stripped, Fig. 3(d). Then, the device μbumps and the support μbumps were subsequently patterned using the same photoresist and treated with the oxygen plasma as described before. Subsequently, 4 μm of Cu (NB SEMIPLATE CU 100) and 2.5 μm of Sn (NB SEMIPLATE SN 100) were electroplated at a current density of 15 and 10 mA/cm^2, respectively, Fig. 3(e) and (f). After every electroplating step, the thickness was confirmed by a contact profilometer at five different locations across wafer. The final thickness of electrodeposited Cu and Sn was measured to be Cu—5.1 $\pm$ 0.3 μm and Sn—2.3 $\pm$ 0.2 μm for bottom wafer and Cu—4.9 $\pm$ 0.2 μm and Sn—2.5 $\pm$ 0.3 μm for top wafer.

After stripping the resist, the final patterning was done with the photoresist to protect the Cu traces and device μbumps during the etching step of the Cu seed layer and TiW adhesion layer. Cu was etched in a commercial etchant Cu etch 150 purchased from NB technologies GmbH, and TiW was etched in an H_2O_2 solution heated at 60 °C, Fig. 3(g). The etching of Cu and TiW layers was visually confirmed under an optical microscope before stripping the resist. Finally, the wafer bonding process was carried out in an Applied Microengineering Limited (AML) wafer bonder. The wafers were mounted on the top and bottom platens, and the chamber was pumped down to $\approx 1e-6$ bar. The wafers were preheated to 150 °C before bringing them into contact. After alignment of the wafers, a force of 8 kN ($\approx$20 MPa, total bonding area—4 cm^2) was applied on the platens, and the temperature was ramped up to 320 °C at a ramp up rate of 10 °C/min. The bonding was then carried out for 1-h duration, after which the temperature was ramped down. Finally, the bonded wafer pairs were diced along the through and partial cut scribe lines on a DAD3220 dicer tool from Disco, Fig. 3(h). Fig. 3(i) shows the schematic of the bond line, Cu–Cu_3Sn–Cu. Fig. 3(j) shows the platen force and temperatures versus time from the wafer bonding process. A good match was there between the temperatures of the upper and lower platens. Fig. 3(k) shows the scanning electron microscopy (SEM) image of the final fabricated chip.

C. Nondestructive Analysis

The nondestructive analysis of the chips was carried out with two techniques. Phoenix GE Nanomex with minimum detectability of 200 nm was employed for X-ray imaging of the chips. Sentris from Optotherm Inc. was employed for lock-in thermography (LiT) to locate the failure zones in the EM stressed chips.

D. Destructive Analysis

As can be seen from Fig. 2, the device bumps are at the middle of the chip. To assess it for cross-sectional imaging, the chips were first cut in two parts along a horizontal cutline at the vicinity of the device μbumps ($\approx$300 μm away) with a femtosecond laser micromachining tool. A femtosecond laser has now been widely used for destructive analysis, which generates negligible laser-induced damage to the samples [13]. The cut chips were then molded into epoxy and cured for subsequent grinding and polishing steps, which was carried out using standard metallographic methods.

E. SEM Characterization

After sample preparation, the initial cross-sectional imaging of the support bumps and elemental dispersive spectroscopy (EDS) point analysis was carried out with JEOL JSM-6335F field-emission SEM (FESEM) equipped with the Oxford Instruments INCA X-sight EDS detector. After EM tests,

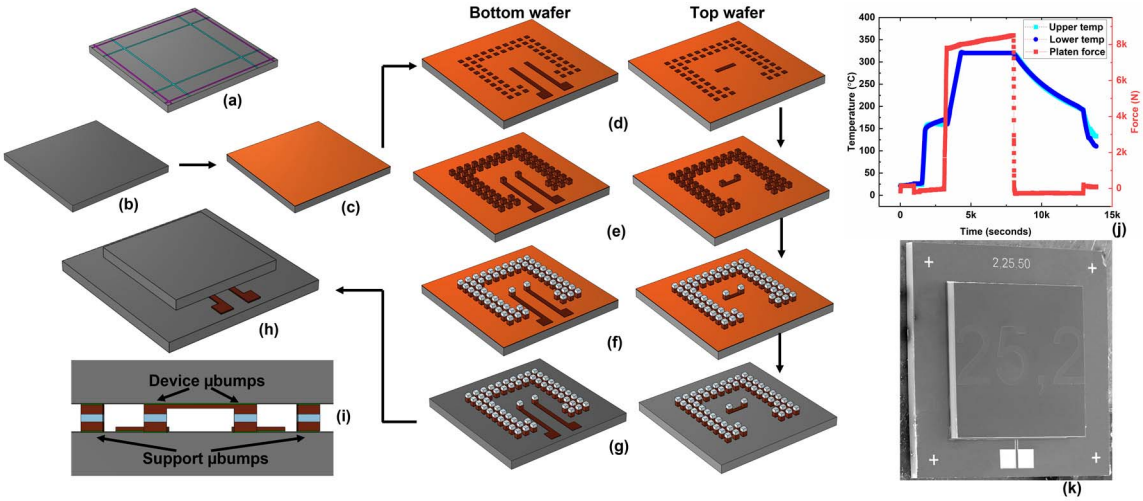

Fig. 3. (a) Back side patterning for scribe lines, magenta for bottom wafer (through cut), and cyan for top wafer (partial cut—only top wafer), (b) front side Si wafer, (c) TiW/Cu deposition, (d) patterning and electrodeposition of Cu electrodes on bottom and top wafers, (e) patterning and electrodeposition of Cu bumps, (f) electrodeposition of Sn bumps, (g) etching of Cu seed layer and TiW, (h) wafer bonding and dicing, (i) cut plane across the chip showing the Cu (brown)–Cu_3Sn (blue)–Cu (brown) bond line, (j) wafer bonding process profile, and (k) SEM image of the as-fabricated chip.

the cross-sectional imaging and in-depth analysis of the test structures were carried out with a dual beam focused ion beam (FIB)-SEM JEOL JIB-4700F equipped with the Oxford instruments Ultim Max 100 EDS detector.

F. EM Tests

Before the EM tests, a current–voltage (I–V) sweep analysis was performed on the as-fabricated chips to assess the linear resistance of the bumps. The I–V tests were conducted via an Agilent B1500 semiconductor parameter analyzer. A voltage sweep from −0.5 to 0.5 V was performed, and the corresponding current values were recorded. Subsequently, EM tests were performed on a thermal chuck at 150 °C with Keithley 2231A-30-3 three-channel dc power supply with nominal current densities across the μbumps ranging from 2×10^4 to 1×10^5 A/cm^2. The current densities were calculated based on the ideal dimensions of μbumps (25 and 50 μm^2).

III. Results and Discussion

A. SEM Cross-Sectional Imaging

Fig. 4(a) and (b) shows the cross-sectional SEM images of the support μbumps of 25- and 50-μm test structures, respectively. The EDS point analysis of the μbumps shows that Cu_3Sn was formed in the bond line, with the atomic percentage of Cu and Sn as ≈73.8% ± 0.3% and ≈26.2% ± 0.3%, respectively. Moreover, in the support μbumps from 50-μm test structures, small amount of Cu_6Sn_5 was observed, Fig. 4(b). It was also confirmed with the EDS point analysis with the atomic percentage of Cu and Sn as ≈58.0% ± 1.8% and ≈42.0% ± 1.8%, respectively. However, Cu_6Sn_5 was not observed in the support μbumps from 25-μm test structures.

Fig. 4(c) and (e) shows the SEM images of the device μbumps from 25- and 50-μm test structures, respectively. Cu_3Sn was also observed to be formed on the top Cu trace, which is due to the squeeze out of liquid Sn during the bonding process [shown in Fig. 4(c) (red circle)]. Ideally, the upper Cu trace should connect the Cu pads of the two μbumps, as shown in the schematic of Fig. 3(i). Fig. 4(d) and (f) shows the EDS elemental mapping of Cu, Sn, and Si on the test structures. Fig. 4(g) and (h) shows the atomic percentage plots across the cutline shown in the inset, respectively. As can be seen, full Cu_3Sn was formed in the bond line, and the atomic weight percentage of the Cu and Sn was found to be ≈71.1% ± 1.8% and ≈27.2% ± 1.9%, respectively. No Cu_6Sn_5 was observed in the device μbumps of the test structures under consideration. The height of all the μbumps measured was ≈11 μm. The total thickness of the electroplated Cu and Sn stack from top and bottom wafer was ≈15 μm, so the reduction in thickness of the final bond line is attributed to the squeeze out of liquid Sn. Moreover, formation of voids could be seen in the test structures concentrated mostly at the Cu/Cu_3Sn interface, which is widely reported due to interplay of various parameters, such as Kirkendall voiding and impurities incorporation in the electroplated structures [14], [15].

B. I–V Sweep and EM Tests

Fig. 5(a) and (b) shows the linear I–V characteristics of the two-bump test structures performed before the EM tests. The resistance of the two-bump test structures measured varied from 6 to 7 Ω and 3 to 4 Ω for the 25- and 50-μm test structure, respectively. Fig. 5(c) shows the EM test of a 25-μm test structure (25-μm TS1) conducted on a thermal chuck at 150 °C at a current density of ≈8×10^4 A/cm^2 (current value 0.5 A). The resistance was stable for ≈63 h [time to failure (TTF)] after which there was a sudden jump in the resistance value, which was stable for further 30 h. Fig. 5(d) shows the EM test result of another 25-μm test structure (25-μm TS2)

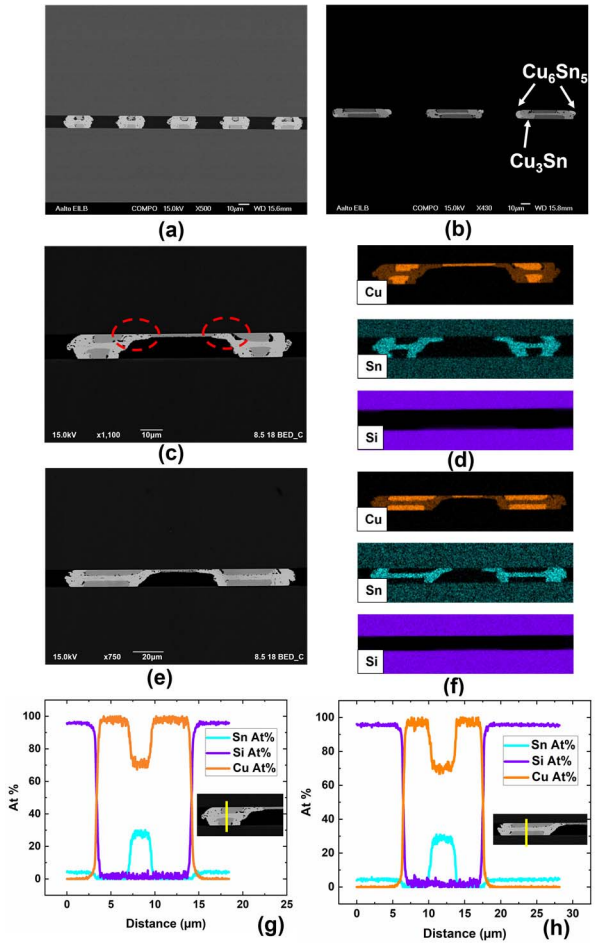

Fig. 4. (a) SEM image of 25-μm support bumps, (b) SEM image of 50-μm support bumps, and (c) SEM image of 25-μm two-bump test structure. Cu_3Sn formed due to Sn squeeze out at the upper Cu trace is shown in red circle, (d) EDS elemental maps of the 25-μm test structure, (e) SEM image of 50-μm two-bump test structure, (f) EDS elemental maps of the 50-μm test structure, and atomic percentage plot versus distance across the cutline shown in the inset figure for (g) 25-μm device μbump and (h) 50-μm device μbump.

conducted at 150 °C and at a current density of $\approx 1 \times 10^5$ A/cm^2. In this case, the resistance was stable for $\approx$105 h before the failure.

For the 50-μm test structure (50-μm TS), for the current level of 0.5 A, the current density corresponds to $\approx 2 \times 10^4$ A/cm^2. At this current density, the resistance was observed to be stable for $\approx$336 h (approximately two weeks), and no failure was recorded, Fig. 5(e) and (f). The current density was then increased to $\approx 4 \times 10^4$ A/cm^2 and monitored for $\approx$40 min during which the resistance was again stable. The small increase in the base resistance because of increase in current could be attributed to the Joule heating, which increased the measured resistance value. Subsequently, the current density was increased to $\approx 6 \times 10^4$ A/cm^2 (current—1.5 A), and the resistance was observed to gradually increase after which the test was terminated.

C. Failure Analysis

1) Nondestructive Failure Analysis: Two techniques were employed for the nondestructive analysis of the failure spots in the EM tested sample—X-ray imaging and LiT. The X-ray imaging of the chips is an effective way of examining the μbumps and checking the alignment of the chips.

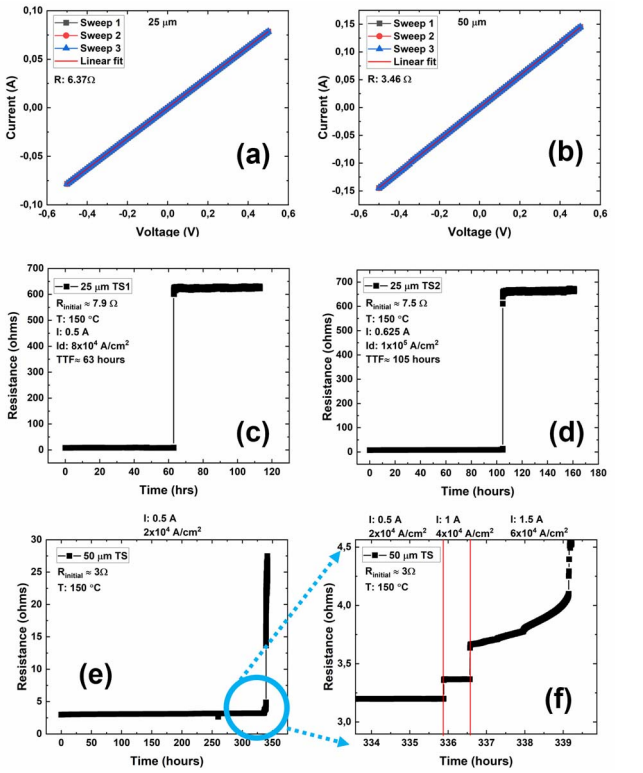

Fig. 5. *I–V* characteristics of (a) 25-μm test structure and (b) 50-μm test structure, EM tests of 25-μm test structures for a current density of (c) 8×10^4 and (d) 1×10^5 A/cm^2, and (e) and (f) EM tests of the 50-μm test structure.

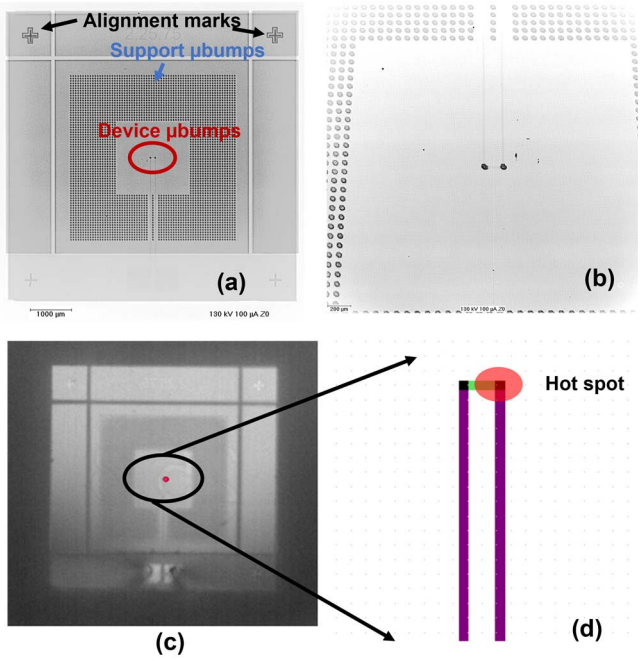

Fig. 6. (a) 2-D X-ray image of 25-μm TS1 chip with the device μbumps and support μbumps marked, (b) zoomed-in image of the device bumps with tilt, (c) LiT thermal image of the chip showing the hot spot, which indicates probable failure location, and (d) schematic showing the location of the hot spot in (c).

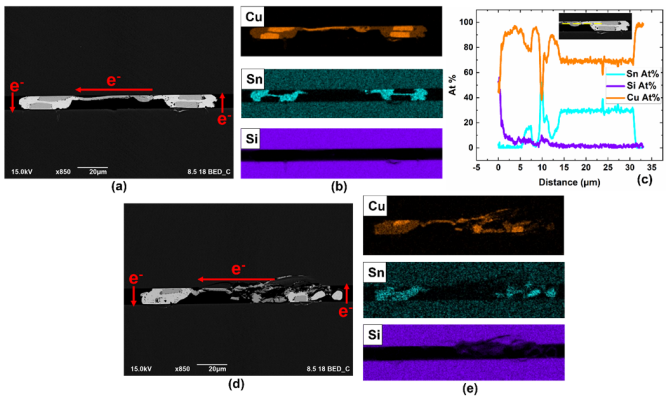

Fig. 7. (a) SEM image of EM tested 25-μm TS1 for a current density of 8×10^4 A/cm^2 with the electron current direction shown, (b) corresponding EDS elemental maps, (c) atomic percentage plot versus distance across the cutline shown in the inset, (d) SEM image of EM tested 25-μm TS2 for a current density of 10^5 A/cm^2 with the electron current direction shown, and (e) corresponding EDS elemental maps.

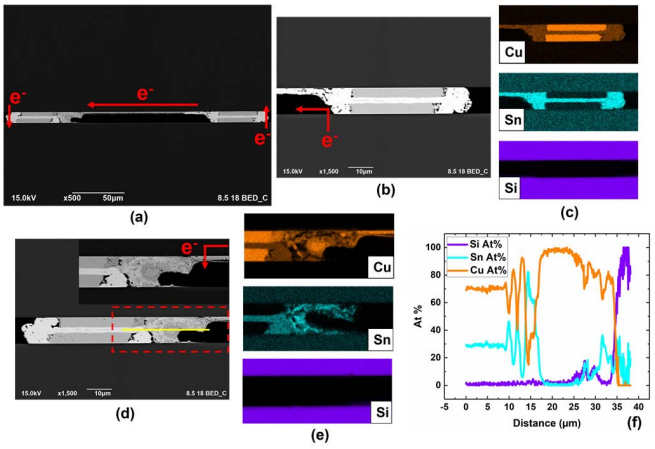

Fig. 8. (a) SEM image of EM tested 50-μm TS with the electron current direction shown, (b) zoomed-in SEM image of the right bump and (c) corresponding EDS elemental maps, (d) zoomed-in SEM image of the left bump and (e) corresponding EDS elemental maps, and (f) atomic percentage plot versus distance across the yellow cutline shown in (d).

Fig. 6(a) shows the image of an entire chip, where device μbumps and support μbumps are marked. The alignment marks at the top corners (left and right) demonstrate good alignment of the top and bottom chips. Fig. 6(b) shows the zoomed-in image of the device μbumps. Two limitations were recognized: 1) small size—the size of the bumps was $\approx$25 μm $\times$ 25 μm $\times$ 11 μm, which is too low for effective analysis and 2) the device μbumps were surrounded by the support μbumps, which makes the full 3D image construction of the device μbumps challenging.

On the other hand, LiT demonstrated effectiveness in locating the failure spots. The applied voltage during the LiT tests was set to 8.5 V at a frequency of 2.5 Hz, and the thermal image was acquired after 46 cycles. Fig. 6(c) shows the infrared (IR) thermal image of EM stressed sample for 25-μm test structure (25-μm TS1) of which the EM test result is shown in Fig. 5(c). The hot spot corresponding to the probable failure location near the device μbumps is clearly visible.

2) Destructive Failure Analysis (FIB): A destructive analysis was carried out to explore the probable failure locations in detail. Fig. 7(a) and (b) shows the SEM and elemental EDS mapping of the device μbumps from 25-μm TS1, which was EM tested [Fig. 5(c)] and on which the LiT analysis was performed [Fig. 6(c)]. Cu traces were found to be delaminated near the location where hot spot was observed. Due to delamination, the dissipation of Joule heating gets affected, which results in hot spot formation adjacent to those locations. On the other hand, accumulation of Cu was observed on the Cu trace near to the right bump, Fig. 7(a). Fig. 7(c) shows the EDS line scan generated from the cutline shown in the inset. With closer analysis of the line scans, diffusion of Sn into the Cu trace due to EM could be suspected. The diffusion of Sn in the direction of electronic current at higher temperatures has also been widely reported in the literature for solder bumps [16].

Fig. 7(d) and (e) shows the SEM and elemental EDS mapping of 25-μm TS2 sample, which was tested at a current density of $\approx 1 \times 10^5$ A/cm^2 [Fig. 5(d)]. As can be seen from the elemental maps, complete burnout and melting of μbump and silicon were observed in the right bump. Also, delamination [similar to Fig. 7(a)] and cracking of upper Cu trace were observed near the left bump. However, no detailed information could be extracted regarding the initiation and mechanism of failure, as the tests continued for almost $\approx$55 h after the failure [Fig. 5(d)].

Fig. 8(a) shows the SEM image of the 50-μm TS for which the EM test is shown in Fig. 5(e) and (f). The EM tests were terminated when sudden increase in the resistance was observed at a current density of $\approx 6 \times 10^4$ A/cm^2. Fig. 8(b) and (c) shows the zoomed-in SEM image of the right bump and elemental EDS maps, respectively. No failure spots were observed at this location. In contrast to the 25-μm test structures [Fig. 7(a) and (d)], the right bump is fully intact. This could be due to the lower current density (even for max—6×10^4 A/cm^2) because of the 4$\times$ increase in the cross-sectional area as compared with 25-μm test structures. Fig. 8(d) and (e) shows the SEM image and the elemental maps of the left bump, respectively. From the mapping result, a segregation of Cu and Sn could be observed in the Cu_3Sn layer near the upper Cu trace, which indicates local melting, as no thermodynamically stable phase could be identified from Cu–Sn system phase diagram with respect to the measured Cu–Sn atomic percentages. Fig. 8(f) shows the atomic percentage plots versus distance across the yellow cutline shown in Fig. 8(d). At the middle of the bump, the composition indicates Cu_3Sn but clearly deviates and shows irregular Cu- and Sn-rich regions. Since the region that was originally Cu_3Sn is supposed to be EM-resistant and thermally stable until 676 °C, observation of these kind of failures has not been reported before.

Then, FIB milling was carried out to examine the region underneath the surface of the failure location. Fig. 9(a)–(d) shows the SEM image after FIB cut and the corresponding elemental map data for Cu, Sn, and Si. The Cu- and Sn-rich regions also penetrate beneath the surface. Interestingly, silicon was also found to be incorporated in traces at the

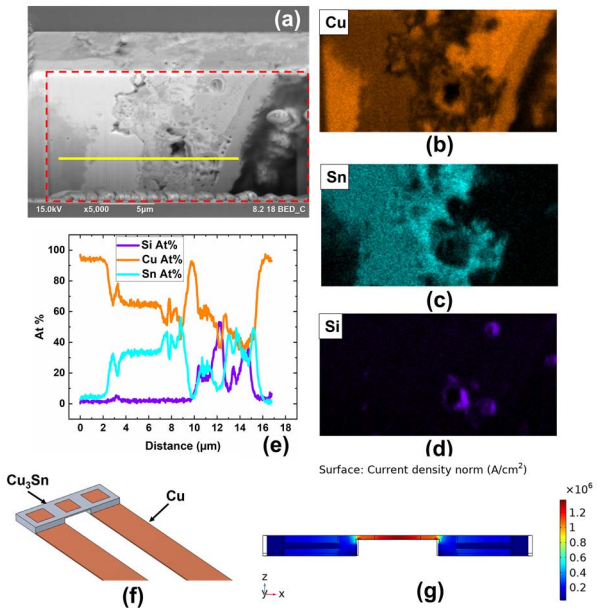

Fig. 9. (a) SEM image after FIB cut of the failure location, elemental maps for (b) Cu, (c) Sn, (d) Si, (e) atomic percentage plots across cutline shown in Fig. 8(a), (f) model schematic of the two-bump test structure, and (g) current density distribution across a cut plane midway of the test structure.

failure location. Fig. 9(e) shows the EDS line scan across the yellow cutline shown in Fig. 9(a), which confirmed the presence of silicon. Although the current density across the 50-μm bumps is lower than 25-μm bumps (4$\times$ cross-sectional area difference), the current density across the upper Cu trace of 50-μm test structure is higher than the Cu trace of 25-μm test structure (2$\times$ cross-sectional area difference) for the maximum current of 1.5 A. Furthermore, even though the EM tests were conducted at 150 °C, the actual temperature near the μbumps at the current crowding zone could be much higher due to Joule heating [3]. As a result, the resistance at the current crowding zone would further increase, ultimately resulting in thermal runaway. This would then result in the local melting of Cu_3Sn and dissolution of Si in the melt with subsequent solidification after the tests are terminated.

To assess the current density levels, the 50-μm two-bump test structure was constructed in the finite element (FE) model in COMSOL by accounting the Cu_3Sn formation due to Sn squeeze out across the Cu bumps, Fig. 9(f). Here, Cu_3Sn formation fully encloses the Cu bump to mimic the experimental observation. The electrical conductivities of Cu and Cu_3Sn were taken as 58.1×10^6 and 11.2×10^6 S/m, respectively. Fig. 9(g) shows the current density distribution for a current of 1 A across a cut plane from the center of the two-bump test structure. The current density is an order of magnitude higher near to the location where failures were observed as compared with the current density in μbumps. Moreover, the resistivity of Cu_3Sn is also higher than Cu, which also worsen the scenario due to Joule heating at the current crowding locations resulting in thermal runaway. This shows that Cu_3Sn though it is thermally stable until 676 °C, such kind of failures could also occur, underlining the importance of proper designing of the SLID μbumps in 3D ICs. Specifically, care must be taken to minimize Sn squeeze out during the bonding process to ultimately prevent Cu_3Sn formation in unwanted locations.

IV. Conclusion

In this work, the wafer-level Cu–Sn SLID bonding process was demonstrated by incorporating various test structures. Due to Sn squeeze out, Cu_3Sn was observed to form at unwanted locations at the upper Cu trace connecting the two-bump test structure. The test structures were tested for its EM reliability to study different failure modes. For 25-μm test structures, two types of failures were observed. For a current density of 8×10^4 A/cm^2, delamination of Cu traces was observed, whereas catastrophic failure in addition to delamination of Cu trace was observed at a higher current density of 1×10^5 A/cm^2. For the 50-μm test structure, thermal runaway-based failure was observed in Cu_3Sn at current crowding location. Therefore, although Cu_3Sn has been shown to be EM-resistant with high thermal stability, thermal runaway and catastrophic failures could not be ruled out in Cu_3Sn in 3D architectures at high current densities due to its formation at unwanted locations. This emphasizes the need of proper designing of SLID μbumps in heterogeneous integration to prevent Sn squeeze out and prevent the formation of Cu_3Sn at undesired locations. This would include proper design considerations to minimize Sn squeeze out, which includes the following: 1) engineering lateral dimensions of the bumps in top and bottom wafers; 2) optimal Sn thickness; and 3) optimal bonding force. The above aspects are easy to control in chip-level bonding, but will be difficult to control in the wafer-level bonding process where nonuniformities in the thickness of electroplating stacks could pose problems on the overall yield. Future work will incorporate these aspects to address the inherent limitations in SLID μbumps for interconnects for enhanced EM reliability.

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