# Investigation of Frequency Models to Predict Dynamic Behavior of ESD Protection Networks

Fabrice Caignet, François Ruffat, Alexandre Boyer, Guillaume Mejecaze, Fabien Escudié, and Fréderic Puybaret

***Abstract*—With the shrinking dimension of technologies and safety requirements, electrostatic discharge (ESD) protections play a more and more important role. Consequently, the prediction of the transient behavior's protection network is becoming difficult for system level designers in order to guarantee systems safety. A model reproducing the turn-ON behavior is needed to obtain a precise simulation's protection strategy network, especially during the protection triggering. In this article, we propose a complete measurement and computation setup to access an equivalent frequency model of devices under strong pulse injections for a rapid model construction. Details of the measurement and data computation to obtain a frequency model using a transmission line pulse generator combined with time-domain reflectometry measurement will be provided. To validate our proposed frequency model, a comparison between the measurements and simulations is first performed on passive and linear components, and then on two protection devices (transient voltage suppressor). A simulation on a protection network, at the board level, will show that the combination of the frequency models could be done to predict its response to ESD pulse with an acceptable precision, without the tedious step of component modeling.**

***Index Terms*—Electrostatic discharge (ESD) protection device models, *S* parameters, system level ESD, transmission line pulse (TLP).**

## I. Introduction

EMBEDDED systems are using more and more computations and high-frequency communications. All these electronics' products are constituted by complex integrated circuits (IC) that assume most of the system's functionalities. Those electronics have to survive harsh environments that induce fast electrical transient, such as electrostatic discharge (ESD). As a result, numerous standards exist to reproduce most of the common stresses that electronic systems have to survive in their environment, such as the very well-known IEC 61000-4-2 also called gun stress [1]. System designers must consider security requirements to ensure that systems survive any stress that occurs and they also must predict the robustness against system level ESD up to some kilovolt as defined by the article presented in [2].

This work focuses on systems defined as a printed circuit board (PCB) on which network protections are developed to ensure that all the system functionalities will survive ESD stresses. The most sensitive device is the IC that integrates dedicated on-chip ESD protections. But these protections are not always sufficient to protect ICs against strong system level stresses. As a result, additional protections are added on the PCB, such as passive components (*R*, *L*, or *C*). PCB lines can also be used to introduce propagation effects, or even external protections, such as transient voltage suppressor (TVS).

Building simulation models to predict robustness to system level ESD is not an easy task [2]. Models should be elaborated for each element of the protection network, including models for all the components (diodes, TVS, and snapback devices) that are nonlinear elements.

The key measurement system to build models of ESD protections is the transmission line pulse (TLP) generator [3], [4]. Many studies have proposed quasi-static models based on TLP measurements [5], [6]. A piecewise linear $I(V)$ curve is extracted and used in the simulation. These models are able to reproduce the system behavior in most cases as presented in papers [7], [8], [9], [10], [11], [12], [13], [14], [15]. All these publications show how behavioral models, based on quasi-static characterization, can give good results if they are combined with parasitic elements of PCB and ICs.

But in some cases, this approach is not sufficient because the turn-ON behavior of the protection is not reproduced. This could lead to a simulation in which the initial overvoltage is not predicted correctly. There is nowadays an increased demand to develop dynamic ESD models that consider the protections dynamic behavior.

One of the most related problems is to develop models with a sufficient accuracy considering the dynamic behavior, such as the protection device's triggering behavior to obtain a good estimation of the overvoltages [16], [17], [18], [19], [20]. Papers generally propose Simulation Program with Integrated Circuit Emphasis (SPICE)-like models to address this issue. However, these SPICE models could be difficult to build and implement because they could generate convergence issues. Moreover, we need dedicated parameters extracted from measurements with high-frequency bandwidth (up to few GHz) and high-power

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injection (in the order of some kV and tens of Amps). A conventional measurement technique to characterize protection devices without damaging the devices is the TLP. Using this generator, some authors have proposed dynamic models for protection devices [17], [18], [19], [20], [21]. The model extraction is based on measurements using both voltage and current probes, which are frequency limited. In this article, we propose a direct measurement model, called the black-box model. It can be used both in time and frequency domains based on the response of the device under test (DUT) to a strong pulse injection. The method is based on the TLP generator used to reach high-power injection combined with time-domain reflectometry (TDR) (see Fig. 1), as introduced in [17]. Here, a different measurement and calibration setup are presented. The proposed setup uses only one voltage probe and no current probe, which may introduce bandwidth limitation as suggested in [22] and [23]. From our proposal measurement system, called TLP-based TDR measurements, an equivalent *S* parameter model is obtained assuming a linear time-invariance (LTI) condition. This assumption has been addressed in paper [23] for protection devices. In this previous paper, the obtained model bandwidth was 200 MHz. We propose now an improvement of the method providing valid models up to 1 GHz.

The rest of this article is organized as follows. The whole setup as well as the dedicated calibration process to obtain the frequency model is presented in Section II. In Section III, the method is validated on linear devices. Frequency models are extracted and used to launch transient simulations. *S*11 parameters obtained with our TLP-based TDR method are compared with vector network analyser (VNA) measurements under low-level injections first. For higher level pulse injections, simulations are performed in the time domain using the *S*11 obtained with the proposed method and compared with the measured transient waveforms to validate the relevance of the extracted models. In Section IV, frequency models of two nonlinear devices, such as TVS, are built. Time-domain simulations using our frequency model are performed showing a good agreement with time-domain measurement. In addition, a conventional PCB-mounted network used to protect devices, composed of TVS followed by a *CRC* network, is investigated. The main goal is to verify if the valid transient simulation can be achieved with frequency models. Finally, Sectionnbsp;V concludes this article.

## II. Principles of Model Extraction Method—Measurements and Processing

### A. TLP-Based TDR Measurement Method

The aim of this method is to obtain a frequency model of a two-terminal protection device (e.g., a filtering capacitor and TVS) based on the measurement of the reflection coefficient of a load impedance through a TDR method [10].

The TDR method principle, as illustrated in Fig. 1, is based on the injection of a forward voltage $V_i$, which is reflected as $V_r$, by the terminal load impedance $Z_{\mathrm{DUT}}$. The measurements of $V_i$ and $V_r$ allow to compute the transient impedance, where $Z_0$ is the characteristic impedance of the cable that drives $V_i$. Equation (1) gives the reflection coefficient, $\Gamma(x_{\mathrm{DUT}}, t)$ at a distance $x_{\mathrm{DUT}}$

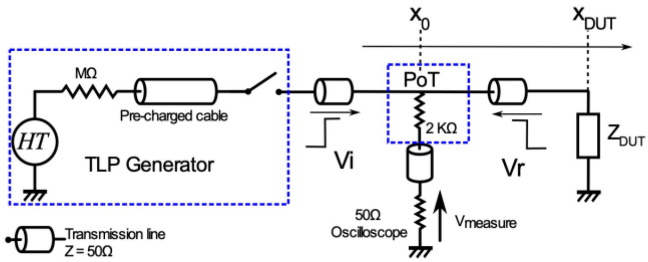


Fig. 1. Principle of the TLP-based TDR measurement method.

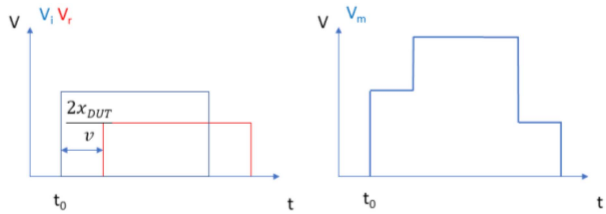


Fig. 2. Example of TDR waveform for an unmatched load.

from the measurement. From this equation, $Z_{\mathrm{DUT}}$ is extracted as

$$\Gamma\left(x_{\mathrm{DUT}}, t\right) = \frac{z_{\mathrm{DUT}}\left(t\right) - Z_0}{z_{\mathrm{DUT}}\left(t\right) + Z_0} = \frac{V_r\left(x_{\mathrm{DUT}}, t\right)}{V_i\left(x_{\mathrm{DUT}}, t\right)}. \quad (1)$$

The pulse is generated by a TLP generator. A pick-off tee (PoT), linked to an oscilloscope, is used to measure the voltage. The distance $x = 0$ is defined at the measurement point. All the lines between the different elements are 50 Ω matched. Forward and reflected voltages overlap, as reported in Fig. 2, with the example on an unmatched load. The measured voltage $V_m$ at a given distance $x$ is constructed from the reflection coefficient $\Gamma(x,t)$ according to the following equation:

$$V_m\left(x, t\right) = V_i\left(x, t\right) + V_r\left(x, t\right). \quad (2)$$

The time delay, $2\,x_{\mathrm{DUT}}/\nu$, between $V_r$ and $V_i$ is related to the distance of the measurement point $x_{\mathrm{DUT}}$ between DUT and PoT and the velocity of the cable, $\nu$. This delay leads to a complex transient waveform for an unmatched load, as shown in Fig. 2. In this article, all the measurements to get the models are performed using 100 ps TLP rise time. The propagation velocity is around 5 ns/m. The PoT is placed at a minimum distance of 3 cm from the DUT. In such condition, the overlap is limited.

Having $V_m$, $V_i$, and $V_r$ must be separated to compute the reflection coefficient. The TDR gives either the transient reflected coefficient or impedance of the DUT. The spectra of $V_i$ and $V_r$ are computed from a Fourier transform, in order to obtain the reflection coefficient, or *S* parameter, in the frequency domain

$$S_{11}\left(x_{\mathrm{DUT}}, f\right) = \frac{Z_{\mathrm{DUT}}\left(f\right) - Z_0}{Z_{\mathrm{DUT}}\left(f\right) + Z_0} = \frac{V_r\left(x_{\mathrm{DUT}}, f\right)}{V_i\left(x_{\mathrm{DUT}}, f\right)}. \quad (3)$$

A calibration method is needed to extract $V_i$, regardless of the connected load, to take into account all the elements of the setup (TLP, cables, PoT, and oscilloscope). The distance $x_{\mathrm{DUT}}$ should be extracted precisely to separate $V_i$ and $V_r$. To get $x_{\mathrm{DUT}}$,

a precalibration on a 50 Ω load and on an open or a short load is needed. Computation is performed using the autocorrelation function. Moreover, some mismatch impedance could appear depending on the elements between the PoT and the DUT, and some corrections should be provided. A matched load $Z_0$ is used instead of $Z_{\mathrm{DUT}}$ to cancel $V_r$ and ensure that $V_m = V_i$. The setup parameters and charge voltage level of the TLP are identical to those used to measure $V_m$ on $Z_{\mathrm{DUT}}$. As shown in (2), $V_i$ and $V_r$ are separated to obtain an impedance measurement.

### B. Calibration Method

The calibration aims at de-embedding the *S* parameter measured at the PoT level (4) to move the calibration plane at the DUT (3) input. This calibration process also compensates all the imperfections and error sources (e.g., imperfect TLP output matching, cable, and PoT attenuation). This method is detailed in [11]

$$\begin{cases} V_{\mathrm{PoT}} = V_i(0,f) + V_r(0,f) \\ S_{\mathrm{PoT}}\ (0,f) = \frac{V_r(0,f)}{V_i(0,f)} \end{cases} \tag{4}$$

$$S_{11} = \frac{S_{\mathrm{PoT}} - e_{00}}{\Delta e - e_{11} S_{\mathrm{PoT}}} \tag{5}$$

$$\Delta e\ = e_{10}\, e_{01} - e_{00} e_{11}. \tag{6}$$

$S_{11}$ is seen through a quadrupole error. It can be extracted from $S_{\mathrm{PoT}}$ through (5) and (6). The terms $e_{xx}$ are the elements of an error coefficient matrix [*E*], which are extracted by a series of three measurements on three reference loads. The error coefficient matrix [*E*] is computed by solving the following equation:

$$[S]\ = [M]\ [E] \tag{7}$$

where [*S*] (8) contains the *S* parameters obtained by TLP-based TDR measurement done at the PoT. Measurements on 50 Ω, open and short, are performed at high voltage using TLP. [*M*] is the matrix shown in (10)

$$[S]\ = \begin{pmatrix} S_{\mathrm{PoT\ 50\ \Omega}} \\ S_{\mathrm{PoT\ open}} \\ S_{\mathrm{PoT\ short}} \end{pmatrix} \tag{8}$$

$$[E]\ = \begin{pmatrix} \Delta e \\ e_{00} \\ e_{11} \end{pmatrix} \tag{9}$$

$$[M]\ = \begin{pmatrix} S_{\mathrm{VNA\ 50\ \Omega}} & 1 & S_{\mathrm{PoT\ 50\ \Omega}} S_{\mathrm{VNA\ 50\ \Omega}} \\ S_{\mathrm{VNA\ open}} & 1 & S_{\mathrm{PoT\ open}} S_{\mathrm{VNA\ open}} \\ S_{\mathrm{VNA\ short}} & 1 & S_{\mathrm{PoT\ short}} S_{\mathrm{VNA\ short}} \end{pmatrix}. \tag{10}$$

Some differences could exist between the calibration if the setup uses a VNA at a low-level injection and calibration uses TLP at a high level of injection. [*M*] is obtained using VNA measurement of the setup to compensate the effect of high pulse injection of TLP.

### C. Model Extraction Method Algorithm

The mathematical computation presented above was implemented in MATLAB software. The principle is described in Fig. 3. This algorithm has two types of input data. The first type consists of error coefficients, as computed in the previous part. The second type is a series of two voltage measurements performed at high-level injection: one on a matched load (to extract $V_i$), and the other on the DUT load ($Z_{\mathrm{DUT}}$). The output is the *S* parameters of the load, eventually converted in impedance $Z_{\mathrm{DUT}}$, given as a Touchstone, *S*1*p* file, which can be directly imported as a black-box model in an electrical simulator, such as an advanced design system (ADS).

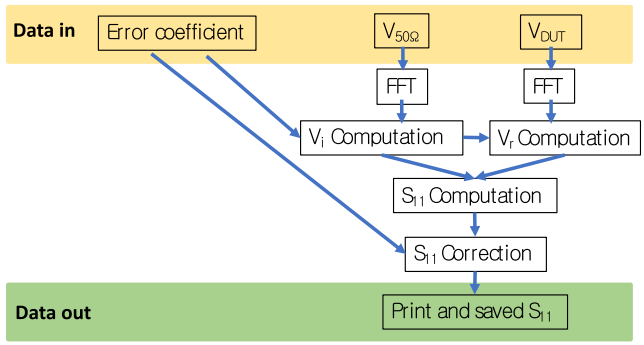


Fig. 3. Flow diagram of the model extraction method.

TABLE I
TESTED COMPONENT SPECIFICATIONS

| Component | Reference | Specification |
|---|---|---|
| Resistor 2R | Yageo RC0805FR-072RL | 2 Ω, 0.125 W |
| Resistor 470R | TE Connectivity CRG0805F470R | 470 Ω, 0.125 W |
| C0G capacitor | Vishay VJ0805A102JXBAT | 1 nF, $V_{max}$ = 100 V |
| TVS1 | Nexperia PESD5V0L1BA 115 | $V_t$ = 7 V, $P_{max}$ = 500 W Ron = 0.35 Ω |
| TVS2 | ST Microelectronics SM6T68CA | 68 V, 600 W Ron = 0.49 Ω |

## III. Validation of the Proposed Approach on Passive Linear Loads

### A. Experimental Setup

To validate the method, the impedance of several passive loads is measured, whose specifications are listed in Table I. Components are mounted on a PCB at around 1 cm from an subminiature version A connector (SMA) connector used for the injection. The characteristic impedances of the PCB lines are 50 Ω. Distance between the PoT and the DUT through cable, connectors, and PCB is approximately 5 cm. The setup is the one provided by high power pulse instruments (HPPI) to perform *I*(*V*) characteristics of protection devices. The setup could be any commercial very fast TLP measurement system as it works in the same amplitude range. References of the materials are listed in Table II. The duration of the pulse generated by the TLP is 100 ns and the rise time is equal to 100 ps, which is the faster rise time available with this TLP generator. Having a faster rise time would get access to models with a higher frequency range (using a 100 ps rise time could permit to have equivalent

TABLE II
MATERIAL SPECIFICATIONS

| Material | Reference | Specification |
|---|---|---|
| TLP | HPPI TLP8010C | $V_{max}$ = 4 kV, $I_{max}$ = 80 A<br>$t_r$ = 100 ps<br>Adapter 50 Ω |
| | | |
| PoT | HPPI-PT-45A | $Z_{PoT}$ = 2.2 kΩ<br>Attenuation factor: 45<br>BW = 18 GHz |
| Oscillocope | Tektronix DPO71254C | 100 GS/s, BW = 12 GHz |

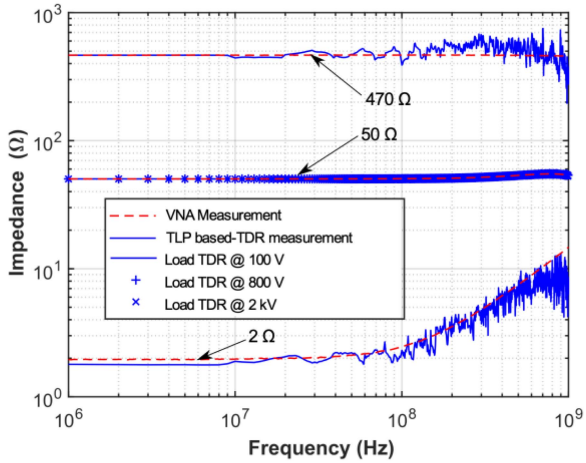


Fig. 4. Comparison of the impedance obtained by TLP-based method and VNA for 2 Ω, 470 Ω load and calibration on 50 Ω load.

to 3.5 GHz bandwidth). In the proposed applications, results are presented up to 1 GHz. For linear passive components, the impedance is also measured by a VNA in order to get a reference impedance.

In the first step, all the components were tested to determine their breakdown voltage. The limit is set so as to have a perfect linear regime and prevent any drift of characteristics due to an accelerated aging [24].

### B. Impedance Extraction Results

*1) 2 Ω and 470 Ω Load:* To validate the method of getting the impedance $Z(f)$ from TLP measurement, two resistances are tested first: 2 Ω and 470 Ω. The 2 Ω resistance is typical of an activated ESD protection impedance. The 470 Ω resistance behaves as a nonactivated or beginning activated protection showing a high impedance. For both devices, $S$ parameters are extracted using the TLP-based TDR at 100 V injection.

Fig. 4 reports the module of the computed impedance $Z(f)$ of both resistors compared with their measurement using VNA. The figure also includes the calibration on a 50 Ω load from VNA obtained at different pulse injections (100 V, 800 V, and 2 kV) using the TLP-based TDR method. It can be noticed that whatever is the pulse injection, the calibration load result fits perfectly with the VNA measurement. The extracted impedances 2 Ω and 470 Ω fit well with VNA measurement up to 1 GHz. In low frequency, TLP-based TDR gives the exact value of the 470 Ω resistance. A small difference is observed for the 2 Ω. The TLP-based TDR provides a value of 1.8 Ω. From

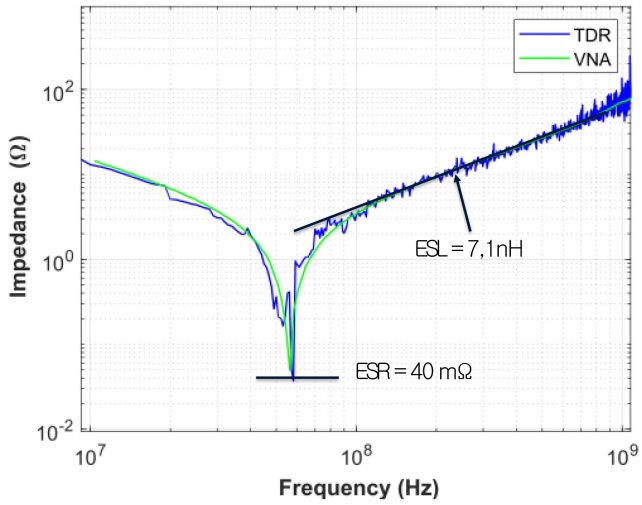


Fig. 5. Comparison between VNA and TLP-based TDR measurements on the 1 nF C0G capacitor.

100 MHz to 1 GHz, some moderate noise appears but similar behavior is measured with both methods. A part of this noise is due to computation approximations and noise on the transient measurement. Above 1 GHz, more noise appears and the result is not presented. For this study, we assume that a bandwidth of 1 GHz (approximately 300 ps rise time) is enough to reproduce a transient event due to system level ESD. As system level stresses (according to the IEC 61000-4-2) exhibit a rise time of 700 ps, the 300 ps equivalent rise time is sufficient to characterize the response of the device.

*2) C0G Dielectric Capacitance:* C0G dielectric is an extremely stable capacitor, leading to a linear behavior. Its properties do not vary with voltage. As well as for the previous resistive loads, TLP-based TDR (100nbsp;V injection, 100 ps rise time) measurements are compared to VNA measurement and reported in Fig. 5. The module of the extracted impedance fits very well with the VNA measurement. Between 1 MHz and 1 GHz, the gap is under 1%. The resonance peak is also well reproduced. We can extract with both measurement methods the equivalent serial resistance around 40 mΩ and the same equivalent serial inductance (ESL), which is about 7.1 nH. In this case, the DUT is composed of one capacitor and a short length of PCB trace explaining the large ESL.

The measurements of both resistors and the C0G capacitor validate that TLP measurement with 100 ps rise time can provide the impedance of devices under strong pulse injection up to 1 GHz with good accuracy. Some noise could appear around 1 GHz compared with VNA measurement. We have to assume that the extraction of the impedance is performed in one single pulse and we can see the limits of such method compared with VNA. But this method allows to get access to frequency parameters even in a high pulse injection regime without destroying the device.

### C. Validation of the Simulated Transient Behavior

The second step of validation is to compare transient measurements and simulations issued from the component model

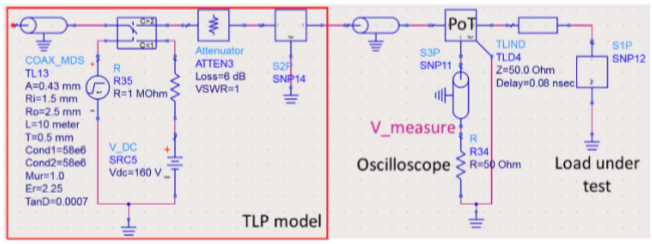


Fig. 6. Electrical diagram simulation into ADS software.

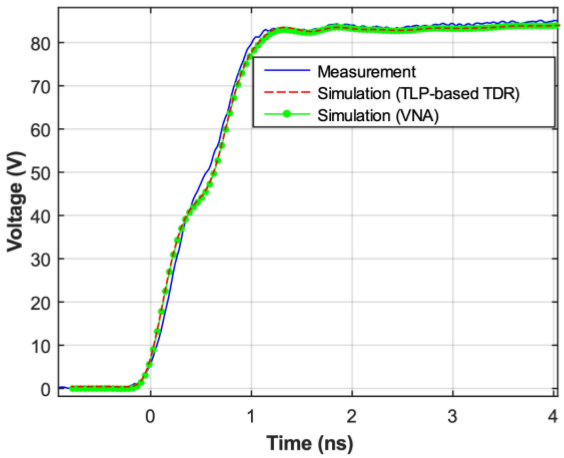


Fig. 7. Transient measurement versus simulations using VNA and TLP-based TDR models for 470 Ω load.

extracted from TLP-based TDR. The simulations are made with ADS software. For the previous linear devices, simulations are computed using *S* parameter from TLP-based TDR measurement and from VNA measurement. These measurements are loaded in a « *S1P* » box. The frequency range of the *S* parameter is 1 MHZ–1.2 GHz. The TLP generator electrical model is provided by the TLP manufacturer (HPPI) and has been validated through comparison with measurement on calibration loads. The schematic simulation, including the TLP, the PoT, and the load under test, is described in Fig. 6.

In Fig. 7, the measurement of the voltage under 100 V pulse across the 470 Ω resistor is compared with the simulations based on the models extracted either with TLP-based TDR or VNA.

The measured and simulated voltages in the steady-state regime are identical. During the transient regime, the first part of the rising transition is modeled correctly. The gap in the transient part is 3% for both TLP-based and VNA extracted models. We cannot see the difference between the results given by the VNA and TLP-based TDR models. The small step at 50 V is equal to $V_i$ and its duration is due to the time delay introduced by the connector and the short PCB trace. The simulated step is a little bit long due to a longer cable between DUT and PoT introduced into the simulation. The estimated overshoot with both models is in excellent agreement with the measured one. The influence of the noise observed in the measurement of the impedance in the frequency domain, *Z*(*f*), does not affect the transient simulation result.

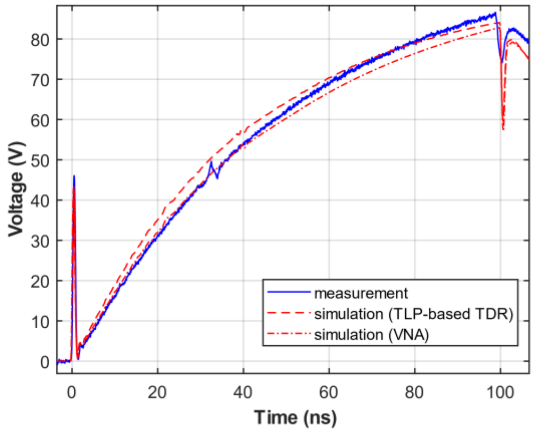


Fig. 8. Transient measurement versus simulation for C0G capacitor load.

The second case study concerns the C0G capacitor. The measured and simulated transient waveforms are shown in Fig. 8. A good match appears between the measurement and the simulation results obtained from TLP-based TDR and VNA extracted models. In this case, a small difference exists between TLP-based TDR and VNA models. The maximum gap between the measured and simulated waveforms is 11%. The measurement of the TLP-based TDR measurement enables to simulate the transient response of linear load under a high voltage pulse with an acceptable accuracy.

## IV. Characterization and Modeling of Nonlinear Passive Load

In this part, a passive nonlinear load (i.e., its behavior changes with the applied voltage) is characterized with the TLP-based TDR in order to extract a model for the transient simulation. The two TVSs, whose characteristics are given in Table II, are used as case studies. In this part, the relevance of the linear assumption is tested. Because of its nonlinear behavior, the VNA measurement cannot be used as a reference. To have the first understanding of its behavior, the study will focus on the TVS1 whose quasi-static *I*(*V*) curve is reported in Fig. 9.

Below the triggering voltage $Vth = 7.5$ V, the protection is not activated, leading to a very high impedance (open). Above *Vth*, the protection is activated and its equivalent dynamic resistance *Ron* is 0.35 Ω. Three TLP-based TDR computed impedances of the TVS1 are given in Fig. 10, corresponding to the following points A, B, and C, as reported in Fig. 9:

1) A at 5 V injection, below *Vth*;
2) B at 10 V injection just at the triggering voltage of the protection *Vth*;
3) C at 80 V when the protection is fully activated.

As shown in Fig. 10, the three impedance curves are different. For pulse voltage less than *Vth*, TDR@5 V, the measurement shows that the TVS has a capacitive behavior, with an equivalent capacitance of 63 pF. It is consistent with the value of 70 pF given by the datasheet. For pulse amplitude close to *Vth*, TDR@10 V, the low frequency exhibits a resistance around 180 Ω. The evolution of the impedance for frequency higher than 10 MHz

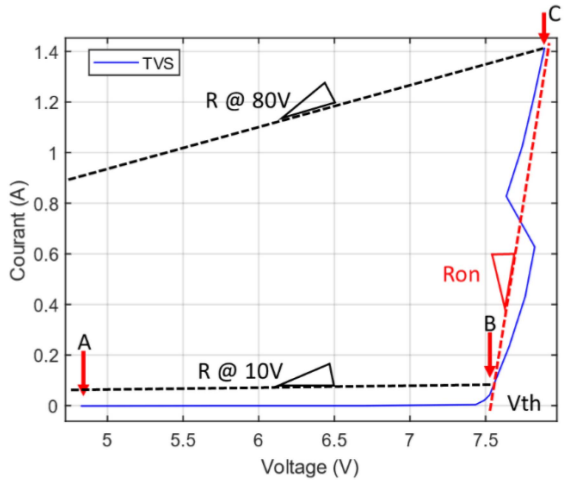


Fig. 9. Quasi-static $I(V)$ curve of the TVS1.

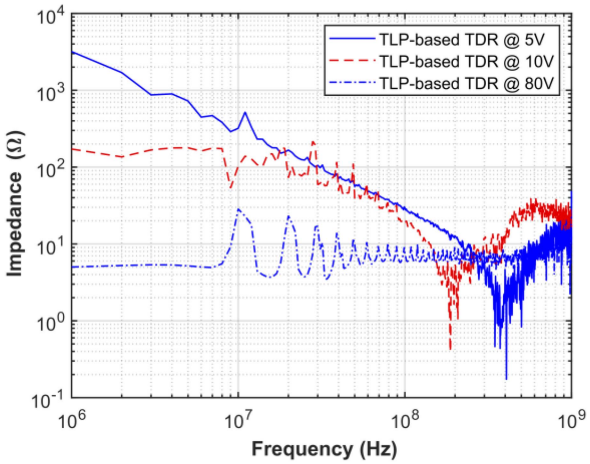


Fig. 10. Measured impedance of the TVS1 for different pulse voltages.

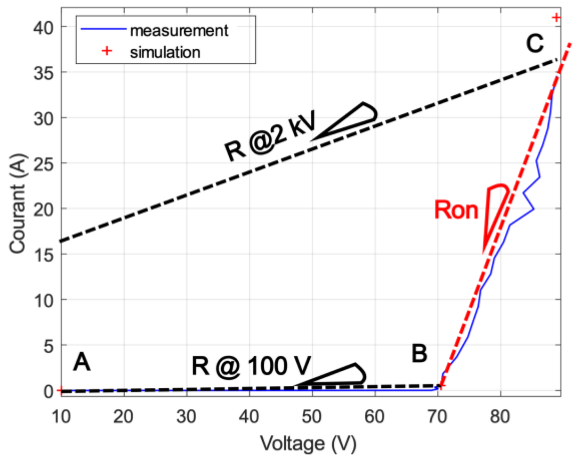


Fig. 11. Quasi-static $I(V)$ curve of the TVS2.

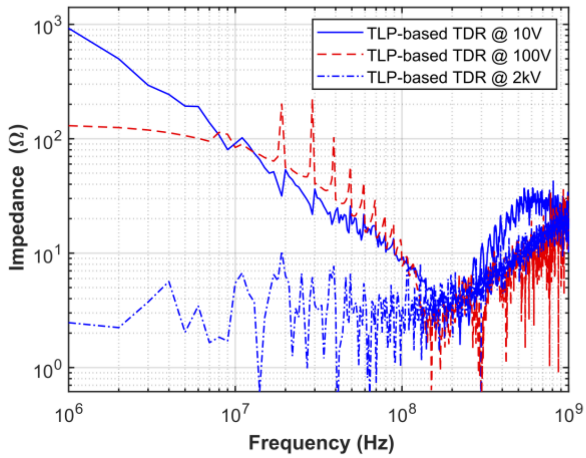


Fig. 12. Measured impedance of the TVS2 for different pulse voltages.

shows a complex behavior. B, the operating point, obtained for 10 V injection, is given at 7.6 V with 0.05 A. The equivalent quasi-static resistance is equal to 152 Ω, resulting in a difference of 16%. The most complex and nonlinear behavior is obtained around the triggering point. For 80 V injection, following the same way of thinking, the operation point (C) is at 7.8 V for 1.4 A. It leads to an equivalent quasi-static resistance of 5.6 Ω, $R$@80 V, which fits with the value of 5.3 Ω obtained with our TLP-based TDR measurement. At high frequency (> 700 MHz), the impedance is dominated by the TVS parasitic inductance. We can expect that the TVS initial transient response will be dominated by this parasitic inductance.

The same study is performed for TVS2. Fig. 11 reports its quasi-static $I(V)$ response. As for TVS1, we focus on the three similar operating points. Fig. 12 reports the impedance obtained for the three levels of TLP injection: 10 V, 100 V, and 2 kV. This TVS triggers at 68 V, with a higher level of robustness. The behavior is similar to the one observed with TVS1. It can be noticed that the effect of the parasitic inductance appears above 200 MHz. This corresponds to the characteristics of this TVS, which has to withstand a larger power, and is mounted within a bigger packaging. When this protection has triggered (at 100 V and 2 kV), some noise is observed at low frequency. This noise is related to the limit of the LTI assumption. The acquisition of the waveform is done during some hundreds of nanoseconds and the pulse duration is 100 ns. At the rising edge, the protection triggers, exhibiting the turn-ON behavior. At the falling edge of the pulse, the protection is already turned ON and the behavior is different. In such a case, the algorithm to get the $S$ parameters to form the transient measurement is limited, and noise is generated. This is the main limitation of the LTI approximation: it generates noise mainly in the low-frequency domain. The main question is how these obtained models are able to reproduce the transient behavior in the time domain.

### A. Comparison Measurement Versus Simulation of the Transient Behavior

The first step consists in simulating the behavior of the TVS below the triggering voltage. Fig. 13 shows the comparison between the measurements and simulations using the TLP-based TDR extracted models for TVS1 and TVS2, at 5 V and 10 V, respectively. The rise time has been set at 300 ps while the models have been extracted with a TLP rise time of 100 ps.

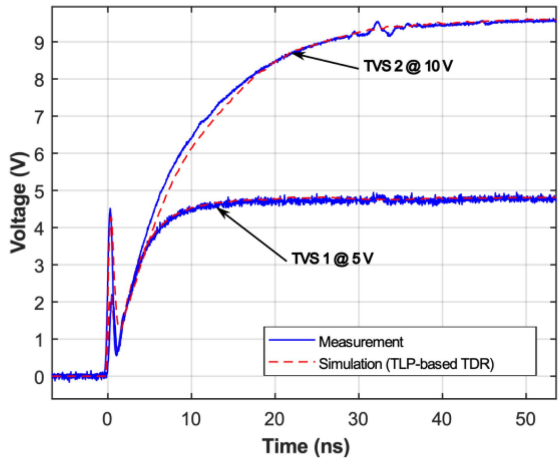


Fig. 13. Transient measurement versus simulation of TVS for 5 V TLP pulse.

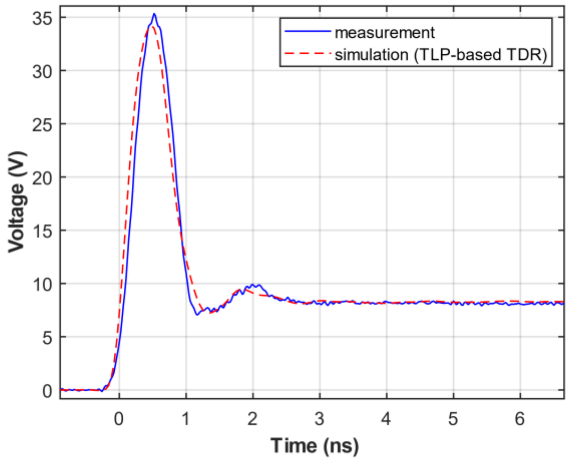


Fig. 14. Transient measurement versus simulation of TVS for 80 V TLP pulse.

The simulated transient responses are similar to the measured curves. The quasi-static level is exactly at more or less 1%. The charge time is reproduced correctly. This excellent fit is expected, as both devices operate in a quasi-linear regime.

Figs. 14 and 15 show the comparison between the measurement and simulation of the transient response for TVS1 at 80 V and TVS2 at 2 kV TLP injection, respectively. Both results show a very good fit between the measurement and simulation. The quasi-static level merges with the measurement. The simulated and measured initial transient responses are similar. In spite of the linear LTI assumption used to extract the TVS models, the dynamic responses of the transient trigger of the TVS are correctly predicted, especially the magnitude of the initial overshoot.

### B. Simulation on a Protection Network

The validity of the frequency models extracted, based on the TLP-based TDR method, is evaluated through a more complex network with a *CRC* structure and a TVS, as reported in Fig. 16. Starting from the input of the PCB, the network is composed of TVS1, followed by a *CRC* structure made of 1 nF C0G capacitors and a 2 Ω resistance. The previous frequency models are used

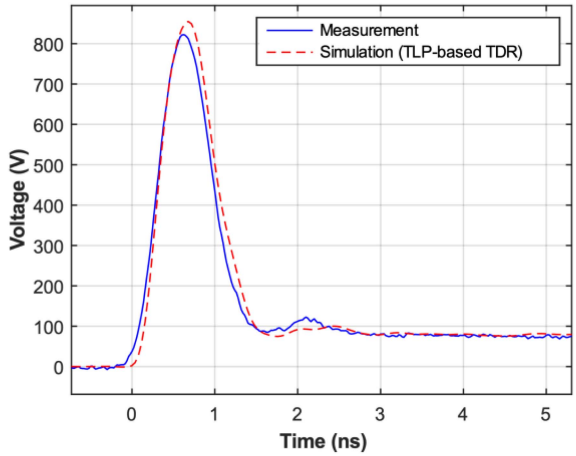


Fig. 15. Transient measurement versus simulation of TVS2 for 2 kV TLP pulse.

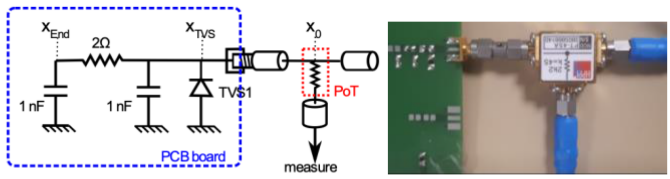


Fig. 16. Schematic and photograph of the *CRC*+TVS network.

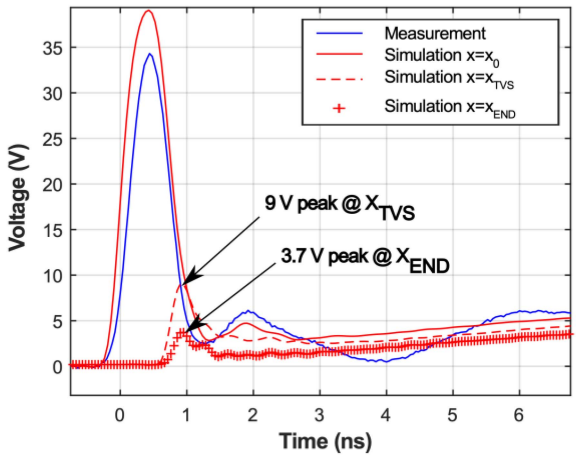


Fig. 17. Transient measurement and simulation of the TVS+*CRC* network.

in ADS simulator to estimate the resulting overshoot at the end of the network ($x_{\mathrm{end}}$). The measurement can only be performed outside the PCB ($x0$). We also take attention to the overshoot at the TVS1 diode ($x_{\mathrm{TVS}}$). Measurement results at $x0$ and the simulations performed at $x_0$, $x_{\mathrm{TVS}}$, and $x_{\mathrm{end}}$ are reported in Fig. 17 with 80 V TLP injection.

At $x_0$, the simulation overestimates the measurement by 14%, but the error is not so important, as this first peak is meanly related to the delay line between the measurement and DUT. The model accuracy can be improved by a more precise model of the PCB. The validation at $x_0$, where measurement can be done, allows to extrapolate the waveforms at $x_{\mathrm{TVS}}$ and $x_{\mathrm{end}}$. Values are reported in Fig. 17. The first overvoltage peaks are estimated

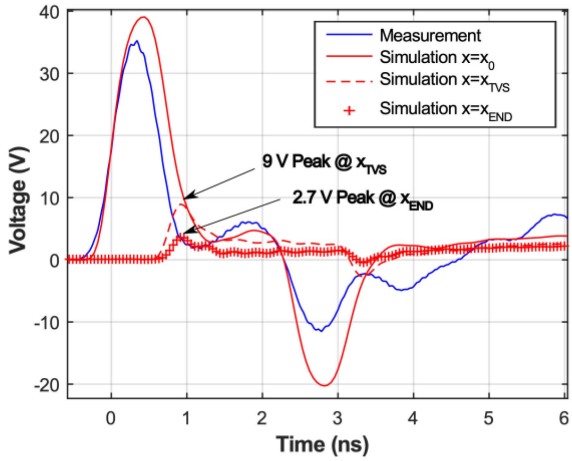


Fig. 18. Transient measurement and simulation of a 80 V HMM pulse TVS1+*CRC* network.

at 9 V at the TVS and 3.7 V at the end of the network. The measurement shows some oscillations between 2 and 10 ns, not visible in the simulation results. After 15 ns, a small difference appears during the charge of the network, which is not explained at this time. Some possible reasons could be related to the low-frequency noise we have on the measurement of the TVS, due to the LTI approximation.

### C. *HMM Response of a* CRC *Plus TVS Network*

To finalize the study, a human metal model (HMM) [26], [27] stress is injected on the previous protection network. The HMM pulse has the same waveform as the one defined by IEC 61000-4-2, but the stress is directly applied to the input pin of the board, and the return ground is directly connected to the ground of the PCB. In our study, the HMM generator from HPPI is used, whose output is a 50 Ω matched. To validate our HMM model in the simulator, a preliminary comparison between the measurement and simulation has been performed on a 50 Ω resistor. We decided not to report this simulation but the first peak is well reproduced with a relative error of 10% on the second peak.

Fig. 18 reports the simulation results while an HMM stress of 80 V is injected into the TVS1+*CRC* network. The observations are similar to the TLP injection case. The first peak is overestimated of nearly 10%. But an estimation of the peak at the TVS and at the end of a network can be obtained to predict the effectiveness of this protection network.

## V. Conclusion

This article has presented a TLP-based TDR method to facilitate the ESD protection device model construction in order to simulate their transient response to high voltage fast pulses. The proposed model is based on *S* parameter black-box macromodels that can be directly imported in SPICE simulator, without any tedious and time-consuming model fitting phase. The setup and algorithm to compute the frequency models are presented and validated on several passive linear loads (resistors and capacitors). Transient simulations are performed to verify that the transient behavior can be predicted using such models.

Although the proposed method relies on the LTI assumption, validation case studies on two different TVS confirm that the transient response of such a nonlinear device can be simulated with good precision, up to 2 kV TLP (40 A). In the article, we focus on 100 V and 2 kV, TLP, which have an equivalent current injection of 10 kV IEC gun stress, to clearly show the range permitted by the system. But there is no restriction for injection level between these two values. For higher injection level, more caution should be taken to protect the materials measurement. Regarding the simulation results using the *S* parameter black box, the first nanoseconds, which are crucial to predict the overvoltage of protection devices, are well reproduced. Related to the limit of the LTI assumption, quasi-static level exhibits some variations in the simulation. The noise observed in low frequency introduces a little oscillation in the quasi-static regime. Some improvement in the model extraction algorithm is certainly required to compensate this effect. Nevertheless, this technique was developed to get access to the first nanoseconds of the protections triggering and this was perfectly done. Quasi-static level can be easily simulated with conventional models.

Using frequency simulation, a protection network model was developed. This case demonstrates that the frequency model could be used in a simple manner to estimate its effectiveness to protect sensitive devices. Measurement and simulations were compared at the measurement point with good agreement. As a result, the proposed frequency model extracted using TLP setup is useful to perform prediction under system level ESD conditions. This model has the advantage to be easily built, as a black-box model. Its use requires to take attention to the energy. One model remains valid for a given pulse energy.

## Acknowledgment

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