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This index covers all technical items—papers, correspondence, reviews, etc.—that appeared in this periodical during 2019, and items from previous years that were commented upon or corrected in 2019. Departments and other items may also be covered if they have been judged to have archival value.

The Author Index contains the primary entry for each item, listed under the first author's name. The primary entry includes the coauthors' names, the title of the paper or other item, and its location, specified by the publication abbreviation, year, month, and inclusive pagination. The Subject Index contains entries describing the item under all appropriate subject headings, plus the first author's name, the publication abbreviation, month, and year, and inclusive pages. Note that the item title is found only under the primary entry in the Author Index.

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Optimizing File Systems with a Write-Efficient Journaling Scheme on Non-Volatile Memory. *Zhang, X.*, +, *TC March 2019 402-413*

PaRS: A Popularity-Aware Redundancy Scheme for In-Memory Stores. *Zhou, P.*, +, *TC April 2019 556-569*

Phantasy: Low-Latency Virtualization-Based Fault Tolerance via Asynchronous Prefetching. *Ren, S.*, +, *TC Feb. 2019 225-238*

String matching

Evaluating High Performance Pattern Matching on the Automata Processor. *Roy, I.*, +, *TC Aug. 2019 1201-1212*

Supervised learning

Dynamic Voltage and Frequency Scaling in NoCs with Supervised and Reinforcement Learning Techniques. *Fettes, Q.*, +, *TC March 2019 375-389*

Switches

An STT-MRAM Based in Memory Architecture for Low Power Integral Computing. *Zhao, Y.*, +, *TC April 2019 617-623*

Symmetric matrices

Better Circuits for Binary Polynomial Multiplication. *Find, M.G.*, +, *TC April 2019 624-630*

Synchronization

Self-Synchronized Encryption for Physical Layer in 10Gbps Optical Links. *Perez-Resca, A.*, +, *TC June 2019 899-911*

System recovery

RT-ByzCast: Byzantine-Resilient Real-Time Reliable Broadcast. *Kozhaya, D.*, +, *TC March 2019 440-454*

System-on-chip

An Energy-Efficient Accelerator Based on Hybrid CPU-FPGA Devices for Password Recovery. *Liu, P.*, +, *TC Feb. 2019 170-181*

Exploring Shared Virtual Memory for FPGA Accelerators with a Configurable IOMMU. *Vogel, P.*, +, *TC April 2019 510-525*

The Security of ARM TrustZone in a FPGA-Based SoC. *Benhani, E.M.*, +, *TC Aug. 2019 1238-1248*

T

Table lookup

Improved Affine Arithmetic-Based Precision Analysis for Polynomial Function Evaluation. *Bellal, R.*, +, *TC May 2019 702-712*

NV-eCryptfs: Accelerating Enterprise-Level Cryptographic File System with Non-Volatile Memory. *Xiao, C.*, +, *TC Sept. 2019 1338-1352*

SPARE: Spiking Neural Network Acceleration Using ROM-Embedded RAMs as In-Memory-Computation Primitives. *Agrawal, A.*, +, *TC Aug. 2019 1190-1200*

Task analysis

DR Refresh: Releasing DRAM Potential by Enabling Read Accesses Under Refresh. *Cao, Y.*, +, *TC Nov. 2019 1584-1596*

Telecommunication computing

Value Iteration Architecture Based Deep Learning for Intelligent Routing Exploiting Heterogeneous Computing Platforms. *Fadlullah, Z.M.*, +, *TC June 2019 939-950*

Telecommunication network reliability

Efficient Design-for-Test Approach for Networks-on-Chip. *Wang, J.*, +, *TC Feb. 2019 198-213*

Telecommunication network routing

CD-Xbar: A Converge-Diverge Crossbar Network for High-Performance GPUs. *Zhao, X.*, +, *TC Sept. 2019 1283-1296*

Efficient Design-for-Test Approach for Networks-on-Chip. *Wang, J.*, +, *TC Feb. 2019 198-213*

Value Iteration Architecture Based Deep Learning for Intelligent Routing Exploiting Heterogeneous Computing Platforms. *Fadlullah, Z.M.*, +, *TC June 2019 939-950*

Telecommunication network topology

CD-Xbar: A Converge-Diverge Crossbar Network for High-Performance GPUs. *Zhao, X.*, +, *TC Sept. 2019 1283-1296*

Value Iteration Architecture Based Deep Learning for Intelligent Routing Exploiting Heterogeneous Computing Platforms. *Fadlullah, Z.M.*, +, *TC June 2019 939-950*

Telecommunication traffic

An Absorbing Markov Chain Based Model to Solve Computation and Communication Tradeoff in GPU-Accelerated MDRUs for Safety Confirmation in Disaster Scenarios. *Mao, B.*, +, *TC Sept. 2019 1256-1268*

CD-Xbar: A Converge-Diverge Crossbar Network for High-Performance GPUs. *Zhao, X.*, +, *TC Sept. 2019 1283-1296*

Value Iteration Architecture Based Deep Learning for Intelligent Routing Exploiting Heterogeneous Computing Platforms. *Fadlullah, Z.M.*, +, *TC June 2019 939-950*

Temperature distribution

On the Efficiency of Voltage Overscaling under Temperature and Aging Effects. *Amrouch, H.*, +, *TC Nov. 2019 1647-1662*

Sensors

Secure Tensor Decomposition for Big Data Using Transparent Computing Paradigm. *Kuang, L.*, +, *TC April 2019 585-596*

Theorem proving

CHERI Concentrate: Practical Compressed Capabilities. *Woodruff, J.*, +, *TC Oct. 2019 1455-1469*

Thermal noise

Microcontroller TRNGs Using Perturbed States of NOR Flash Memory Cells. *Poudel, P.*, +, *TC Feb. 2019 307-313*

Thermal variables control

An Aging-Aware GPU Register File Design Based on Data Redundancy. *Valero, A.*, +, *TC Jan. 2019 4-20*

Throughput

DR Refresh: Releasing DRAM Potential by Enabling Read Accesses Under Refresh. *Cao, Y.*, +, *TC Nov. 2019 1584-1596*

Time complexity

A New Cube Attack on MORUS by Using Division Property. *Ye, T., +, TC Dec. 2019 1731-1740*

Torque

HALLS: An Energy-Efficient Highly Adaptable Last Level STT-RAM Cache for Multicore Systems. *Kuan, K., +, TC Nov. 2019 1623-1634*

Training data

A Scalable Near-Memory Architecture for Training Deep Neural Networks on Large In-Memory Datasets. *Schuiki, F., +, TC April 2019 484-497*

Transaction processing

Maintaining Data Freshness in Distributed Cyber-Physical Systems. *Li, G., +, TC July 2019 1077-1090*

Transistors

An Aging-Aware GPU Register File Design Based on Data Redundancy. *Valero, A., +, TC Jan. 2019 4-20*

On the Efficiency of Voltage Overscaling under Temperature and Aging Effects. *Amrouch, H., +, TC Nov. 2019 1647-1662*

Tree data structures

CHERI Concentrate: Practical Compressed Capabilities. *Woodruff, J., +, TC Oct. 2019 1455-1469*

Trusted computing

The Security of ARM TrustZone in a FPGA-Based SoC. *Benhani, E.M., +, TC Aug. 2019 1238-1248*

Two dimensional displays

SqueezeFlow: A Sparse CNN Accelerator Exploiting Concise Convolution Rules. *Li, J., +, TC Nov. 2019 1663-1677*

U**Ubiquitous computing**

An Ontology-Based Method for HW/SW Architecture Reconstruction. *Musavi, S.A., +, TC July 2019 1007-1018*

Upper bound

Better Circuits for Binary Polynomial Multiplication. *Find, M.G., +, TC April 2019 624-630*

V**Virtual machines**

Disaggregated Cloud Memory with Elastic Block Management. *Koh, K., +, TC Jan. 2019 39-52*

GCMA: Guaranteed Contiguous Memory Allocator. *Park, S., +, TC March 2019 390-401*

Phantasy: Low-Latency Virtualization-Based Fault Tolerance via Asynchronous Prefetching. *Ren, S., +, TC Feb. 2019 225-238*

Virtual prototyping

Translation, Abstraction and Integration for Effective Smart System Design. *Lora, M., +, TC Oct. 2019 1525-1538*

Virtual storage

Enhancing Instruction TLB Resilience to Soft Errors. *Sanchez-Macian, A., +, TC Feb. 2019 214-224*

Virtualization

An Absorbing Markov Chain Based Model to Solve Computation and Communication Tradeoff in GPU-Accelerated MDRUs for Safety Confirmation in Disaster Scenarios. *Mao, B., +, TC Sept. 2019 1256-1268*

Disaggregated Cloud Memory with Elastic Block Management. *Koh, K., +, TC Jan. 2019 39-52*

Exploring Shared Virtual Memory for FPGA Accelerators with a Configurable IOMMU. *Vogel, P., +, TC April 2019 510-525*

Phantasy: Low-Latency Virtualization-Based Fault Tolerance via Asynchronous Prefetching. *Ren, S., +, TC Feb. 2019 225-238*

Visual communication

An Absorbing Markov Chain Based Model to Solve Computation and Communication Tradeoff in GPU-Accelerated MDRUs for Safety Confirmation in Disaster Scenarios. *Mao, B., +, TC Sept. 2019 1256-1268*

Viterbi algorithm

A Low-Power, High-Performance Speech Recognition Accelerator. *Yazdani, R., +, TC Dec. 2019 1817-1831*

W**Wireless sensor networks**

A Light-Weight White-Box Encryption Scheme for Securing Distributed Embedded Devices. *Shi, Y., +, TC Oct. 2019 1411-1427*

Write-once storage

Reducing Flash Memory Write Traffic by Exploiting a Few MBs of Capacitor-Powered Write Buffer Inside Solid-State Drives (SSDs). *Chen, X., +, TC March 2019 426-439*